University of Tehran

Electrical and Computer Engineering Department

Computer Architecture

Computer Assignment #3

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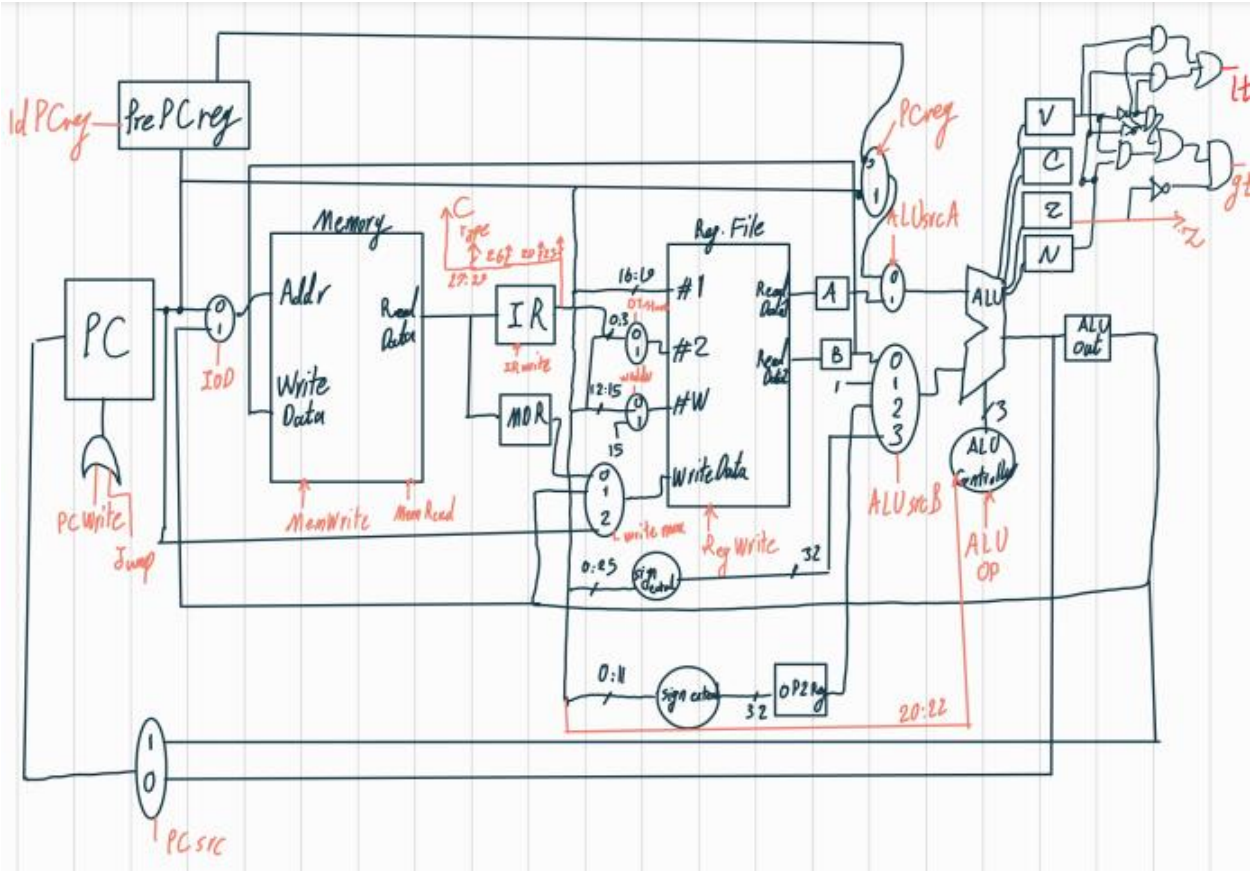
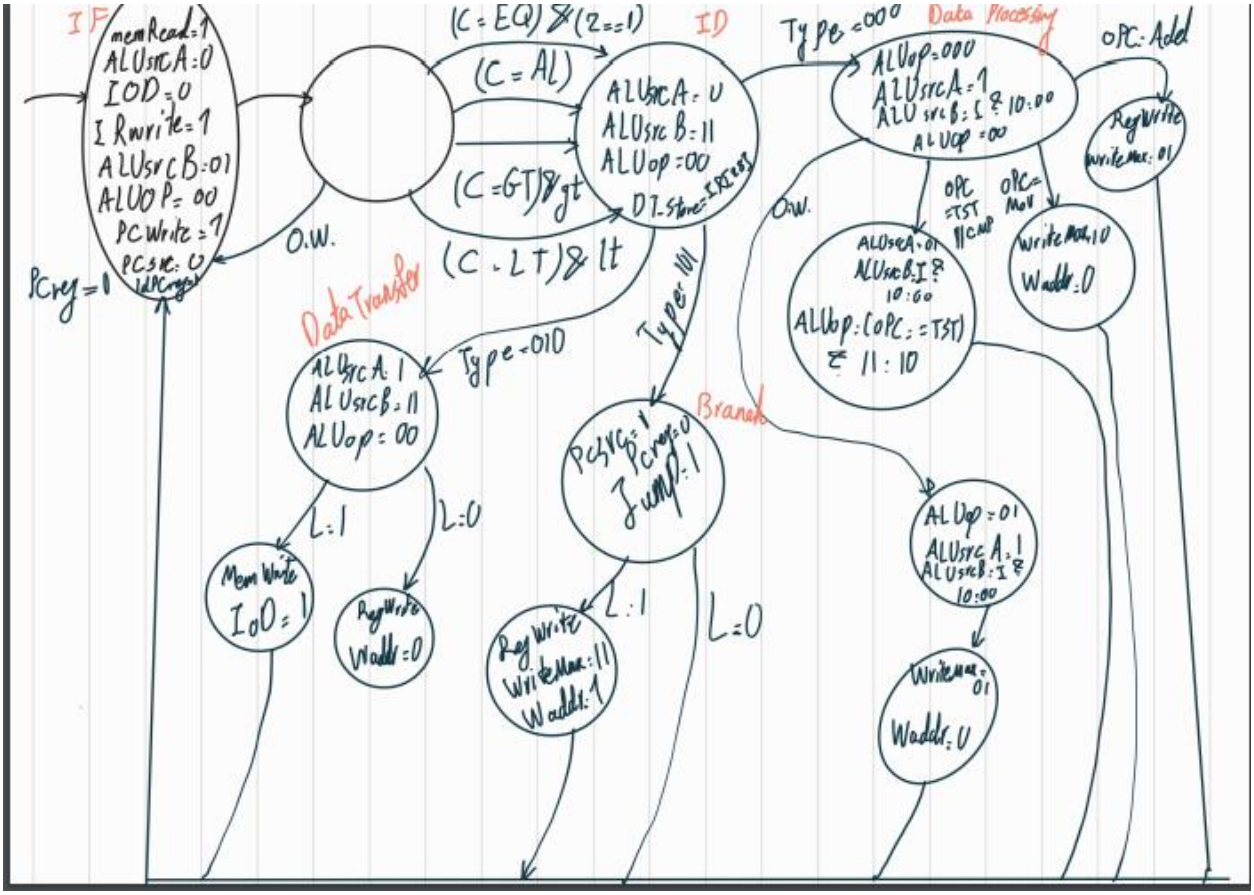
Date	Tuesday - 2022 04 January

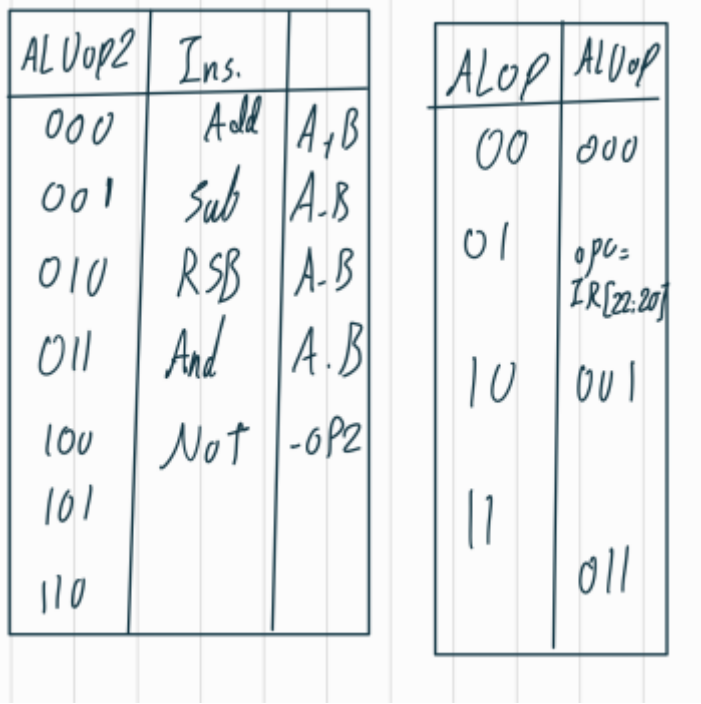
1. Datapath


Id PCreg
PrePCreg
PCreg
PC
IoD
Memory
Addr
Write Data
Read Data
IR
MDR
Reg. File
#1
#2
#W
Write Data
A
B
ALUsrcA
ALU
ALU out
V
C
Z
N
ALUsrcB
ALU Controller
ALU OP
PCwrite
Jump
MemWrite
MemRead
Reg Write
32
PCsrc
OP2reg
20:22

2. Control Unit



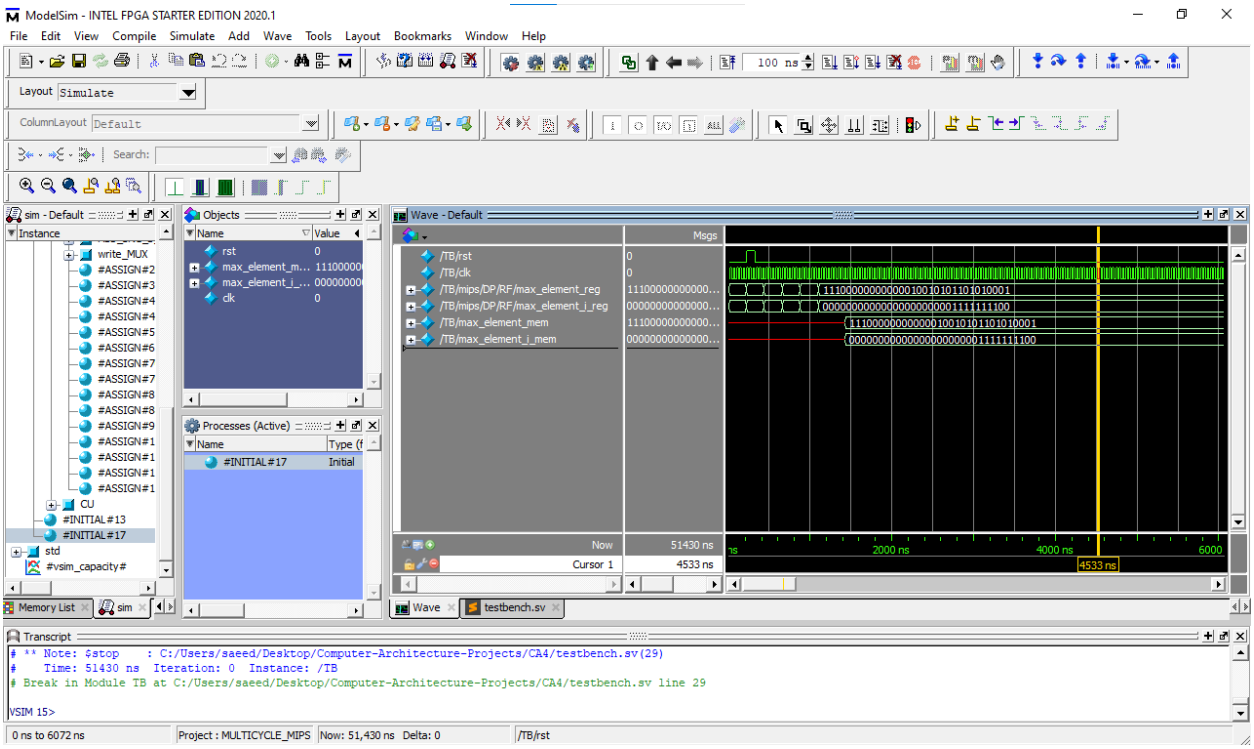
3. ALU Truth Table & Controller



ALUop2	Ins.	
000	Add	A+B
001	Sub	A-B
010	RSB	A-B
011	And	A.B
100	Not	~OP2
101		
110		

ALOp	ALUop
00	000
01	opc= IR[22:20]
10	001
11	011

Testbench


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/TB/rst
/TB/clk
/TB/mips/DP/RF/max_element_reg
/TB/mips/DP/RF/max_element_i_reg
/TB/max_element_mem
/TB/max_element_i_mem
Transcript
** Note: $stop : C:/Users/saeed/Desktop/Computer-Architecture-Projects/CA4/testbench.sv(29)
Time: 51430 ns Iteration: 0 Instance: /TB
Break in Module TB at C:/Users/saeed/Desktop/Computer-Architecture-Projects/CA4/testbench.sv line 29
VSIM 15>