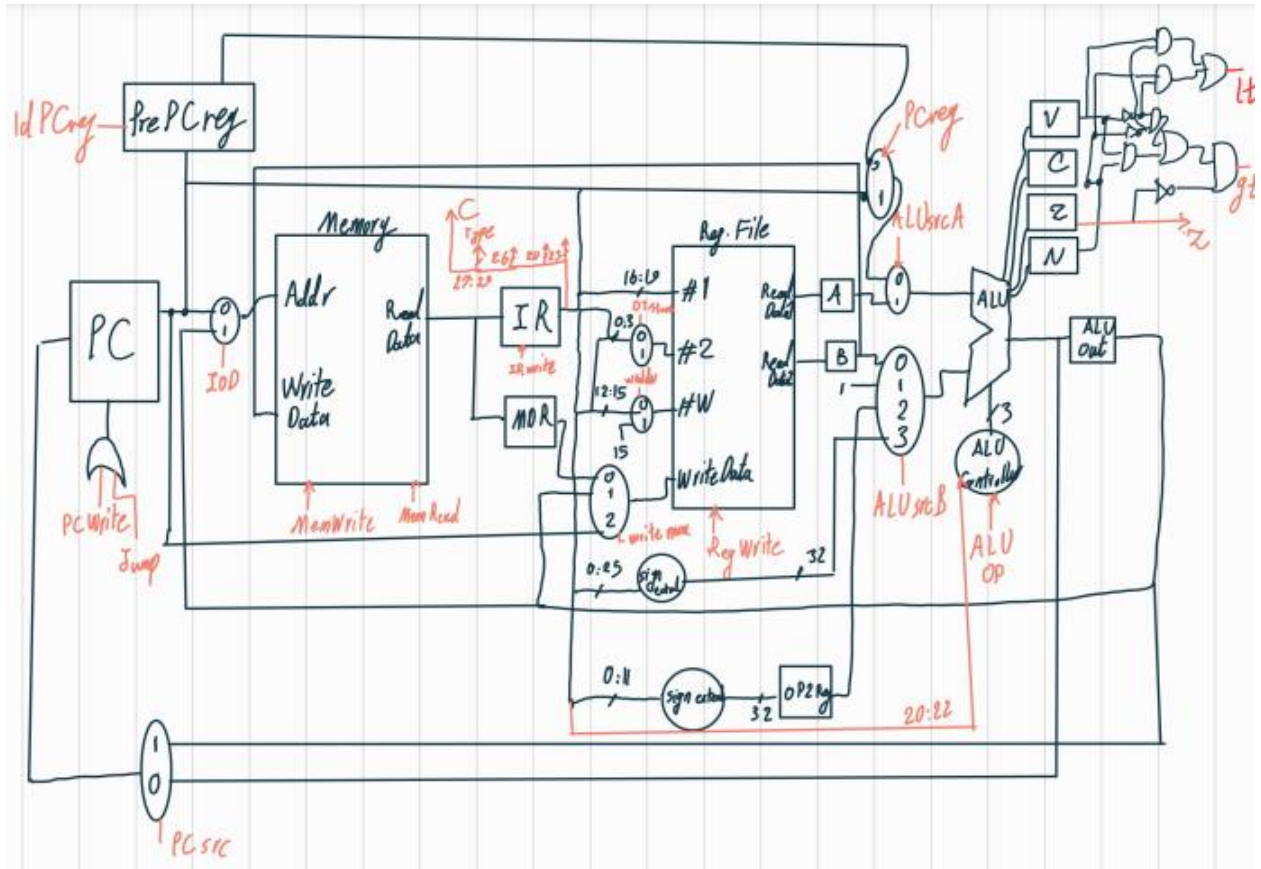




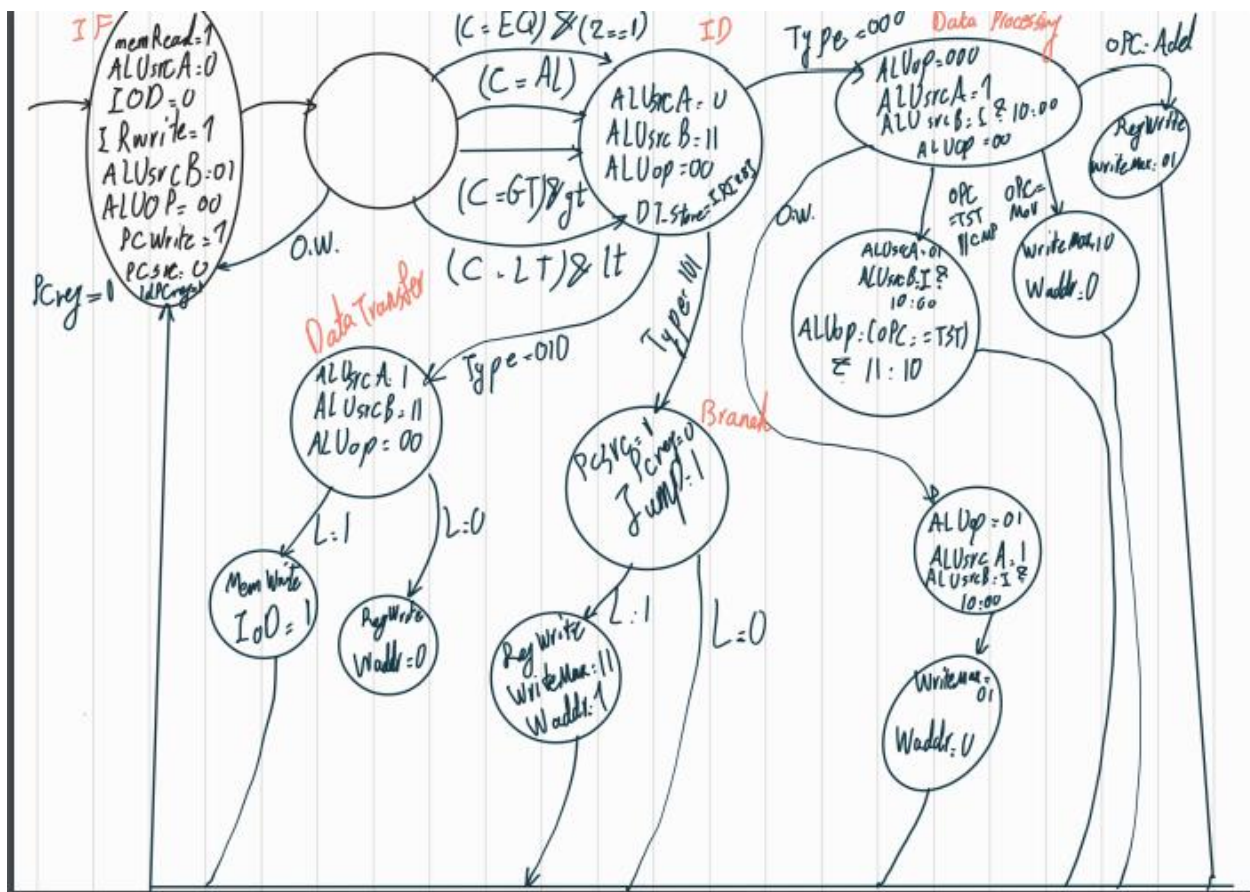
University of Tehran
Electrical and Computer Engineering Department
Computer Architecture
Computer Assignment #3

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Date	Tuesday - 2022 04 January

1. Datapath



2. Control Unit



3. ALU Truth Table & Controller

ALUop2	Ins.	
000	Add	$A+B$
001	Sub	$A-B$
010	RSB	$A-B$
011	And	$A \cdot B$
100	Not	$\neg OP2$
101		
110		

ALop	ALUop
00	000
01	$opc =$ $IR[22:20]$
10	001
11	011

The screenshot displays the Intel FPGA Starter Edition 2020.1 IDE. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Wave, Tools, Layout, Bookmarks, Window, and Help. Below the menu bar is a toolbar with various icons for file operations, simulation, and layout. The main workspace is divided into several panels:

- Layout:** Shows the current layout of the design, with a dropdown menu for selecting a layout.
- ColumnLayout:** A panel for managing the layout columns.
- Search:** A search bar for finding components or signals.
- Objects:** A panel showing the hierarchy of components in the design. It includes a tree view with components like 'Write_MUX', 'max_element_reg', 'max_element_mem', and 'CU'. The 'Processes (Active)' section shows the current process, '#INITIAL#17', with its initial state.
- Wave:** A panel displaying a timing diagram. It shows signals like 'rst', 'clk', and 'max_element_reg' over time. The diagram includes a cursor at 51430 ns and a yellow vertical line at 4533 ns.
- Transcript:** A panel showing the simulation log. It includes a note about the simulation path and a break statement in the testbench module.

The status bar at the bottom indicates the current time is 0 ns to 6072 ns, the project is 'MULTICYCLE_MIPS', and the current time is 51,430 ns with a delta of 0. The signal being monitored is 'TB/rst'.