University of Tehran

Electrical and Computer Engineering Department

Computer Architecture

Computer Assignment #4

MIPS Pipeline

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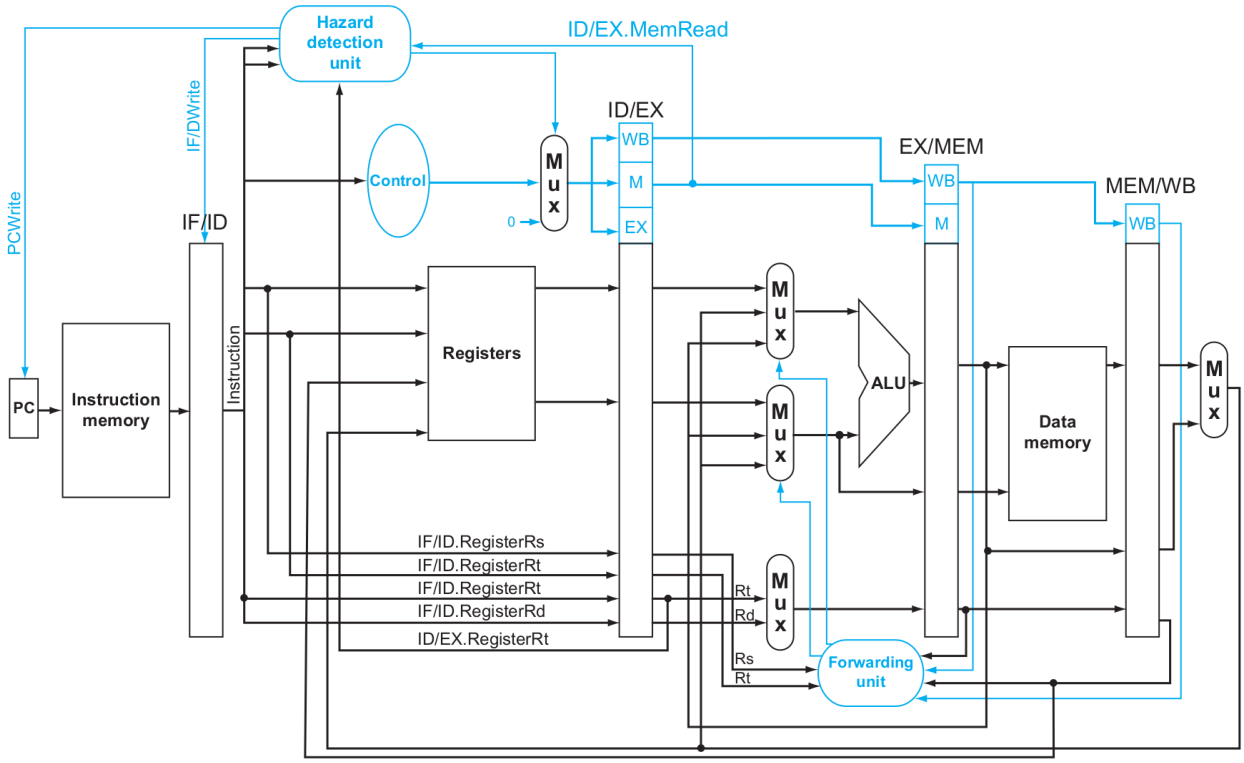
Date	Tuesday - 2022 04 January

1. Datapath


Hazard detection unit
ID/EX.MemRead
IF/DWrite
PCWrite
ID/EX
EX/MEM
MEM/WB
Control
M u x
0
WB
M
EX
IF/ID
PC
Instruction memory
Instruction
Registers
ALU
Data memory
IF/ID.RegisterRs
IF/ID.RegisterRt
IF/ID.RegisterRt
IF/ID.RegisterRd
ID/EX.RegisterRt
Rt
Rd
Rs
Rt
Forwarding unit

2. Control Unit

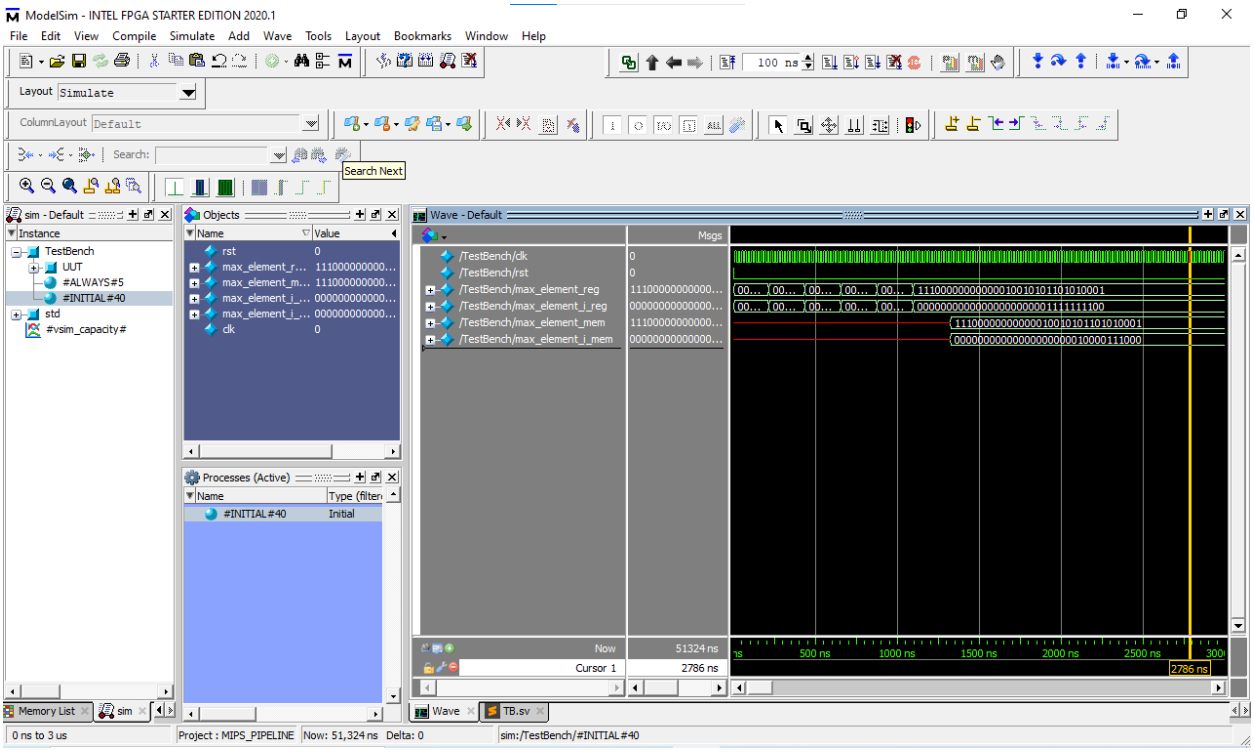
	ALUOp	MemtoReg	Reg_Write	Mem_Read	Reg_Write	Branch	ALUsrc	Id	regDst	writeDst	Mem_Write	Jump
add	101	0	1	0	0	0	1	0	0	000	0	00
sub	101	0	1	0	0	0	1	0	0	000	0	00
and	101	0	1	0	0	0	1	0	0	000	0	00
or	101	0	1	0	0	0	1	0	0	000	0	00
slt	101	0	1	0	0	0	1	0	0	000	0	00
addi	000	1	0	0	0	0	1	0	0	000	0	00
slti	011	1	0	0	0	0	1	0	0	000	0	00
lw	000	0	1	1	0	0	1	0	0	100	0	00
sw	000	0	0	0	0	0	1	0	0	000	1	00
beq	001	0	0	0	0	1	0	0	0	000	0	00
j	0	0	0	0	0	0	0	0	0	000	0	01
jr	0	0	0	0	0	0	0	0	0	000	0	10
jal	0	0	1	0	0	0	0	0	1	001	0	01

3. ALU Truth Table & Controller

ALUop	ALUoperation	func
000	0000	x
001	0111	x
010	1000	x
011	0110	x
100	0010	x
101	0000	add
101	0001	sub
101	0011	and
101	0100	or
101	0101	xor
101	0110	slt

ALU_Sel	Output
0000	In1 + In2
0001	In1 - In2
0011	In1 & In2
0100	In1 | In2
0101	In1 ^ In2
0110	slt
0111	Branch Equal
1000	Branch Not Equal

Testbench


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Search Next
sim - Default
Instance
TestBench
UUT
#ALWAYS#5
#INITIAL#40
std
#vsim_capacity#
Objects
Name
Value
rst
max_element_r...
max_element_m...
max_element_i_...
max_element_i_...
clk
Processes (Active)
Type (filter
#INITIAL#40
Initial
Wave - Default
Msgs
/TestBench/clk
/TestBench/rst
/TestBench/max_element_reg
/TestBench/max_element_i_reg
/TestBench/max_element_mem
/TestBench/max_element_i_mem
Now
51324 ns
Cursor 1
2786 ns
500 ns
1000 ns
1500 ns
2000 ns
2500 ns
Memory List
sim
Wave
TB.sv
0 ns to 3 us
Project : MIPS_PIPELINE
Now: 51,324 ns
Delta: 0
sim:/TestBench/#INITIAL#40