

## UNIVERSITY OF TEHRAN

## Electrical and Computer Engineering Department Digital Logic Design, ECE 367, Spring 1400 Computer Assignment 3

RT Level Components, Iterative Logic, Synthesis - Week 12

Name:	Date:
Username:	

The problem for this assignment is a circuit that calculates the number of 1's on its data inputs. The circuit that is to be designed has 127 inputs, and it is built of cascadable modules in a regular structure.

- 1 Show the design of a full-adder using basic gate structures. Using the delay values from transistors of Computer Assignment 1, estimate the worst-case gate delays of your full-adder structure. Write a parameterized full-adder and use the delay values in this SystemVerilog description. Simulate this structure and verify your worst-case delay values.
- 2. Based on delay values of the full-adder of Part 1, write a parametrized n-bit adder that uses n to adjust the size and delay value of the adder. The adder module uses #parameter(...) construct in its header part. For the delay values assume the adder is realized as a Ripple-carry adder. You can use an assign statement for this description. No need to do a structural description based on the full-adder.
- Test the adder of Part 2 for n value of 4 using a SystemVerilog testbench. Use constructs such as **repeat** and **\$random()** for test data generation.
- **4.** Using SystemVerilog **generate** statement wire n-bit adders (where n is 1 to 6) in a tree structure to build a 127-bit one's counter.
- 5. Pest your design of Part 4 for functionality and timing using a SystemVerilog testbench. Among other tests, in the testbench generate a 127 bit Marching-1 data generator for providing data to your counter.
- Using SystemVerilog **always** and procedural **for** statements write a synthesizable description of the One's Counter of Part 4. Annotate this description with delays obtained from the SystemVerilog of Part 4. Run simulations and compare results.
- 7. Using YoSys synthesize the circuit of Part 4 and that of Part 6 and compare the results.