UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Spring 1399-1400
Computer Assignment 5
State Machine Coding, Pre- and Post-Synthesis
Week 24

Name:
Date:

In this experiment, you are to design and implement a Moore and Mealy **10010** detector in SystemVerilog and implement and test them in Quartus. You will use pre-synthesis and post-synthesis descriptions of the same machine and compare simulation results. You will also use pre-synthesis descriptions of a Moore and a Mealy implementation and again see the differences.

a. Write a complete behavioral SystemVerilog description of a Moore machine that detects the **10010** sequence. Use an asynchronous reset and the positive edge of the clock. This is your pre-synthesis design of the Moore **10010** detector.
   i. Using a SystemVerilog testbench in the ModelSim simulation environment completely simulate your circuit. This is your pre-synthesis description.
   ii. Import your Moore design in Quartus and build a symbol for it. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of your Moore 10010 detector. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
   iii. Instantiate the pre- and post-synthesis descriptions of the Moore machine in a SystemVerilog testbench and compare the timing of the two descriptions.

b. Write a complete behavioral SystemVerilog description of a Mealy machine that detects the **10010** sequence. Use an asynchronous reset and the positive edge of the clock. This is your pre-synthesis design of the Mealy **10010** detector.
   i. Using a SystemVerilog testbench in the ModelSim simulation environment completely simulate your circuit. This is your pre-synthesis description.
   ii. Import your Mealy design in Quartus and build a symbol for it. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of your Mealy **10010** detector. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
   iii. Instantiate the pre- and post-synthesis descriptions of the Mealy machine in a SystemVerilog testbench and compare the timing of the two descriptions.

c. In a SystemVerilog testbench instantiate the post-synthesis Moore and post-synthesis Mealy machines and run simulations to verify their operations and their differences. Make sure you apply data inputs that illustrate where the outputs are different.
   i. In your testbench use an **assign** statement to show the differences between the two outputs. This can simple be done by XORing the two outputs.
   ii. Be able to explain where the differences can and where they cannot be ignores.
   iii. How can you adjust the XOR function to only show differences that are beyond just gate delay differences, and are due to changes on the inputs?