Experiment 1 - Clock and Periodic Signal Generation

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***Abstract*— This is the report of experiment 1 and in this experiment, we have to get familiar with some components and circuits like ring oscillator, Schmitt trigger oscillator, T Flip-Flop, LM555 timer etc. Delay of NOT gates, duty cycle and clock frequency using LM555, frequency of input and output using frequency divider, ring oscillator and T Flip-Flop are the items will be calculated.**

***Keywords*— Ring Oscillator, Schmitt Trigger Oscillator, Frequency Divider, T Flip-Flop, LM555, Clock Signal, Duty Cycle, Digital Logic Gates**

1.1 Ring Oscillator

In this part, Vcc = 5V has been used for a chained odd number of NOT gates. First we confused output and Vcc and we didn't differentiate them.

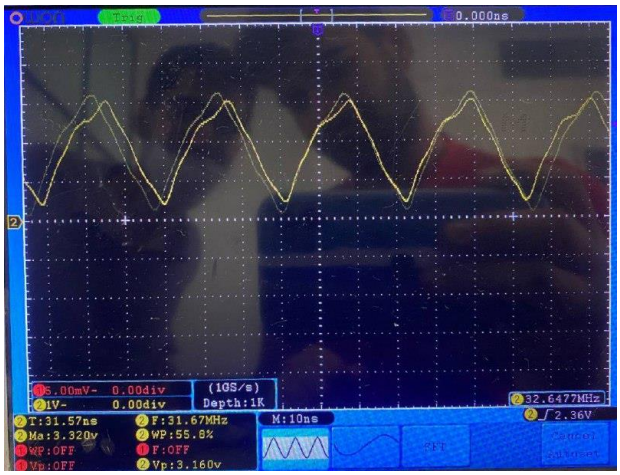

Fig. 1 Output wave of Part 1.1 with Ring Oscillator

1) We observed the wave's frequency equals to 31.67 MHz

$$T = \frac{1}{f} \rightarrow T = \frac{1}{31.67 * 10^6} \rightarrow T \cong 31.58\, ns$$

The propagation delay equals to 31.58 ns.

2) For this part, we use 5 inverters.

$$T = 2N * Delay \rightarrow 31.58 * 10^{-9} = 2 * 5 * Delay$$
$$\rightarrow Delay \cong 3.16\, ns$$

The delay of a single inverter equals to 3.16 ns.

1.2 LM555 Timer

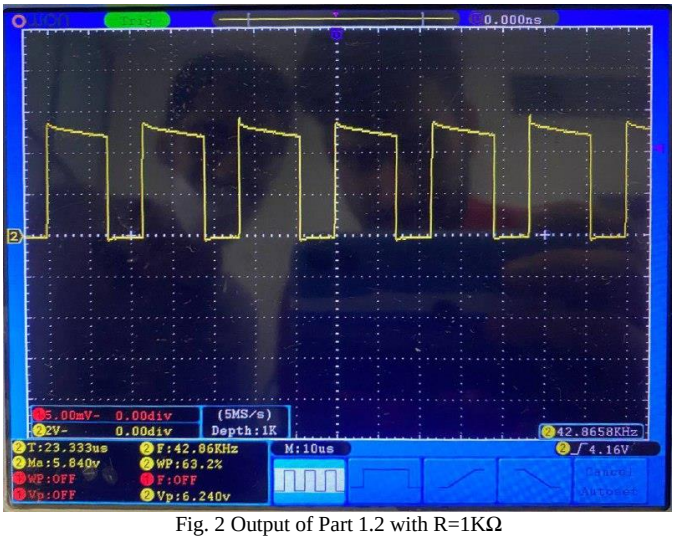

Fig. 2 Output of Part 1.2 with R=1KΩ

Clock frequency = 42.86 KHz

Duty cycle = WP = 63.2%

$$f = \frac{1}{T} = \frac{1}{0.693 * (R1 + 2R2) * C}$$
$$\rightarrow f = \frac{1}{0.693 * (1 + 2 * 1) * 10^3 * 10 * 10^{-9}}$$
$$\rightarrow f \cong 48 * 10^3\, Hz = 48\, KHz$$

$$duty\ cycle = \frac{R1 + R2}{R1 + 2R2}$$
$$\rightarrow duty\ cycle = \frac{1 + 1}{1 + 2} \cong 66\%$$

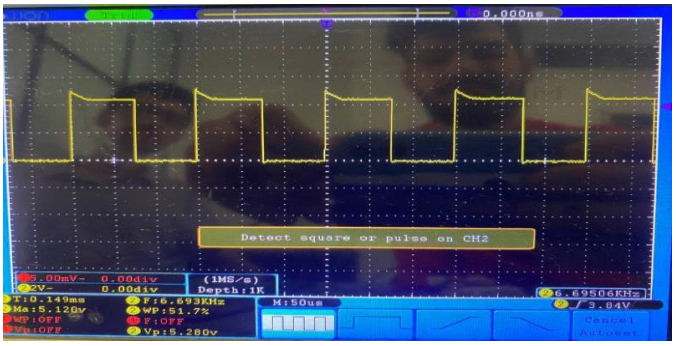

Fig. 3 Output of Part 1.2 with 10 KΩ

Clock frequency = 6.69 KHz

Duty cycle = WP = 51.7%

$$f = \frac{1}{0.693 * (1 + 2 * 10) * 10^3 * 10 * 10^{-9}}$$
$$\rightarrow f \cong 6.87 * 10^3\ Hz = 6.87\ KHz$$

$$\rightarrow duty\ cycle = \frac{1 + 10}{1 + 20} \cong 52.3\%$$

Fig. 4 Output of Part 1.2 with 100 KΩ

Clock frequency = 710 Hz

Duty cycle = WP = 50%

$$f = \frac{1}{0.693 * (1 + 2 * 100) * 10^3 * 10 * 10^{-9}}$$
$$\rightarrow f \cong 717.9\ Hz$$

$$duty\ cycle = \frac{1 + 100}{1 + 200} \cong 50\%$$

We can see that with increasing the amount of R2, the duty cycle gets closer to 50% and the amount of frequency decreases.

1.3 Schmitt Trigger Oscillator

1.4 Synchronous Counter as a Frequency Divider

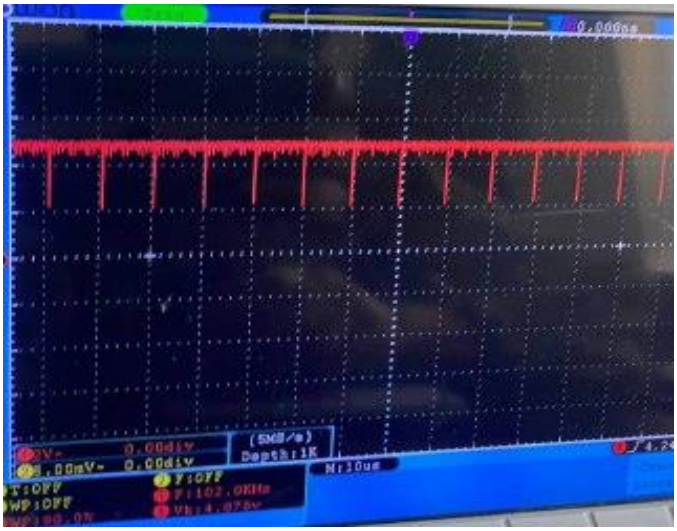

Fig. 5 Carry Out's Wave of MSB

The frequency of output equals to 102 KHz. This means that the input frequency (That was approximately 20 MHz) divided by 200. In this part, the output is approximately 196 times the input. We can calculate initial value by subtracting modulus from maximum value.

$$Initial\ value = 256 - 200 = 56 = (0001\ 1100)_2$$

0001 will be the MSB and 1100 will be the LSB.

1.5 T Flip-Flop

Fig. 6 Wave's Output with Additional T Flip-Flop

By adding T Flip-Flop, the frequency of circuit would be decreased from 102 KHz to 50.51 KHz. That means this component divided the frequency by 2.