

# Experiment 4 - Accelerator and Wrappers

Mohammad Ghareh Hasanloo, 810198461

Danial Saeedi, 810198571

**Abstract**— This is the report of experiment 4 and in this experiment, at first a testbench is implemented for exponential engine functionality. Then exponential accelerator wrapper is added to control handshaking by a controller and an input buffer. At last the accelerator is implemented on FPGA to see output with LEDs.

**Keywords**— Exponential Engine, Exponential Accelerator Wrapper, Accelerator Buffer, Huffman Style, Handshaking

## 1 Exponential Engine

In this part a testbench is written to check functionality of exponential engine. Code and its functionality can be seen below.

```
exponential_TB.v
1 `timescale 1ns/1ns
2
3 module exponential_TB();
4     reg start=0, clk=0, rst=0;
5     reg [15:0] x;
6     wire done;
7     wire [1:0] intpart;
8     wire [15:0] fracpart;
9
10    exponential exp(.x(x), .start(start), .clk(clk),
11    .rst(rst), .done(done), .intpart(intpart), .fracpart(fracpart));
12
13    always #10 clk = ~clk;
14
15    initial begin
16        #20 x = 16'h8000; start = 1;
17        #20 start = 0;
18        while (~done) #20;
19        #20 x = 16'b1000000000000001; start = 1;
20        #20 start = 0;
21        while (~done) #20;
22        #20 x = 16'b1000000000000010; start = 1;
23        #20 start = 0;
24        while (~done) #20;
25        #100 $stop;
26    end
27 endmodule
```

Fig. 1 Testbench

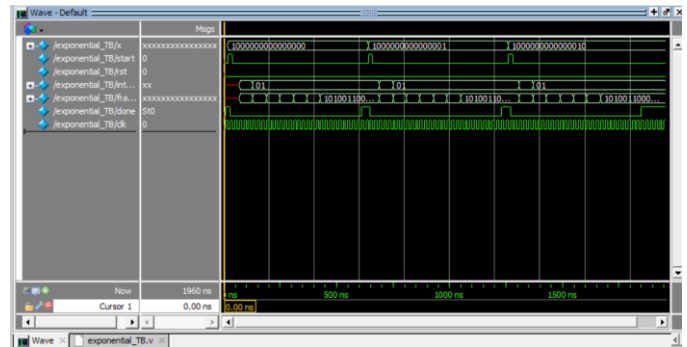


Fig. 2 Testbench Result with Three Inputs

The maximum frequency of this accelerator after synthesizing design is shown below.

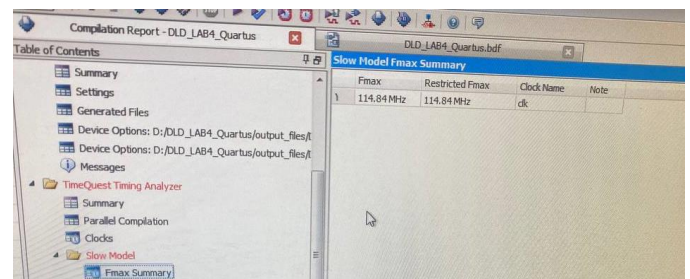


Fig. 3 Maximum Frequency Calculated by Quartus

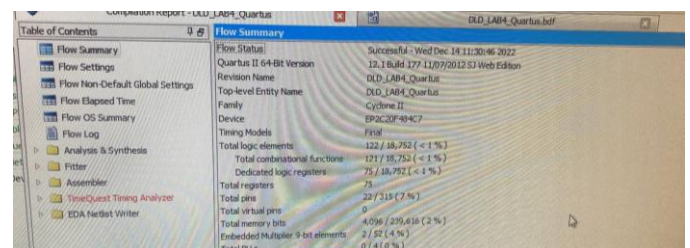


Fig. 4 Synthesis's Result

## 2 Exponential Accelerator Wrapper

This part is designed to accelerator calculates multiple exponential values. CPU saves input values into input buffer and exponential engine uses these values to compute corresponding outputs. In this project, an input buffer is just implemented and the memory element is ROM. A top level wasn't implemented because of Quartus option to make top

level. The input values are stored as mif file inside ROM. The ROM is shown below.

ROM.mif - Notepad

File Edit Format View Help

WIDTH=16;  
DEPTH=256;

ADDRESS\_RADIX=HEX;  
DATA\_RADIX=HEX;

CONTENT BEGIN

00: 8000;  
01: CCCC;  
02: 3333;  
03: FD70;

Fig. 5 ROM Contents

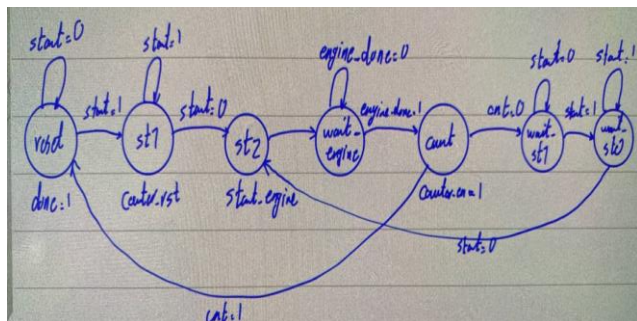


Fig. 6 State Diagram of the Controller

```

1  WrapperController.v
2  WrapperController.v
3  module WrapperController(
4      input start, engDone, clk, rst, incCounter,
5      output reg done, engStart, rstCounter, cnt_en
6  );
7
8      reg [2:0] ps, ns;
9
10     always @(posedge clk, posedge rst) begin
11         if (rst) ps <= 'reset;
12         else ps <= ns;
13     end
14
15     always @(ps, start, engDone, incCounter) begin
16         case (ps)
17             'reset: ns = start ? 'st1 : 'reset;
18             'st1: ns = start ? 'st1 : 'st2;
19             'st2: ns = 'wait_engine;
20             'wait_engine: ns = engDone ? 'count : 'wait_engine;
21             'count: ns = incCounter ? 'reset : 'wait_st1;
22             'wait_st1: ns = start ? 'wait_st2 : 'wait_st1;
23             'wait_st2: ns = start ? 'wait_st2 : 'st2;
24             default:;
25         endcase
26     end
27
28     always @(ps) begin
29         {done, engStart, rstCounter, cnt_en} = 4'b0;
30         case (ps)
31             'reset: done = 1'b1;
32             'st1: rstCounter = 1'b1;
33             'st2: engStart = 1'b1;
34             'wait_engine: ;
35             'count: cnt_en = 1'b1;
36             'wait_st1: ;
37             'wait_st2: ;
38             default:;
39         endcase
40     end
41 endmodule

```

Fig. 7 Wrapper's Controller

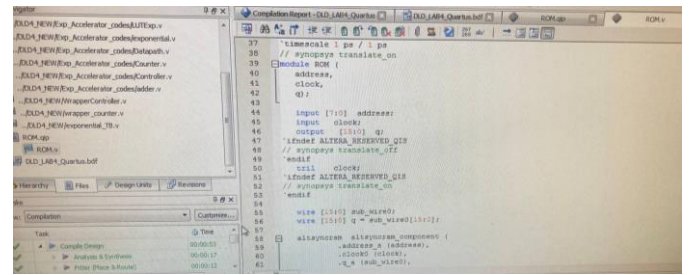


Fig. 8 Instance of ROM IP

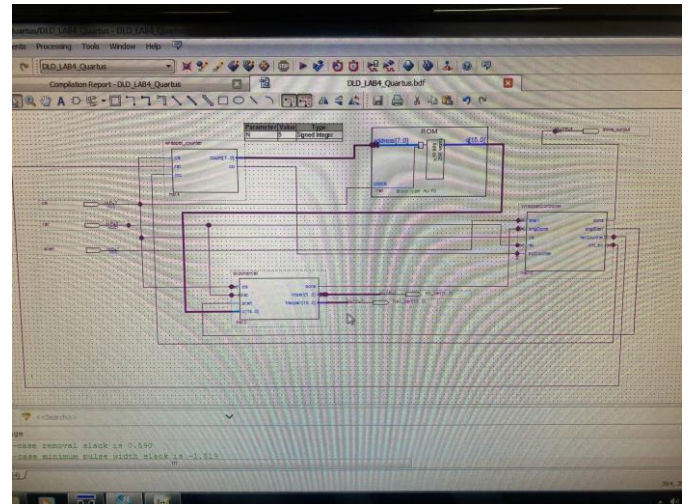


Fig. 9 Block Diagram

### 3 Implementing Accelerator on FPGA

The wrapper is synthesized and implemented on FPGA board and the outputs are shown step by step below. the inputs has been shown in figure 5.

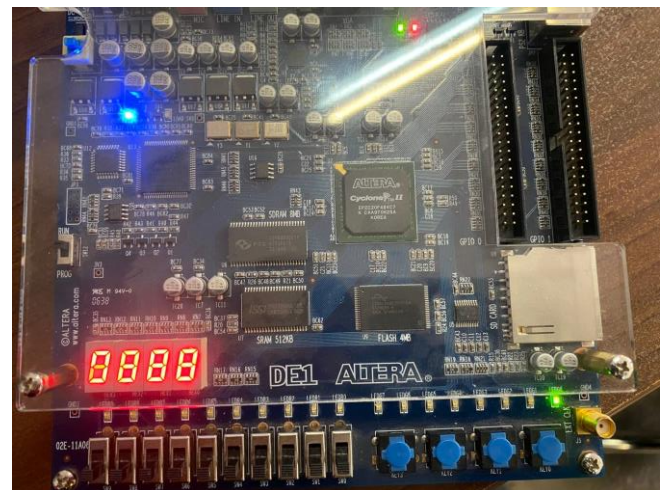


Fig. 10 The Picture before Starting Calculations



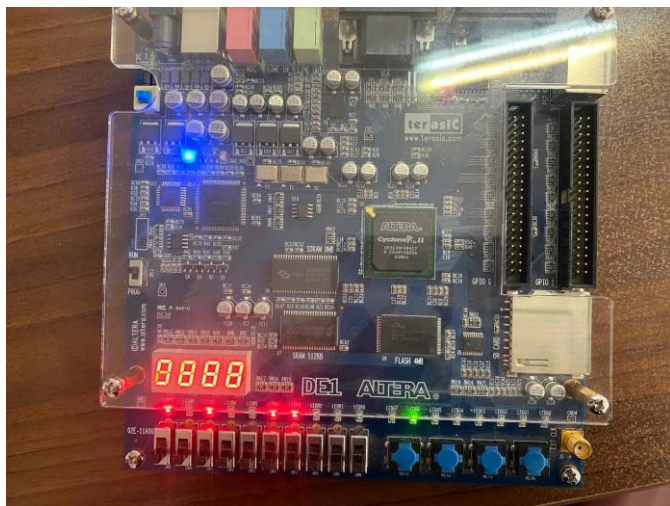


Fig. 11 Output for First Input

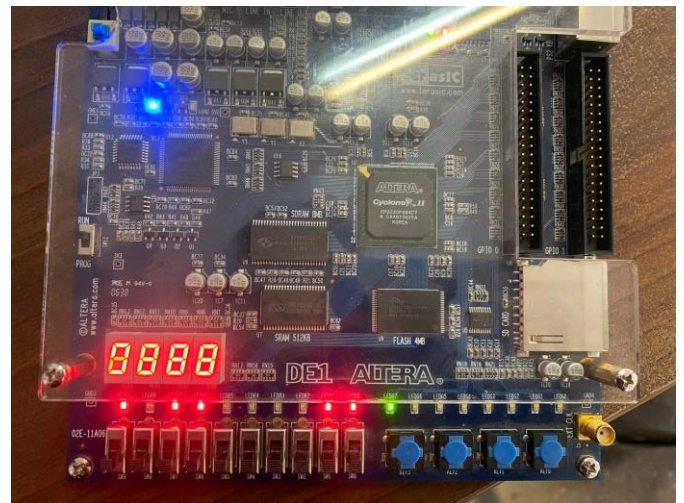


Fig. 14 Output for Forth Input

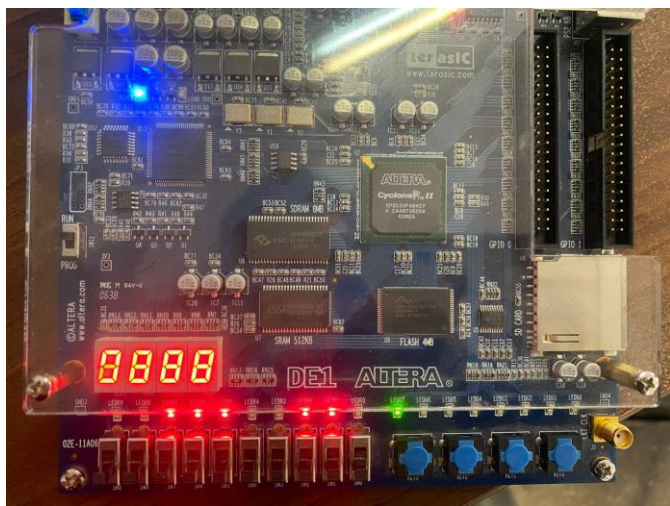


Fig. 12 Output for Second Input

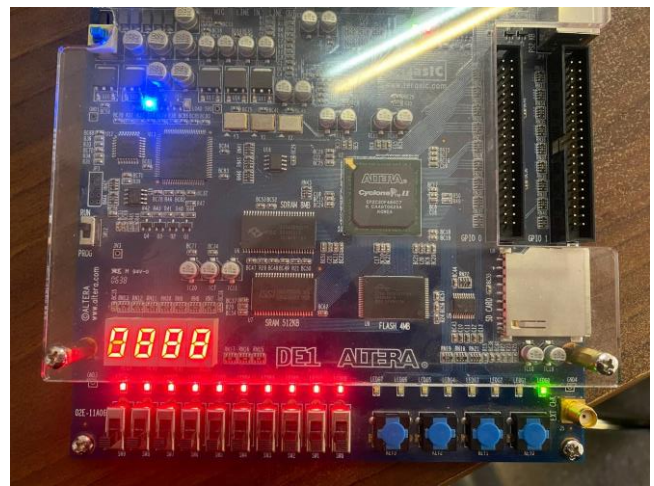


Fig. 15 Board after Finishing Calculations

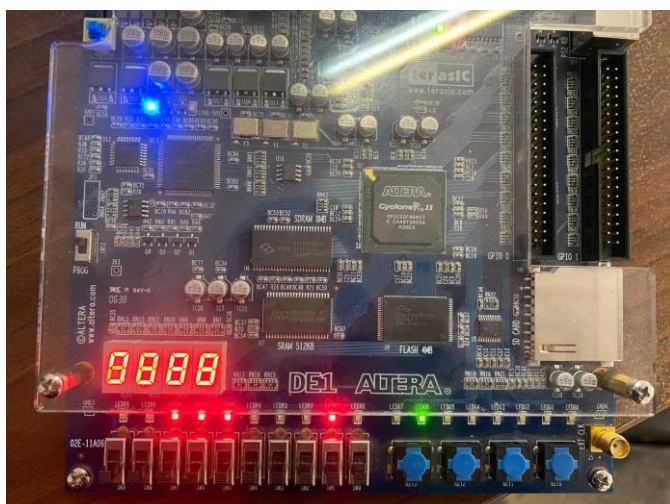


Fig. 13 Output for Third Input

The screenshot displays the LUCAS GUI with two windows open: 'Report' and 'Tasks'.

**Report Window:** The title bar indicates 'Top View - Item Board' and 'Case Name - LUCAS20140427'. The main content is a table with the following columns: Node Name, Direction, Location, I/O Bank, YREF Group, Filter Location, I/O Standard, Reserved, Current Strength, and Differential Pair. The table lists various nodes (e.g., Pac\_P010, Pac\_P011, Pac\_P012) and their associated parameters.

**Tasks Window:** The title bar indicates 'Run Analysis and Elaboration'. The main content is a list of tasks with checkboxes and labels: 'Early Pin Planning', 'Early I/O Planning', 'Run I/O Assignment Analysis', and 'Export I/O Assignments...'. The 'Early Pin Planning' task is currently selected.

Node Name	Direction	Location	I/O Bank	YREF Group	Filter Location	I/O Standard	Reserved	Current Strength	Differential Pair
Pac_P010	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P011	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P012	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P013	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P014	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P015	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P016	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P017	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P018	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P019	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P020	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P021	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P022	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P023	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P024	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P025	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P026	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P027	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P028	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P029	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P030	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P031	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P032	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P033	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P034	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P035	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P036	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P037	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P038	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P039	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P040	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P041	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P042	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P043	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P044	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P045	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P046	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P047	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P048	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P049	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P050	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P051	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P052	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P053	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P054	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P055	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P056	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P057	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P058	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P059	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P060	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P061	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P062	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P063	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P064	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P065	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P066	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P067	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P068	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P069	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P070	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P071	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P072	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P073	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P074	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P075	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P076	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P077	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P078	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P079	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P080	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P081	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P082	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P083	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P084	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P085	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P086	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P087	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P088	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P089	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P090	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P091	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P092	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P093	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P094	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P095	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P096	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P097	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P098	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P099	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P100	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P101	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P102	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P103	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P104	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P105	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P106	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P107	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P108	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P109	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P110	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P111	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P112	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P113	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P114	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P115	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P116	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P117	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P118	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P119	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P120	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P121	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P122	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P123	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P124	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P125	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P126	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P127	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P128	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P129	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P130	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P131	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P132	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P133	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P134	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P135	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P136	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P137	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P138	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P139	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P140	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P141	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P142	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P143	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P144	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P145	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P146	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P147	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P148	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P149	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P150	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P151	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P152	Output	PP_U10	6	PP_U10	PP_U10	3.3V LVTTL (default)		2mA (default)	
Pac_P153	Output	PP_U10							

Fig. 16 Pin Assignments