Savitribai Phule Pune University
Second Year of Computer Engineering (2015 Course)
210246: Digital Electronics Lab

Teaching Scheme:	Credit	Examination Scheme:
PR: 02 Hours/Week	01	TW: 25 Marks PR: 50 Marks

Guidelines for Instructor's Manual

The instructor‘s manual is to be developed as a hands-on resource and reference. The instructor's manual need to include prologue (about University/program/ institute/ department/foreword/ preface etc), University syllabus, conduction & Assessment guidelines, topics under consideration-concept, objectives, outcomes, data sheets of various ICs, 8051 simulator and references.

Guidelines for Student's Lab Journal

The laboratory assignments are to be submitted by student in the form of journal. Journal consists of prologue, Certificate, table of contents, and **handwritten write-up** of each assignment (Title, Objectives, Problem Statement, Outcomes, software & Hardware requirements, Date of Completion, Assessment grade/marks and assessor's sign, Theory- Concept, circuit diagram, pin configuration, conclusion/analysis).

As a conscious effort and little contribution towards Green IT and environment awareness, attaching printed papers as part of write-ups and program listing to journal may be avoided.

Guidelines for Lab /TW Assessment

Continuous assessment of laboratory work is done based on overall performance and lab performance of student. Each lab assignment assessment should assign grade/marks based on parameters with appropriate weightage. Suggested parameters for overall assessment as well as each lab assignment assessment include- timely completion, performance, innovation, efficiency, punctuality and neatness.

Guidelines for Laboratory Conduction

The instructor is expected to frame the assignments by understanding the prerequisites, technological aspects, utility and recent trends related to the topic. The assignment framing policy need to address the average students and inclusive of an element to attract and promote the intelligent students. The instructor may set multiple sets of assignments and distribute among batches of students. It is appreciated if the assignments are based on real world problems/applications. Student should perform at least 14 experiments-5 experiments from group A and 5 assignments from group B, 2 from group C and 2 from group D.

Guidelines for Practical Examination

Both internal and external examiners should jointly set problem statements. During practical assessment, the expert evaluator should give the maximum weightage to the satisfactory implementation of the problem statement. The supplementary and relevant questions may be asked at the time of evaluation to test the student‘s for advanced learning, understanding of the fundamentals, effective and efficient implementation. So encouraging efforts, transparent evaluation and fair approach of the evaluator will not create any uncertainty or doubt in the minds of the students. So adhering to these principles will consummate our team efforts to the promising start of the student's academics.

Suggested List of Laboratory Assignments	
Sr No	**Group A**
1.	Realize Full Adder and Subtractor using a) Basic Gates and b) Universal Gates
2.	Design and implement Code converters-Binary to Gray and BCD to Excess-3
3.	Design of n-bit Carry Save Adder (CSA) and Carry Propagation Adder (CPA). Design and Realization of BCD Adder using 4-bit Binary Adder (IC 7483).
4.	Realization of Boolean Expression for suitable combination logic using MUX 74151 / DMUX 74154
5.	Verify the truth table of one bit and two bit comparators using logic gates and comparator IC
6.	Design & Implement Parity Generator using EX-OR.
	Group B
7.	Flip Flop Conversion: Design and Realization
8.	Design and implement a system using flip-flops, to monitor number of vehicles entering and exiting from a car parking area with maximum capacity of 15 and having separate entry and exit gates.
9.	Design of Ripple Counter using suitable Flip Flops
10.	a. Realization of 3 bit Up/Down Counter using MS JK Flip Flop / D Flip Flop b. Realization of Mod -N counter using (7490 and 74193)
11.	Assume a scenario of a hall where students are entering to attend seminar. Design and implement a system which will increment count if student is entering in the hall and will decrement count if student is exiting the hall. Assume seating capacity of a hall is 63.
12.	Design and Realization of Ring Counter and Johnson Ring counter.
13.	Design and implement Sequence generator using JK flip-flop.
14.	Design and implement pseudo random sequence generator.
15.	Design and implement Sequence detector using JK flip-flop
16.	Design of ASM chart using MUX controller Method.
	Group C
17.	Design and Implementation of Combinational Logic using PLAs.
18.	Design and simulation of - Full adder , Flip flop, MUX using VHDL (Any 2) Use different modeling styles.
19.	Design & simulate asynchronous 3- bit counter using VHDL.
20.	Design and Implementation of Combinational Logic using PALs.
Group D (Study Assignments)	
21.	Study of Shift Registers (SISO,SIPO, PISO,PIPO)
22.	Study of TTL Logic Family: Feature, Characteristics and Comparison with CMOS Family
23.	Study of Microcontroller 8051 : Features, Architecture and Programming Model