Report on 1-D Time-Domain Convolution

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Implementation:

The project was implemented successfully as tested by the provided C++ code in the board.

DRAM_RD implementation:

The block diagram and important signals of our dram_rd IP are shown below:

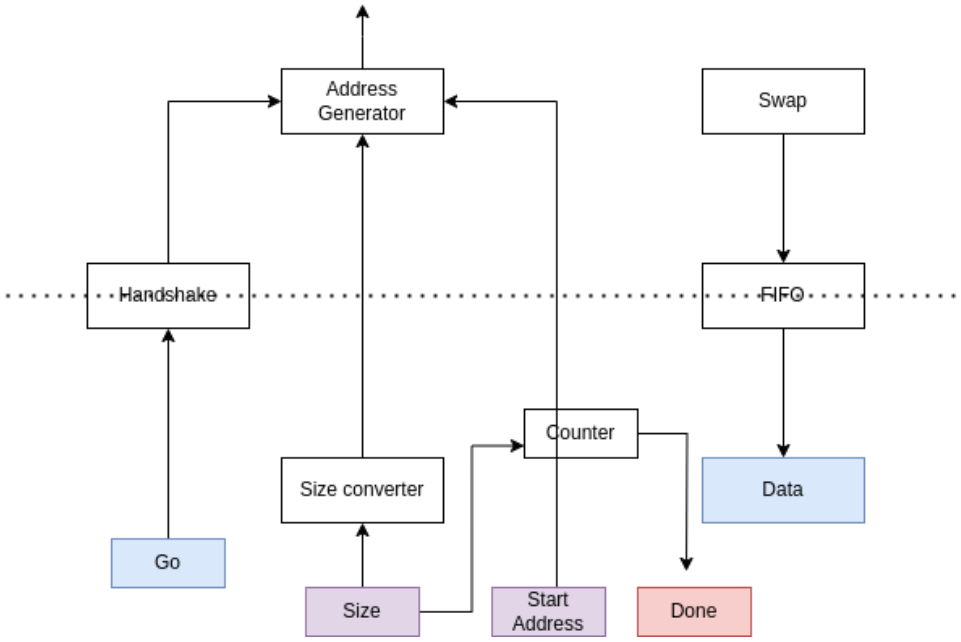


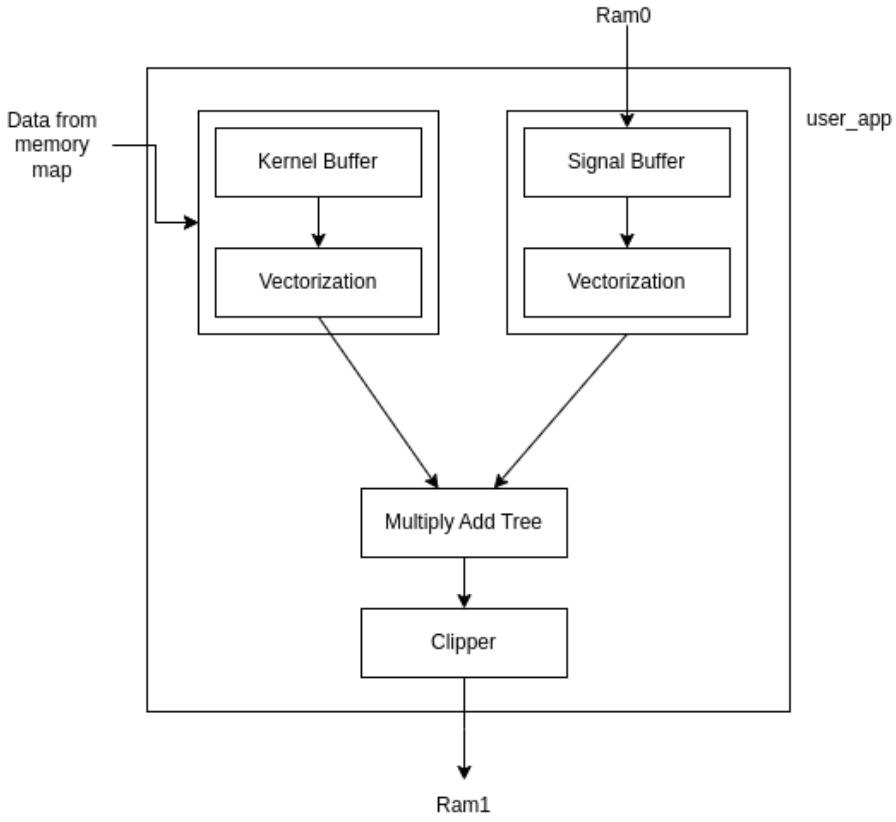
Fig. 1: Block diagram of dram_rd.

Design considerations:

1. Address generator generates address of specified size from a starting address.
2. We designed the address generator using 2 process which made sure the address generator has no latency in producing addresses.
3. A counter generates the done signal which counts the number of times the fifo has been read
4. Input to Fifo was needed to be swapped between upper and lower 16 bits.

Convolve implementation:

The block diagram of our convolve IP is given below:

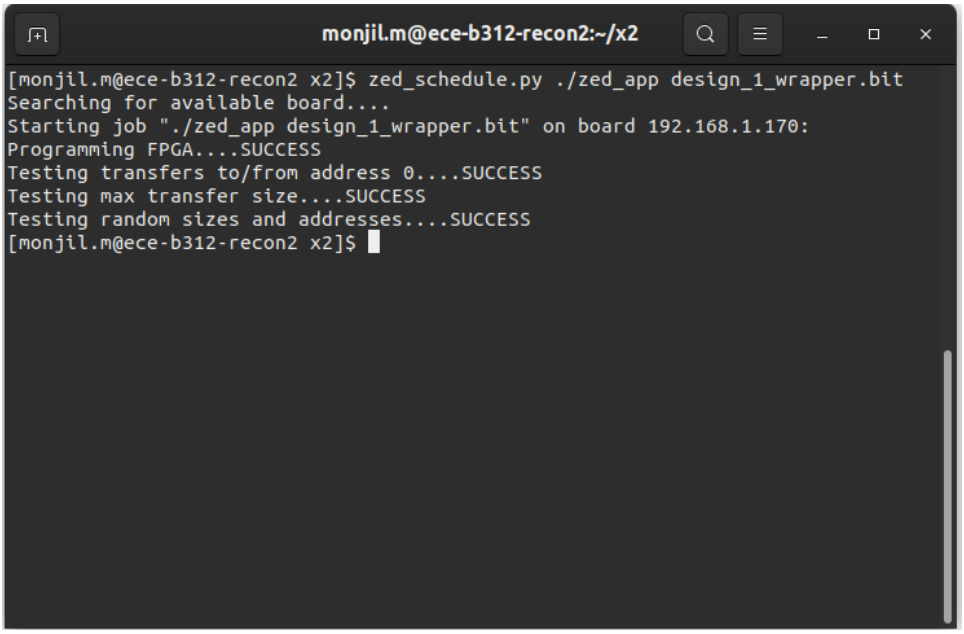


Design considerations:

1. No FSM were required for control.
2. Ram_1_wr_ready was used as the enable signal of the user app.
3. 2 separate entities for kernel and signal buffer was designed. Vectorization was done inside the buffers.
4. Ram_1_wr_done as the done signal for the user_app

Results:

Dram test:



Convolve: