EL 4930 - System-on-Chip Design

Spring 2023

Homework 3

The Lab is a group assignment

Total: 100 points

(Deadline: 03.19.2023, 11.59pm)

Objective:

This homework is the SoC implementation of Homework 1. In this work, you will implement a Hardware software co-design of Pong Game on FPGA. The goal of this lab is to be familiar with the HW/SW partitioning while designing a SoC and the interaction between the HW and SW components.

Tools and Hardwares required:

1. Xilinx Vivado tool is required for this lab.
2. The BASYS 3 board will be used which has an ARTIX 7 FPGA.
3. A VGA cable for connecting with monitor
4. A USB-UART cable to program the board
5. A Monitor with VGA input port

Task Description:

In this task, you will implement the same Pong Game you have designed in Homework 1. The game specification and requirements (paddle position, ball shape, score representation etc.) are same as previous. But, in this design, you must use the Microblaze processor, AXI interconnect, GPIO for push buttons input, VGA controller, and image generator in the HW. You must implement the game controller in the SW using C. The SW part will run on the Microblaze. A high-level block diagram is given below.

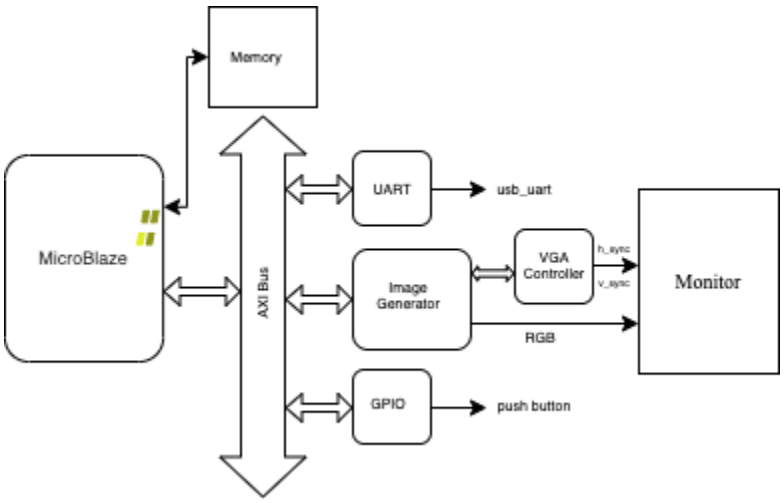

Figure: High level block design of Pong Game SoC

Please feel free to reuse the hardware module HDL codes you used for Homework 1.

Hardware/Software Partitioning:

In your report, please draw a flow diagram of your Pong Game application program showing all the components required for the implementation and clearly show which parts are in hardware and which parts are in software (e.g. identifying HW/SW partitioning).

Submission Guidelines:

1. Include all source code and constraint files.
2. A video demonstration of the Game.
3. A short report describing the block diagram, implementation description, what problems you faced, and what you have learnt.

Grading Rubrics:

Implementation ---- 70%

Video Demo ---- 20%

Report ---- 10%