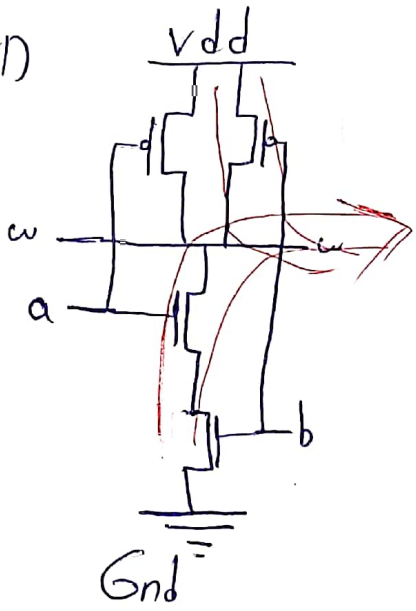
Mohammad Saadati
810198410

DLD
CA 4

46

2) 2 input NAND



#(8,8)

3) Based on the testbench

clk	D	Q^+
1	0	0
1	1	1
0	-	Q

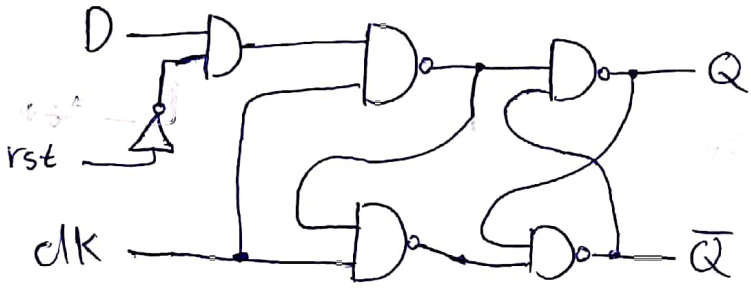
$Q^+ = D$

glitch happend when the input make this transtation for $\bar{Q}$:

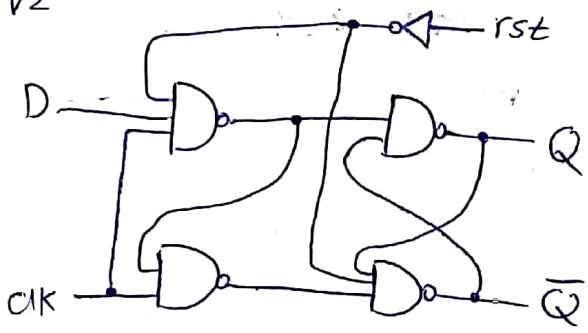
D=1, clk 0 to 1 : 8NS

4- active high reset

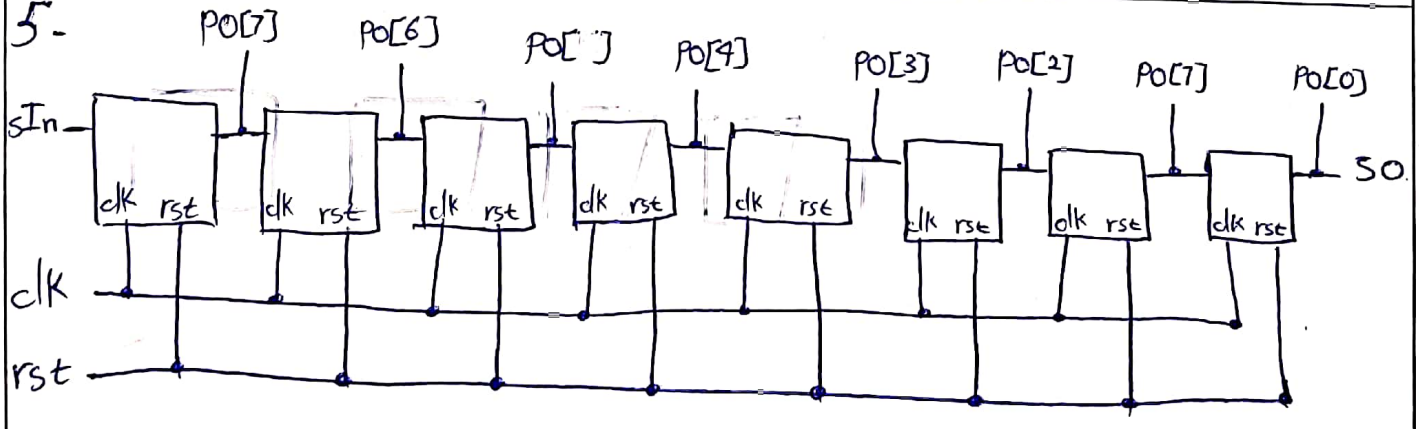
V1



V2

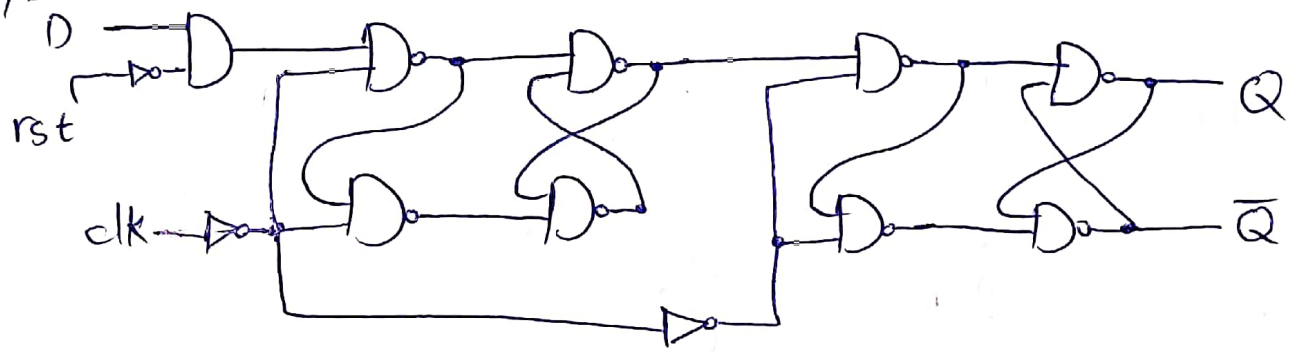


5-

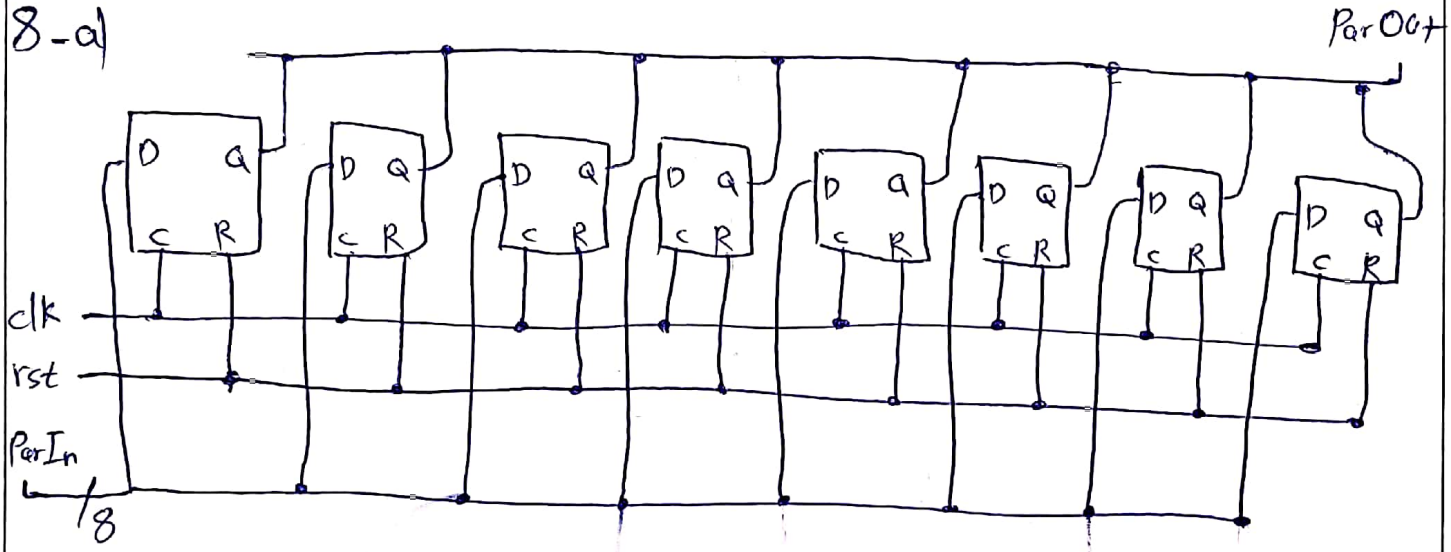


6- The circuit of part 5 doesn't works as expected and the sIn will be shifted to all 8 bit output when we clk to 1 because we use D-Latch in this circuit and D-Latch have transparancy.

7-



8-a)



8-b) like part 5

9- like part 5

10- Less logic block used

When we use always, we consider the worst case delay and we haven't any glitch.