Mohammad Saadati
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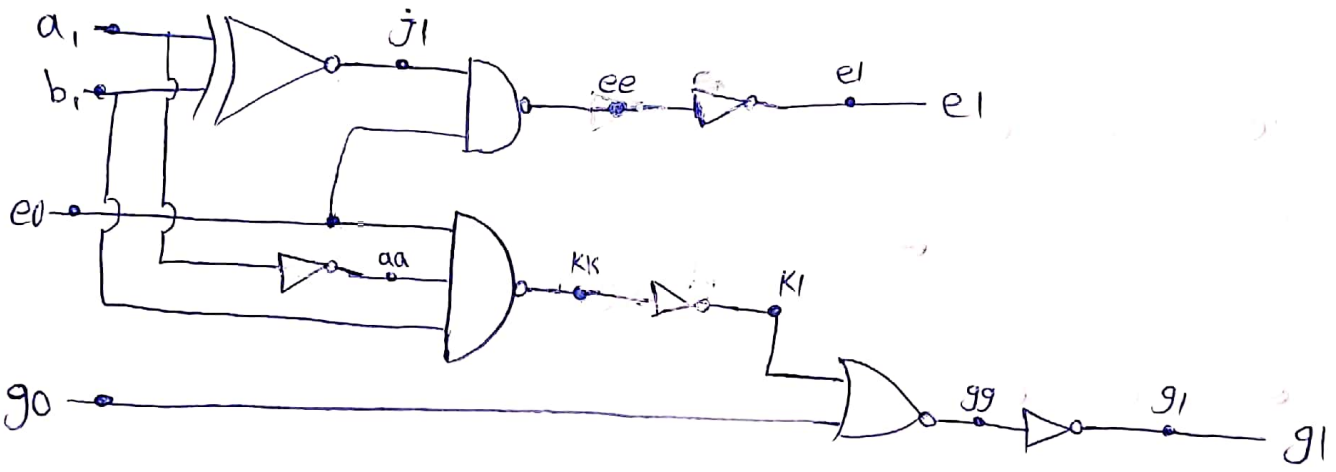
DLD
CA7



$a1=1$, $b1=1$, $e0=1$, $g0=0$ $\Rightarrow$ $e1=1$, $g1=0$, $j1=1$, $k1=0$

$a1=0$, $b1=1$, $e0=1$, $g0=0$ $\Rightarrow$ $e1=0$, $g1=1$, $j1=0$, $k1=1$

2)

Transistor-level BCS output		j1	e1	k1	g1
worst case delay	estimated	(12,10)	(25,27)	(26,25)	(47,40)
	simulation	(12,9)	(24,21)	(17,19)	(36,36)

4)

Gate-level BCS output		j1	e1	k1	g1
worst case delay	estimated	(12,9)	(28,25)	(17,19)	(48,51)
	Simulation	(12,9)	(36,30)	(17,19)	(53,55)