Experiment #2 - Clock Adjusting and Monitoring

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***Abstract*— This document is a student report to experiment #2 of Digital Logic Laboratory course at ECE Department, University of Tehran. In the previous experiment we implemented some clock generation methods such as Ring Oscillator, Schmitt Trigger Oscillator, and etc. The goal of this experiment is to design an adjustable clock generator that can fix the output frequency at a desired value.**

***Keywords*— Clock, Ring Oscillator, Frequency Regulation, Synchronization, Cyclone IV E**

I. Introduction

Synchronization is a crucial issue in sequential digital circuit design. An Overall view of the adjusting system is showed in figure 1. It consists of 3 main units:

1. Clock Adjusting Unit.
2. Clock Monitoring Unit.
3. Noise Eliminator Unit.

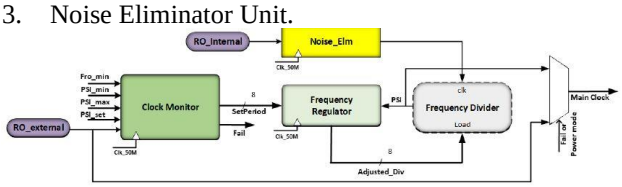


Fig. 1 Overall view of the clock source unit

II. Clock Adjusting Unit

An easy way to comply with the conference paper formatting requirements is to use this document as a template and simply type your text into it.

A. Design and Synthesis

1) *Frequency Regulator :* This section is the main processing unit. It inputs the T flip flop output (PSI) from the clock divider unit (implemented in experiment #1). It counts PSI's high pulse duration (in terms of number clocks). If this counted duration is larger than setPeriod[7:0], it increments the adjustedDiv [7:0] for counters in clock divider by 1 unit so they count less number of units so the duration of high pulse on PSI would become closer to setPeriod[7:0]. If this counted duration is less than setPeriod[7:0], it decrements the adjustedDiv [7:0] for counters in clock divider by 1 unit so they count more number of units so the high pulse duration of PSI would become closer to setPeriod[7:0]. setPeriod[7:0] is the desired high pulse duration of PSI in terms of number of clocks. This unit's clock is the FPGA's clock which we set to be 50MHz. It changes the value (increment or decrement) of adjustedDiv[7:0] when seeing a falling edge on PSI. It starts counting the duration when seeing a rising edge on PSI.

```
always @(posedge rst , posedge clk) begin : decide_when_to_count_and_count
    if (rst == 1)
        count <= 0;
    else begin
        if ({prev , PSI} == 2'b01)
            count <= 0;
        if ({prev , PSI} == 2'b11)
            count <= count + 1;
    end
end

always @(PSI , setPeriod , count , prev) begin : comparsion
    dec_inc = 2'b10;
    if ({prev , PSI} == 2'b10) begin
        if (count < ({8'b00000000, setPeriod} - 1))
            dec_inc = 2'b00;
        else if (count > ({8'b00000000, setPeriod} - 1))
            dec_inc = 2'b11;
    end
end

always @(posedge rst , posedge clk) begin : increment_decrement
    if (rst == 1)
        adjustedDiv <= 8'b01111111;
    else if ({prev , PSI} == 2'b10) begin
        if ((dec_inc == 2'b00))
            adjustedDiv <= adjustedDiv - 1;
        else if ((dec_inc == 2'b11))
            adjustedDiv <= adjustedDiv + 1;
    end
end

always @(posedge clk , posedge rst) begin : transition
    if (rst) prev <= 0;
    else prev <= PSI;
end

endmodule
```

Fig. 2 Verilog description of Frequency Regulator unit

2) *Frequency Divider Unit:* This unit is implemented using two 74193 IC's. They are cascaded and used to build a counter with parallel load inputs coming from the frequency regulator unit. The clock of this unit is 20MHz generated by a ring oscillator. Whenever the counter's reaches 255 (11111111), the carry out of the MSB counter becomes 1 and there is a pulse on the clock of the T Flip Flop, therefore it toggles. Afterwards, the counters start counting from the loaded values.

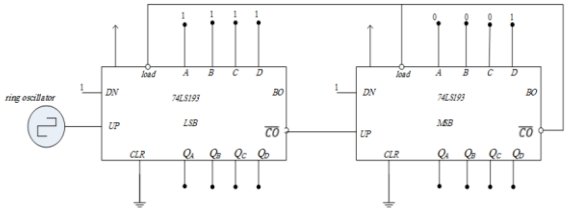


Fig 3. Frequency divider using 74193

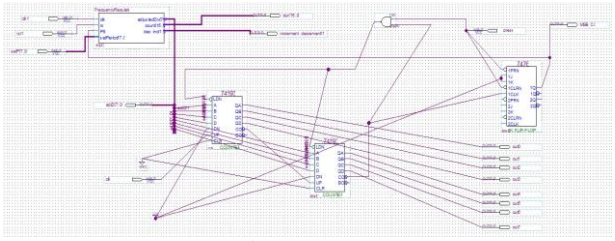


Fig 4. Schematic of Clock Divider unit in Quartus

Analysis & Synthesis Status	Successful - Mon May 03 20:38:18 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	FrequencyRegulator
Top-level Entity Name	FrequencyRegulator
Family	Cyclone IV E
Total logic elements	86
Total combinational functions	85
Dedicated logic registers	25
Total registers	25
Total pins	37
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Fig 5. synthesis results of Frequency Regulator

Analysis & Synthesis Summary	
Analysis & Synthesis Status	Successful - Mon May 03 21:11:40 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	fc2
Top-level Entity Name	fc2
Family	Cyclone IV E
Total logic elements	119
Total combinational functions	118
Dedicated logic registers	34
Total registers	34
Total pins	47
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Fig 6. synthesis results of Frequency Divider Unit

B. Simulation in Modelsim

In the waveforms, the clock generated by the ring oscillator for the clock divider unit is called is named clk_d and the clock used for the frequency regulator unit is named clk_r.

In this scenario set_period [7:0] is set to 125 , initial parallel load is set to 127 and ring oscillator frequency is set to 20 MHz. The adjusted load value finally reaches 205.

Ring Oscillator Frequency	20 MHz.
Desired Frequency	200 kHz
Final Parallel Loads	205
Initial Parallel Loads	127
Setperiod	125

The final Desired Frequency is 200 kHz and it doesn't reaches 400 kHz. The frequency before the TFF is 400 kHz but the frequency after the TFF is 200 kHz. When the output signal comes to the TFF, duty cycle of it become 50% and the signal frequency become 200 kHz so with 127 for initial parallel loads and 125 for setperiod, we can't have 400 kHz frequency after TFF because 255 – 205 = 50 and we need 100 clk that its 0.01 of 20 MHz = 200 kHz.

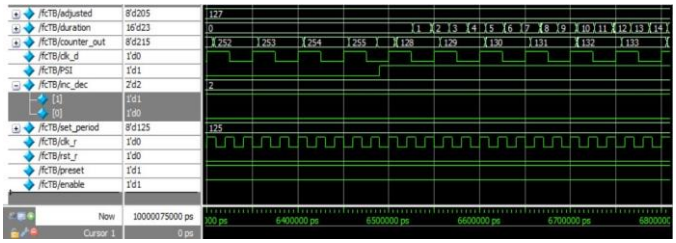


Fig 7. Whenever there is a rising edge on PSI (TFF output), the duration counter starts counting from *adjusted*.

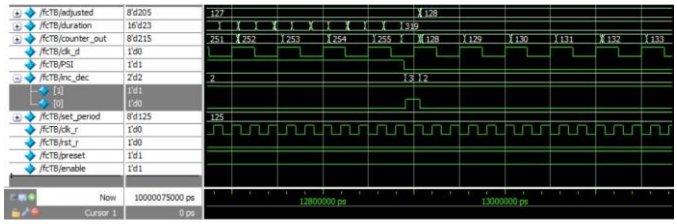


Fig 8. Whenever there is a falling edge on PSI (TFF Out) the value of duration is compared with *set_period*. In this figure 319 > 125 therefore it needs to increment *adjusted*. As you can see an *inc* signal is issued to 1 in this case.

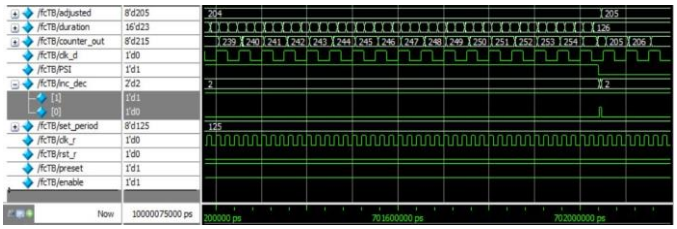


Fig 9. The process in figure 7 is continued until finally the counted duration becomes *set_period*. This happens when parallel load is 205.

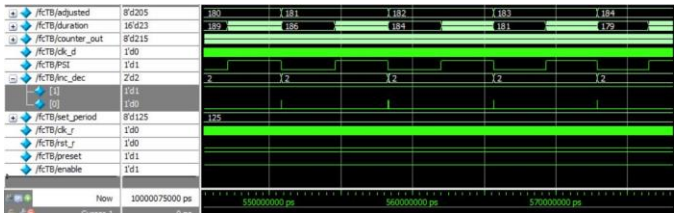


Fig 10. An overall view of the process. *duration* is decreasing until it reaches *set_period*.

III. CLOCK MONITORING UNIT

A. *Design and Synthesis*

```
module ClockMonitoring (clk50,clk_ex,PSI_set,PSI_min,PSI_max,FRO_min,Fail,setPeriod);
    input clk50;
         input clk_ex;
         input [7:0]PSI_set;
         input [7:0]PSI_min;
         input [7:0]PSI_max;
         input [7:0]FRO_min;
         output reg Fail;
         output reg [7:0]setPeriod;
    reg rst , prev;
         reg [15:0]count = 0;

         always @(clk50) begin : transition
        prev <= clk_ex;

    end

    always @(posedge clk_ex) begin
        Fail <= (count > (FRO_min*6)) ? 1 : 0;
        rst <= ({prev,clk_ex} == 2'b01) ? 1 : 0;
    end

         always @(PSI_set , PSI_min , PSI_max) begin
        if ((PSI_set < PSI_max) && (PSI_set > PSI_min))
                        setPeriod <= PSI_set;
        else if (PSI_set < PSI_min)
                        setPeriod <= PSI_min;
        else if (PSI_set > PSI_max)
                        setPeriod <= PSI_max;
    end

    always @(posedge clk50) begin
        if(rst) count <= 0;
        else count <= (count + 1);
    end

endmodule
```

Fig. 11 Verilog description of Clock Monitoring

Analysis & Synthesis Summary	
Analysis & Synthesis Status	Successful - Mon May 03 21:11:40 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	fc2
Top-level Entity Name	fc2
Family	Cyclone IV E
Total logic elements	119
Total combinational functions	118
Dedicated logic registers	34
Total registers	34
Total pins	47
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Fig 12. synthesis results of Clock Monitoring

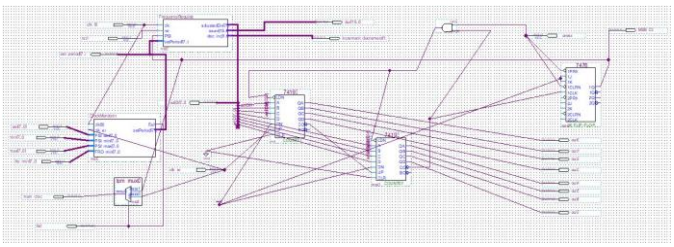


Fig 13. Schematic of Clock Divider unit in Quartus

Flow Status	Successful - Tue May 04 11:37:37 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	fc2
Top-level Entity Name	fc2
Family	Cyclone IV E
Total logic elements	220 / 6,272 (4 %)
Total combinational functions	219 / 6,272 (3 %)
Dedicated logic registers	52 / 6,272 (< 1 %)
Total registers	52
Total pins	81 / 180 (45 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6F17C6
Timing Models	Final

Fig 14. synthesis results of Clock Divider

B. *Simulation in Modelsim*

1) Scenario 1

Internal FRO	24 MHz
Desired Frequency	400 kHz
Final Parallel Loads	226
Final frequency	200 kHz
PSIset	125

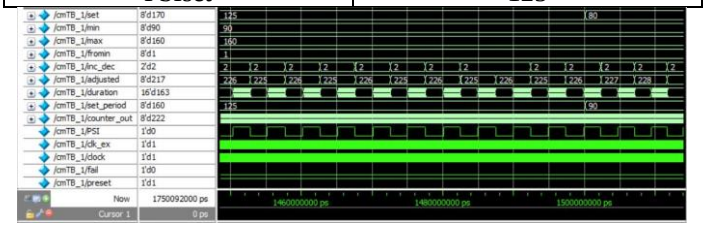


Fig 15. An overall view of the process when *setPeriod* is 125.

Internal FRO	24 MHz
Desired Frequency	400 kHz
Final Parallel Loads	234
Final frequency	200 kHz
PSIset	90

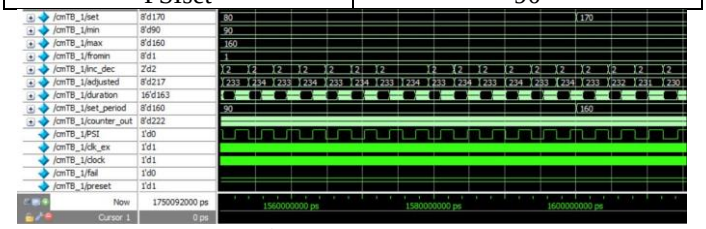


Fig 16. An overall view of the process when *setPeriod* is 90.

Internal FRO	24 MHz
Desired Frequency	400 kHz
Final Parallel Loads	217
Final frequency	200 kHz
PSIset	160

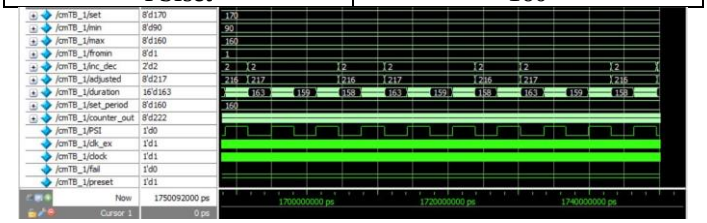
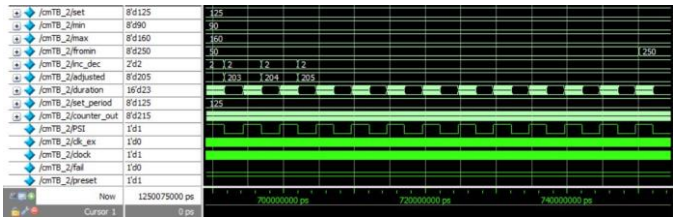
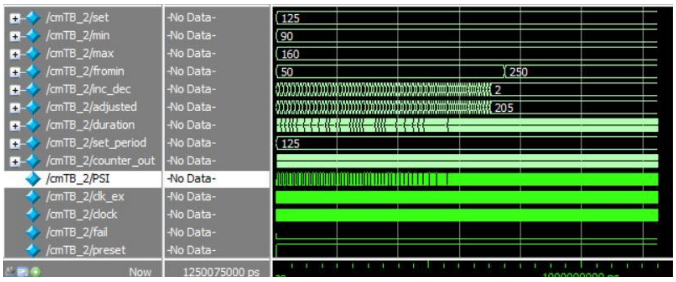


Fig 16. An overall view of the process when *setPeriod* is 160.

2) Scenario 2:





IV. NOISE ELIMINATOR UNIT

A) Design and Synthesis