Mohammad VazirPanah

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Research Interests

Embedded Systems, Cyber-Physical Systems, High Performance Computing, RISC-V Architectures

Education

2018 – 2021 M.Sc. Computer Engineering (Computer Systems Architecture)

Shahid Beheshti University, Tehran, Iran.

Thesis title: A framework for modeling self-aware cyber-physical systems with SystemC.

GPA: 18.43 / 20

Supervisor: Dr. Seyed-Hosein Attarzadeh-Niaki

Advisor: Dr. Armin Salimi Badr

2012 – 2016 **B.Sc. Computer Engineering (Hardware)**

Birjand University, Birjand, Iran.

Project title: Simulation and Programming the Alpha Rex Human-Robot Produced by Lego Company.

GPA: 16.00 / 20

Supervisor: Dr. Mohammad-Hadi Valavi

Work Experiences

2023 – Present Research Fellow | ISISLab laboratory | Supervised by Prof. Biagio Cosenza | University of Salerno, Italy.

2018-2021 **Python Developer Freelancer** | Tehran, Iran.

Teaching | Programming C++, CorelDraw, Free hand and ICDL | Sepehr Educational Institutions | Kashmar, Iran.

2014 **Education Intern** | Abooreyhan Company | Kashmar, Iran.

Research Publications

Journal Articles

S.-H. Attarzadeh-Niaki and M. Vazirpanah, "System-level modeling of dynamic applications with scenario-aware dataflow graphs," *Journal of Innovations in Computer Science and Engineering (JICSE)*, vol. 1, no. 2, pp. 1–13, 2024, ISSN: 2981-2135. ODI: 10.48308/jicse.2024.232987.1023.

Conference Proceedings

- L. Carpentieri, M. VazirPanah, and B. Cosenza, "A performance analysis of autovectorization on rvv risc-v boards," in 2025 33rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP), 2025, pp. 129–136. © DOI: 10.1109/PDP66500.2025.00026.
- M. Vazirpanah, S.-H. Attarzadeh-Niaki, and A. Salimi-Badr, "Ros-based co-simulation for formal cyber-physical robotic system design," in 2022 27th International Computer Conference, Computer Society of Iran (CSICC), 2022, pp. 1–5. DOI: 10.1109/CSICC55295.2022.9780500.

Honors and Awards

- Research Grant: Winner of the national research grant competition among all Master's and Ph.D. students, organized by the R&D Center of the Mobile Telecommunication Company of Iran (MCI).
- Ranked in the top 15% of BSc Computer Engineering students and completed the degree in 7 semesters. Birjand University, Birjand, Iran (2016).

Academic Experiences

Teaching Assistance

- Design and Analysis of Real-Time Embedded Systems | M.Sc. | Shahid Beheshti University | Dr. SH. Attarzadeh-Niaki
 - Advanced Computer Architecture | M.Sc. | Shahid Beheshti University | Dr. SH. Attarzadeh-Niaki
- Fundamentals of Embedded and Real-Time Systems | M.Sc. | Shahid Beheshti University | Dr. SH. Attarzadeh-Niaki
- 2020,2021 System-on-Chip | M.Sc. | Shahid Beheshti University | Dr. SH. Attarzadeh-Niaki
 - 2016 Computer Architecture | B.Sc. | Birjand University | Dr. M. Valavi

Scientific Laboratory Membership

- 2023 Present 📕 Member | ISISLab laboratory | HPC Group | Salerno, Italy
 - 2017 2021 Member | SBU Cyber-Physical Systems Lab Research Team | Tehran, Iran

Conferences Attendance

- 2025 33rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP 2025), Italy, Turin.
- [Presented Paper] 27th International Computer Conference, the Computer Society of Iran (CSICC), Iran, Tehran.

Selected Projects

- 2023-Present
- LibreRT: Portable Heterogeneous Real-time Programming for the Embedded Computing Continuum: It addresses the increasing demand for embedded systems that combine high responsiveness, real-time capabilities, and high computational throughput. The project aims to develop a portable software stack, including programming models, operating systems, and compiler tools, that is capable of running across the entire embedded spectrum, from ultra-low power microcontrollers to high-performance meta-edge platforms equipped with embedded GPUs.
- RISC-V Benchmark Suite: This repository contains a set of benchmarks for RVV on RISC-V and also using programming models: OpenMP, OpenMP-SIMD and SYCL.

Selected Projects (continued)

- A framework for modeling self-aware cyber-physical systems with SystemC [M.Sc. Thesis]: Developed a modeling framework in SystemC (ForSyDe-SystemC) for self-aware cyber-physical systems, enabling simulation and implementation of autonomous, resource-constrained, safety-critical systems. Demonstrated with a robotics path-planning case study using ROS co-simulation.
- FIR Filter on the DEo-Nano-SoC FPGA board: Design an IP Block using Quartus and perform the calculation of the FIR filter using the created block instead of the NiosII Soft processor. Connection of components using an Avalon Memory-Mapped interface and a wrapper to wrap the data.
 - An Audio Control Protocol using Lingua Franca Modeling Language: Implementation of a Distributed Model of this protocol using timed model and verify it using UPPALL.
- Implementation object recognition system using Deep Learning on the DEo-Nano-SoC FPGA board: The design includes an optimal and real-time implementation of the Tiny YOLO1 object recognition system on DEo-Nano-SoC board.
 - Verify and Check Rail Road System Model using NuSMV: Verifying Rail Road system model and check the safety and life requirements.

Skills

HDLs Verilog, VHDL

HVLs SystemC, SystemC-AMS

Simulators Agazebo, Gem5, OVPsim, Qemu

Real Time Operating Systems FreeRTOS

DBMS Microsoft SQL Server, MongoDB

System and Hardware Design Reconfigurable Platforms (FPGAs), RISC-V Architecture

Tools and Libraries Modelsim, Intel Quartus Prime, UPPALL, Proteus, NuSMV, OpenModelica, PSPICE, ROS | roscpp (C++ implementation of ROS), MATLAB-Simulink,

OVP (Open Virtual Platforms), Ansys Scade Suite

Operating Systems Linux, Windows

Typesetting Latex, Microsoft Office

Languages

English | Fluent

Persian Mother Tongue

Italian A2

References

Available on Request.