LAB # 8

Name:_____ Reg#: _____

Aim:

To get better understanding of time shared architecture and working of state machines with FPGA Sparton6 Boards.

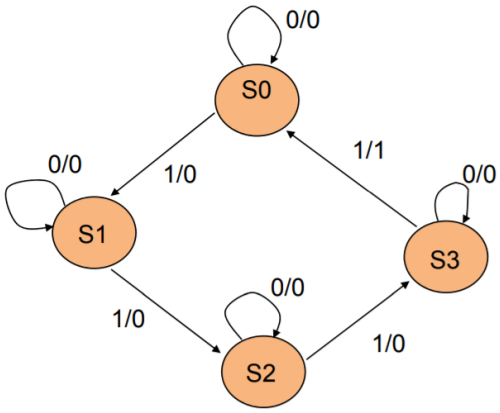
Introduction:

State Machine:

State Machine is a flowchart like graphical notation that describes the cycle by cycle operations of an algorithm and its each step takes one clock cycle. It describes behavior rather than structure and provides a mechanism for performing systematic step-by-step design step design. They can be directly translated to Verilog code and used to design synchronous sequential circuits.

Example:

Generating 1 at the output after counting four number of 1's on a serial interface.



Tasks:

- **TASK 1:**

  Using Spartan6 FPGA board identify the pattern $(1101)_{series}$ and once pattern is identified turn the LED on.

- **TASK 2:**

  Design a time shared architecture using single multiplier and single adder of the following difference equation.
  where $f_{sys}/f_s = 4$.

  □

  $Y[n] = b_o x[n] + b_1 x[n-1] + b_2 x[n-2] + a_1 y[n-1]$