LAB # 7

Name:_____ Reg#: _____

Aim:

Fixed point implementation and RMS error computation.

Introduction:

Let a fixed point format be Qn.m .In case of unsigned number **n=max(number)** whereas in case of signed number **n=max(number)+1.** Maximum and minimum can be find as $(2^{N-1} - 1)$ and (-2^{N-1}) respectively.

In order to read and write a file following commands are used in Verilog.

- Reading a file in Verilog

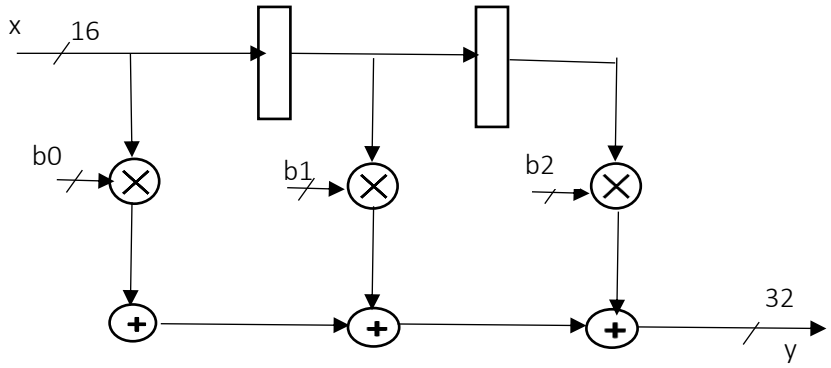
```
reg [<memory_width>] <reg_name> [<memory_depth>];
initial  $readmemb ("<file_name>", <reg_name>, <start_address>, <end_address>);
```

- Writing a file in verilog

```
always@(posedge clk)
$fwrite(<file_desc>, "%d", out);
initial
File_desc =$fopen("filename.txt",w);
```

Tasks:

- **TASK 1:**



1. **Write a MATLAB code for the above diagram using any audio file as input 'x' and compute y.**

2. **Find out the required format Q n.m for intermediate variables, inputs, outputs and coefficients.**

3. **Save input signal in a text file to be read in VERILOG for answer computation**

4. **Write a Verilog code for the above RTL diagram also identify and apply corrections for overflow, underflow and corner case.**

5. **Compare both matlab and Verilog results.**