LAB #4:

INTRODUCTION TO XILINX

Objective:

To introduce students to Xilinx environment and make them comfortable with processes of compilation, synthesis and compilation and to also perform area and frequency.

Introduction:

The figure below shows

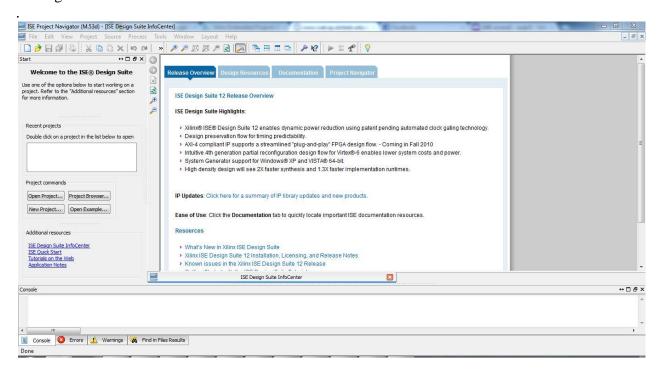


Figure: Main window for the Xilinx environment

Create a project by going to File->New Project

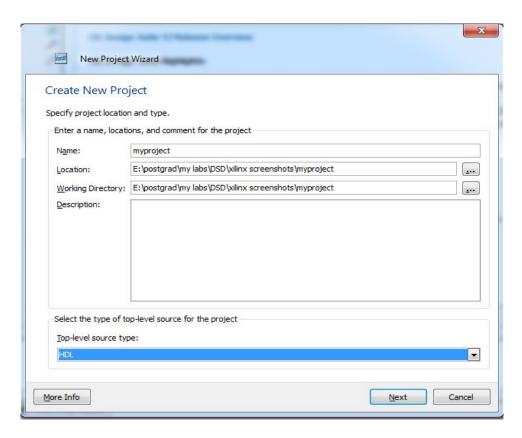


Figure: New Project Wizard

After creating a top level HDL project, use the following settings

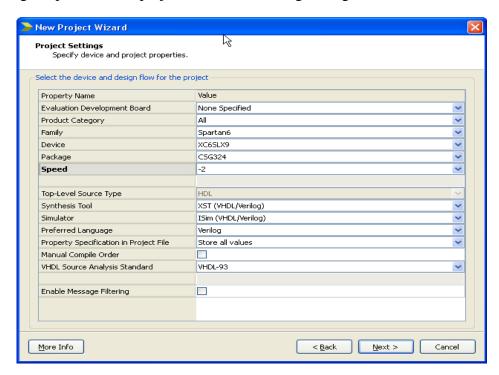


Figure: Project Settings

Create a Verilog module

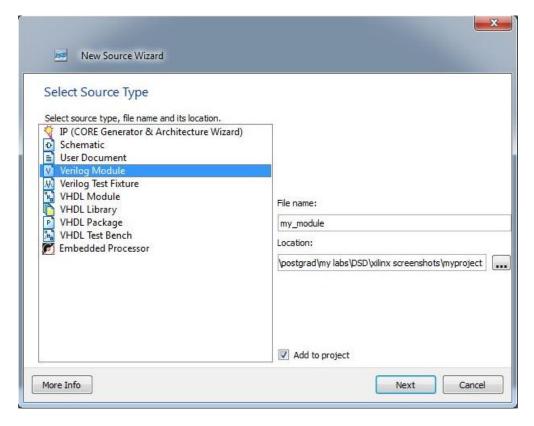


Figure: Verilog Source Type

Populate the port list and write the Verilog code.

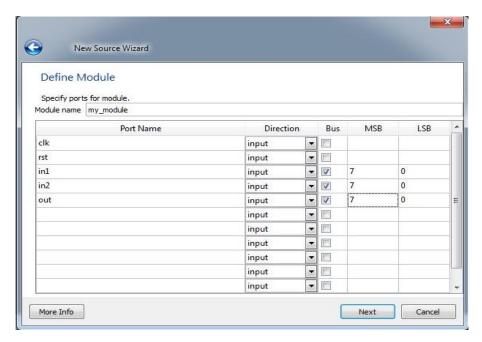


Figure: Defining Input Output

```
Elle Edit View Project Source Process Tools Window Layout Help
↔□♂× a
                                     29 reg [7:0] r0, r1, r2;
View: 

Implementation 

Implementation
                                .
                                     30
   Hierarchy
myproject
c xc3s400-5pq208
                                      31 assign out = r2;
32
00
                                      33 always@(posedge clk or posedge rst)
        my_module (my_module.v)
                                      34 begin
4
                                              if (!rst)
                                      35
                                 4
2
                                      36
                                              begin
                                 %
37
                                                  r0<=0;
                                 %
                                      38
                                                  r1<=0;
                                      39
                                                  r2<=0;
                                      40
No Processes Running
                                      41
                                              else
M
    Processes: my_module
          Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
                                      42
                                              begin
凯
                                                  r0<=in1;
                                      43
K
                                                  r1<=in2;
                                      44
                                                  r2<=r0+r1;
                                      45
                                      46
                                      47 end
          Analyze Design Using ChipScope
                                      48 endmodule
```

Figure: Verilog Code

Once the code is final, check for syntax errors.

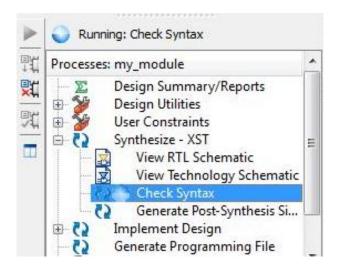


Figure: Check Syntax Error

After successfully checking the syntax and removing the errors create a testbench/stimulus for Verilog module as follows.

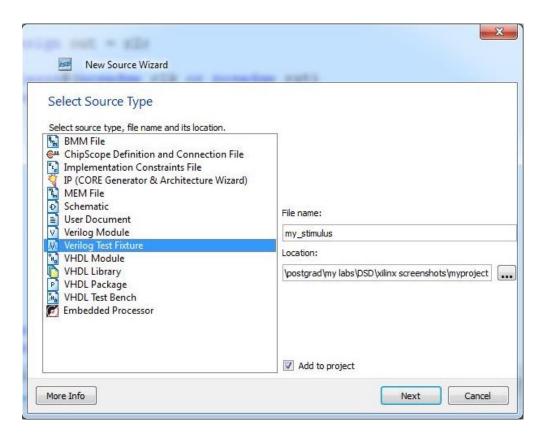
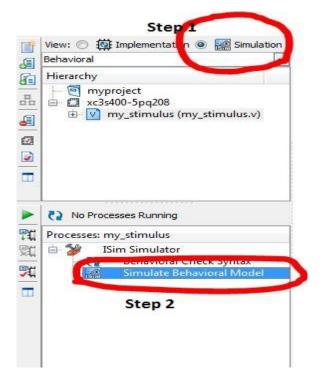


Figure: Verilog Test Bench

Write the stimulus code for testing the module, also generate a clock and simulate by following steps 1 and 2 as shown in the figure below.



ISim of Xilinx is just like the simulation in ModelSim, the result is shown below.



Figure: Simulation Results

Xilinx provides another advantage that it is capable of allowing its users to generate the RTL schematics for the Verilog code as shown below.

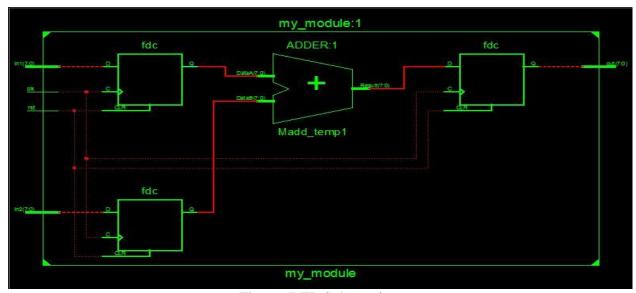


Figure: RTL Schematics

Related Topic/Chapter in theory class:

None

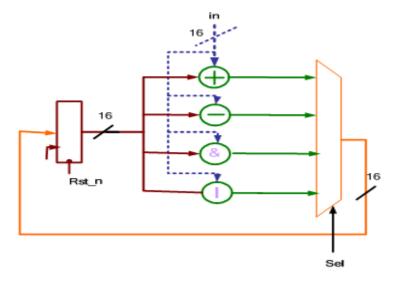
Hardware/Software required:

Hardware: PC

Software Tool: Xilinx /Modelsim

Task:

Use Xilinx to generate the Synthesis Report and RTL diagram for the following diagram.



Conclusion:

In this lab students make themselves comfortable with the Xilinx environment and learn how to use certain functions of Xilinx.