October 12, 2017

Lab # 3

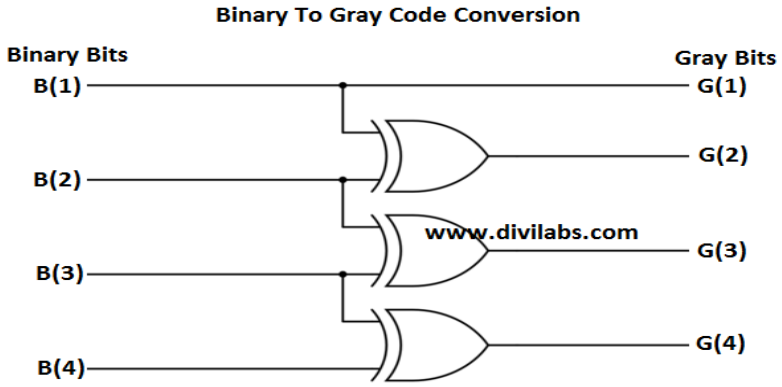
Name: _____ **Reg #:** _____

Aim:

To understand and practice VERILOG syntax and simulation process.

Tasks:

i. Implement the given Logic for binary to grey codes generation (logical circuit which converts binary code to equivalent grey code). Write stimulus to verify the working of your logic.



ii. Draw RTL diagram of the following difference equation, write its RTL VERILOG code. Test your design for all values of x. (Assume input as 4 bit whereas output as 8 bit)

$$y[n] = 2 * x[n] + 3 * x[n-1] + 2 * x[n-2] + 5 * x[n-3] + 6 * x[n-4]$$

iii. Design and implement a HEX counter using RTL VERILOG. Write stimulus to test your code.

iv. **DESIGN QUESTION:**

You are required to design a system which counts the number of cycles required by the system until all (3 i.e. x, y, z) inputs of the system become equal. The system has 3 N bit wide inputs and a single M bit wide output which shows the number of cycles required by the system. The inputs must be stored in the registers before start of the process.