Digital System Design

Question 1:

You are required to design a custom processor which performs the process of correlation on two input signals specifying whether the given signals match each other or not. The system calls a **"display"** function stating the correlation result of the signals **in case the result exceeds a threshold specified by the user.** Length **(N)** of the input signal and the threshold value is specified by the user in the form of an instruction. Correlation is performed via the following expression:

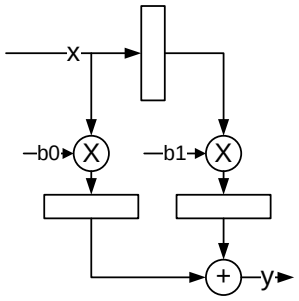
$$Correlation\ Result = \sum_{i=0}^{N-1} x(i) * y(i)$$

a. Specify a valid instruction set for the specified system.
b. Specify instruction format for the specified instruction set.
c. Specify Datapath and Controller for the specified instruction set and instruction format.

Hint: Assume data to be already loaded into 2 RAMS (x and y) of depth N

Question 2:

a. Transform the following RTL diagram such that it uses **only a single Carry Ripple Adder using Compression Trees**. Design should not contain any multiplier in it.
b. Compute correction vector for individual multipliers; also specify a global correction vector.
   - **Assume x to be 8 bit wide and b0 = 8'h36 & b1 = 8'h5D having $Q_{1.7}$ format.**



Question 3:

Given the equation $y = a * b - c + d >> 2 + e * f + g;$

Number	Format
a	Q1.2
b	Q3.0
c	Q0.4
d	Q2.3
e	Q0.4
f	Q1.2
g	Q2.2

Apply **Wallace** Reduction Scheme to compress the said expression such that only 2 rows of numbers are left.

Specify format of y.

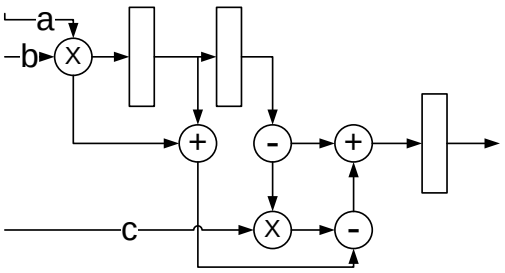
Question 4:

a. Compute A – B using Conditional Sum Adder assuming cin as '1'
b. Compute A + B using Carry Select Adder (4 bit group)

$$A = 10011011$$
$$B = 01100101$$

Question 5:

a. Identify the critical path and its delay in the following system **if multiplier takes 6 time unit, adder takes 2 time unit and subtractor takes 2.5 time unit.**
b. Minimize the critical path of the system using algorithmic registers (i.e. registers already available in the design) provided in the design.
    a. Restate the critical path



Question 6:

Design a mirco coded state machine based design to support the following instructions

if condition_i === TRUE call subroutine function1 N times
else If condition_i == FALSE call subroutine funtion2 M times

condition_i could be COND0, COND1, …, COND7

M, and N are two 3 bit numbers and program memory is 512 instructions wide.
Draw a detailed diagram showing all the control signals.

Question 7:

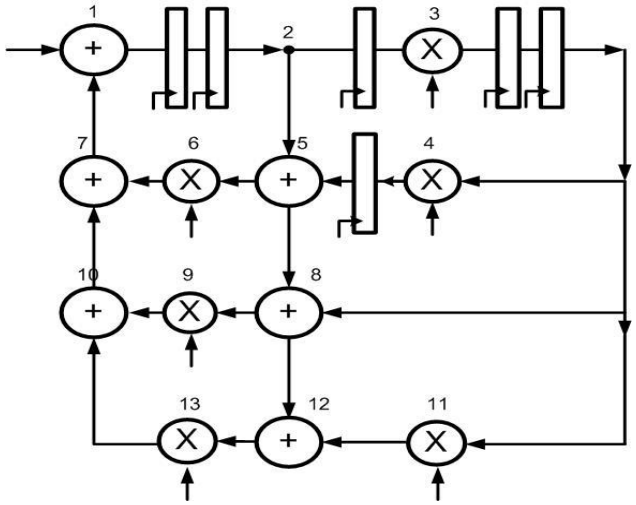
Design and write code in RTL Verilog for a 4-bit 3 entry circular queue. The input value is circularly added in the queue and outputs are circularly read from the queue. No error checking is required, so you may overwrite an unread value or read an already read value. Write stimulus for your design. Give output of the system for the following test vectors.

Write 2
Write 3
Read
Write 4
Write 5
Write 1
Write 0
Read

Read
Read
Read

Question 8:

Find the critical path of the given system.
Minimize the critical path using node transformation theorem using the registers already present in the design



Question 9:

Design a string matcher for a byte interface. The design takes an 8 character reference string (64-bit) as input. On the byte interface, the design gets a byte of data at every *posedge* of clock. The design generates a 1 at the output if string is matched with the input reference string. Draw RTL diagram of the design and write RTL Verilog code of its implementation. Also write stimulus to test the working of your design. (Copy your code on a separate sheet for take home exam. Take your time to code and simulate YOUR CODED design using any Verilog simulator and demonstrate your implementation with the Semester project.)

Question 10:

Compute correction vector for sign extension elimination while computing A+B-C using a compression tree where A, B and C are three signed numbers in Q1.7, Q7.1 and Q3.2 format respectively.

Question 11:

Design a **micro-program memory** based controller for traffic signal in a crossing where a minor road with seldom traffic crosses a main highway. The controller checks if there are no cars on the minor road, it keeps green light on the main road ON. In case it detects a car on the minor road, it switches the lights on the main road to red and minor road to green for 20 seconds and then turns the lights back again.

Question 12:

Draw an 8-bit Conditional Sum Adder architecture to compute the expression

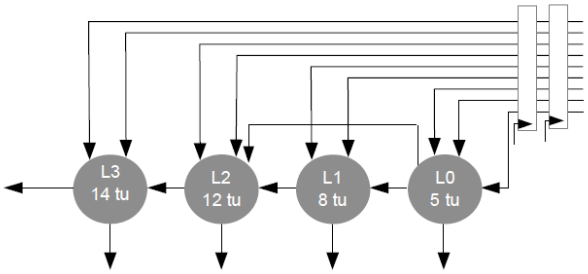
$$if\,(A - B)$$

Show the working of Conditional Sum Adder architecture on the following numbers:

$$A = 1001\_1101$$
$$B = 1101\_1011$$

Question 13:

Use the two registers given at the input to break the critical path to achieve minimum possible delay, Each node shows the combinational time delay of that node.



Question 14:

Draw time shared architecture for the following using a single adder and a single multiplier.