LAB # 6

Name:_____ **Reg#:** _____

Aim:

To understand how to generate a slow clock using a counter and to get familiar with the working of FPGA Boards.

Introduction:

Example:

Assume an FPGA board having an oscillator of 50 MHz, we want generate a clock that toggles after every 1 second (time period of 2 secs). This means:

- 1 sec is equal to 50 M clock cycles
- 1 clock cycle is equal to (1/50 M) secs

In other words, we will use a counter that counts till 50M, at 50 M it toggles a register from 1 to 0 and vice versa. This counter can be used as a delay function or for generation of a new slow clock.

Tasks:

- ## TASK 1:

Using Spartan 6 FPGA Board, program a counter that displays the numbers on the 7 segment display after every increment.