Digital System Design
Assignment 5

Question 1:

Exercise question 9.4

Question 2:

a. **You are required** to design a controller for a system that actuates on the input provided by a 1-bit sensor. The system actuates (gives O/P as 1) when it detects two consecutive ones followed by a zero which are then followed by consecutive one and zero.
b. Give output and state transition of your state machine for the following input stream gathered from the sensor.

1011001011

Question 3 (practice question, not to be submitted as part of assignment):

Exercise question 9.6

Question 4:

You are required to design a basic level controller for a semi-automatic vehicle using state machine based design. Following are the basic characteristics of the controller:

- User can specify if manual or automatic transition of gears is allowed via a one bit input signal "A_M" (A_M = 0 for manual and A_M = 1 for automatic).
- System (controller) only works if user has specified A_M as 1.
- System can work in two modes, normal or boast. User specifies this via 1 bit input signal "N_B" (N_B = 0 for normal, N_B = 1 for boast).
- Controller should provide two signals for gear up and gear down on the bases of input signals and speed of the vehicle.
- The following speed and gear relation is followed if automatic is selected by the user.

Mode	Speed	Gear
Normal	0-20	1st
-do-	20-45	2nd
-do-	45-70	3rd
-do-	>70-	4th

Mode	Speed	Gear
Boast	0-30	1st
-do-	30-55	2nd
-do-	55-80	3rd
-do-	>80-	4th

On the bases of vehicle speed gear is either shifted up or down

Question 5:

Design a state machine to implement a Medium Access Control (MAC) Protocol for a wireless communication network. Draw a bubble diagram to show your design. The protocol should implement the following:

a) Any node to transmit first checks that no other node in its range is transmitting.
b) If the node detects any transmission, it waits for the transmission to end.
c) The node then sends a *req* to the destination node and then waits for the *ack* from the destination node.
d) If the node does not receive any *ack*, then it waits for 10 ms and if there is no other transmission in its range, sends the *req* again and keeps repeating this sequence three times before dropping the current transmission to the destination with a message destination is not in range.
e) In case the destination sends an *ack*, the node transmits a packet of data to the destination and then waits for the *ack_packet* from the destination node. After receiving *ack_pack* it silently receives any transmission meant for the node or let other nodes in the network to transmit.

After transmitting one packet if the node needs to transmit any other packet, it waits for 60 ms and only then serves the request of transmission of a new packet of data in the network.

Question 6:

Design and write code in RTL Verilog for a 4-bit 3 entry circular queue. The input value is circularly added in the queue and outputs are circularly read from the queue. No error checking is required, so you may overwrite an unread value or read an already read value. Write stimulus for your design. Give output of the system for the following test vectors.

Write 2
Write 3
Read
Write 4
Write 5
Write 1
Write 0
Read
Read
Read
Read

Question 7:

Design a state machine based centralized controller, for the system shown below. Node C represents some combinational logic whereas Nodes A, B D and E represent sequential logic. Node D and E require 4 and 5 clock cycles respectively to complete their task (generate output i.e.). Node A waits for 3 input samples before starting its processing and it generates an output

after 4 cycles (after receiving data). Furthermore Node B has variable complete time i.e. it may require 3-10 clock cycles depending upon its input. Your aim is to provide an FSM that controls the flow of this system, SHOW ALL the signals and their respective values.