7 Matching of Resistors and Capacitors

Most integrated resistors and capacitors have tolerances of ±20 to 30%. These tolerances are much poorer than those of comparable discrete devices, but this does not prevent integrated circuits from achieving a high degree of precision matching. All of the devices in an integrated circuit occupy the same piece of silicon, so they all experience similar manufacturing conditions. If one component's value increases by 10%, then all similar components experience similar increases. The ratio between two similar components on the same integrated circuit can be controlled to better than ±1%, and in many cases, to better than ±0.1%. Devices specifically constructed to obtain a known, constant ratio are called *matched devices*.

Analog integrated circuits usually depend on matching to obtain much of their precision and performance. Any number of mechanisms can interfere with matching. Most of these mechanisms are known, and layout designers have devised ways to minimize their impact. This chapter covers the design of matched resistors and capacitors. Much of this information also applies to matching of other components, such as bipolar transistors (Section 9.2), diodes (Section 10.3), and MOS transistors (Section 12.4).

7.1 MEASURING MISMATCH

The *mismatch* between two components is usually expressed as a deviation of the measured device ratio from the intended device ratio. Suppose a designer lays out a pair of matched 10kΩ resistors. After fabrication, one pair of these resistors are found to equal 12.47kΩ and 12.34kΩ. The ratio between these resistors equals 1.0105, or approximately 1% more than the intended ratio of 1.0000. This pair of resistors therefore exhibits a mismatch of approximately 1%.

The concept of mismatch also applies to devices having ratios other than 1:1. The mismatch between any two devices equals the difference between the ratio of their measured values and the ratio of their intended values, divided by the ratio of their intended values. The final step, division by the ratio of intended values, normalizes

the result so that it becomes independent of ratio. If the intended values are X_1 and X_2 and the measured values are x_1 and x_2, then the mismatch δ equals

$$\delta = \frac{(x_2/x_1)-(X_2/X_1)}{(X_2/X_1)} = \frac{X_1x_2}{X_2x_1}-1 \qquad [7.1]$$

Equation 7.1 computes the mismatch of one specific pair of devices. The same measurements performed on a second pair of devices will yield a different mismatch. Measurements of a large number of device pairs will produce a random distribution of mismatches. An analysis of the mismatch distribution of a small sample of devices allows the designer to determine the percentages of units that are likely to fail specifications. In order for this analysis to yield valid results, the sample must fairly represent the capabilities of the process. Ideally, the sample should consist of 50 to 100 devices drawn from random locations on at least ten wafers that are drawn randomly from at least three wafer lots. In practice, one must often rely on a sample drawn from a single wafer lot. When selecting this sample, consider the following guidelines:

- The sample should include no fewer than twenty devices.
- The sample should include devices drawn from at least three wafers. Each wafer should contribute approximately the same number of devices to the sample.
- The wafers should be selected from various positions in the wafer lot. A three-wafer sample should include one wafer from the front of the lot, one from the middle, and one from the back.
- The sample devices should be selected from random locations on each wafer.
- If possible, the sample should include wafers from more than one wafer lot.
- Wafers that have been misprocessed or reworked do not fairly represent the process and should not be used for characterization.
- If at all possible, the sample units should be packaged using the same lead frames and encapsulation as production material.

Once a sample has been selected and all of the sample units have been measured, the resulting data must be statistically analyzed. The theory of such analyses is beyond the scope of this text,[1] but the simplified procedure given below provides a good example of the techniques and terminology involved.

Suppose the sample includes N units, the mismatches of which are $\delta_1, \delta_2, \delta_3 \ldots \delta_N$, as computed by equation 7.1. Mismatches can be either negative or positive quantities. The signs of these mismatches are significant and must be retained in order for the following computations to have meaning. Based on the computed mismatches, one can derive an average mismatch m_δ. This average, or *mean*, consists of the sum of all the mismatches divided by the number of sample units N

$$m_\delta = \frac{1}{N}\sum_{i=1}^{N}\delta_i \qquad [7.2]$$

where the sigma function $\Sigma(\,)$ represents the sum of all of the individual terms. Once the mean has been computed, one can determine the *standard deviation of the mismatches* s_δ:

$$s_\delta = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_i - m_\delta)^2} \qquad [7.3]$$

[1] Any good statistical text will cover this subject in some detail. A discussion of the propagation of error and its measurement is contained in J. Mandel, *The Statistical Analysis of Experimental Data* (New York: Dover, 1984).

The mean m_δ is a measure of the *systematic mismatch,* or ***bias,*** between the matched devices. Systematic mismatches are caused by mechanisms that influence all of the samples in the same manner. Consider the case of a pair of matched 2kΩ and 4kΩ base resistors laid out as single strips of base diffusion with contacts at either end. Both of these resistors have the same contact resistance, which will be assumed to equal 100Ω. This contact resistance causes a 5% increase in the 2kΩ resistor, but only a 2.5% increase in the 4kΩ resistor. Every pair of resistors shows the same imbalance, so the contact resistance represents a systematic mismatch. This mismatch could be eliminated by dividing both resistors into segments of 2kΩ. The 2kΩ resistor would contain one segment with 100Ω of contact resistance, which produces a 5% increase in its value. The 4kΩ resistor would contain two segments with a total of 200Ω of contact resistance, which produces a 5% increase in value. Since both segmented resistors experience the same percentage increase in value, they do not exhibit any systematic mismatch.

The standard deviation quantifies *random mismatch* caused by statistical fluctuations in processing conditions or material properties. These fluctuations are an unavoidable part of semiconductor manufacture, but their magnitude can sometimes be reduced if one can identify their underlying causes. Figure 7.1 shows a histogram of the mismatches of 30 units. The exact appearance of the histogram will change as additional units are added, but the values of the mean and the standard deviation fluctuate relatively little once the distribution contains 20 or 30 units.

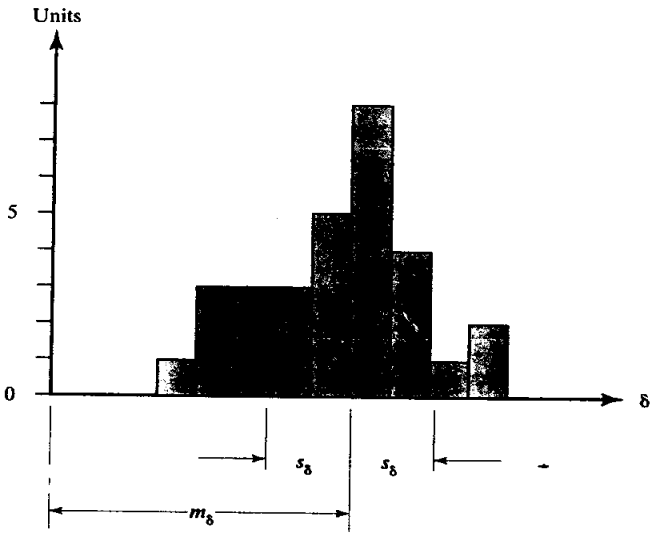

FIGURE 7.1 Histogram of the mismatch, δ, of 30 units, showing mean, m_δ, and standard deviation, s_δ.

Once the mean and standard deviation have been computed using equations 7.2 and 7.3, these can be used to predict worst-case mismatches using one of several indices. The *three-sigma mismatch* equals the sum of the absolute value of the mean plus three times the standard deviation. The *six-sigma mismatch* equals the sum of the absolute value of the mean plus six times the standard deviation. Suppose a pair of resistors shows a mean mismatch of –0.3% with a standard deviation of 0.1%. The three-sigma mismatch of these resistors equals 0.6%, while their six-sigma mismatch equals 0.9%. Less than 1% of all units should have mismatches greater than the three-sigma value, and virtually no units should have mismatches larger than the six-sigma value. The mismatch figures given in this text are all three-sigma values.

7.2 CAUSES OF MISMATCH

Random mismatches stem from microscopic fluctuations in dimensions, dopings, oxide thicknesses, and other parameters that influence component values. Although these statistical fluctuations cannot be entirely eliminated, their impact can be minimized through proper selection of component values and device dimensions. Systematic mismatches stem from process biases, contact resistances, nonuniform current flow, diffusion interactions, mechanical stresses, temperature gradients, and a host of other causes. A major goal of designing matched components consists of rendering them insensitive to various sources of systematic error. The following sections discuss the major known causes of mismatch and techniques for combating them.

7.2.1. Random Statistical Fluctuations

All components exhibit microscopic irregularities, or fluctuations. In the case of a polysilicon resistor, the edges of the poly exhibit microscopic irregularities that give them a slightly ragged appearance. Some of these irregularities stem from the granularity of the polysilicon, while others result from imperfections in the photoresist. The granularity of the polysilicon also causes variations in poly thickness and resistivity. Other types of devices exhibit different types of fluctuations, but all of these fall into one of two categories: fluctuations that occur only along the edges of the device and fluctuations that occur throughout the device. The former are called *peripheral fluctuations* because they scale with device periphery, while the latter are called *areal fluctuations* because they scale with device area. The nature of these scaling relationships can be deduced from statistical arguments.

Consider the case of a pair of matched capacitors, each having capacitance C. The random mismatch due to peripheral and areal fluctuations has a standard deviation s_C, that equals[2,3,4]

$$s_C = \frac{1}{\sqrt{C}}\sqrt{k_a + \frac{k_p}{\sqrt{C}}} \qquad [7.4]$$

where k_a and k_p are constants representing the contributions of areal and peripheral fluctuations, respectively. The contribution of the peripheral term decreases as the capacitance increases. For sufficiently large capacitors, the areal term dominates and the random mismatch becomes inversely proportional to the square root of capacitance. Most practical matched capacitors follow the inverse-square-root relationship fairly closely, so doubling the size of a pair of capacitors decreases their random mismatch by about 30%. The matching of capacitors of different values is dominated by the value of the smaller capacitor, not the larger one. In other words, a 5pF capacitor matches a 50pF capacitor about as well as it matches another 5pF capacitor.

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[2] J. B. Shyu, G. C. Temes, and F. Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources," *IEEE J. Solid-State Circuits*, Vol. SC-19, #6, 1984, pp. 948–956.

[3] J. B. Shyu, G. C. Temes, and K. Yao, "Random Errors in MOS Capacitors," *IEEE J. Solid-State Circuits*, Vol. SC-17, #6, 1982, pp. 1070–1076.

[4] J. L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors," *IEEE J. Solid-State Circuits*, Vol. SC-16, #6, 1981, pp. 608–616.

Now consider the case of a pair of matched resistors[5] having width W and resistance R. The random mismatch between these resistors has a standard deviation s_R that equals

$$s_R = \frac{1}{W\sqrt{R}}\sqrt{k_a + \frac{k_p}{W}} \qquad [7.5]$$

where k_a and k_p are constants representing the contributions of areal and peripheral fluctuations, respectively (Appendix D). This equation shows that random mismatches scale inversely with width. Doubling the width of a pair of matched resistors will at least halve their random offset. The mismatches also scale as the square root of resistance, so larger resistors match better than smaller ones. This leads to a very useful generalization concerning the widths of matched resistors. Suppose a resistance, R_1, requires a width, W_1, to obtain a certain degree of matching. The width, W_2, required to obtain the same degree of matching for a resistance R_2 equals the larger of the two following values:

$$W_2 = W_1\sqrt{\frac{R_1}{R_2}} \qquad [7.6A]$$

$$W_2 = W_1\sqrt[3]{\frac{R_1}{R_2}} \qquad [7.6B]$$

Equation 7.6A represents the extreme case where areal fluctuations dominate over peripheral fluctuations, while equation 7.6B represents the opposite extreme. The actual situation lies somewhere between these extremes, although areal effects generally predominate. As long as one takes the larger of the two widths given by the equations, the matching of the new resistor R_2 should always equal or exceed the matching of the original resistor R_1. In the case of matched resistors of different values, the smaller of the two resistances should be used in equations 7.6A and 7.6B.

An example will clarify the use of these equations. Suppose a pair of 6μm-wide 10kΩ resistors have a worst-case random mismatch of ±0.1%. What width is required to obtain the same degree of matching between 100kΩ resistors? Equation 7.6A predicts a minimum width of 1.90μm, while equation 7.6B predicts a minimum width of 2.78μm. The actual width required to obtain this degree of matching therefore lies somewhere between 1.90μm and 2.78μm. A conservative designer would probably make these resistors 3μm wide.

Equations 7.6A and 7.6B only apply to poly resistors in which the resistor is much wider than its largest poly grains. If this condition is not met, then the equations will underestimate the mismatch of the resistors. Most poly grains are less than 1μm across,[6] so matched poly resistors should be made at least 2 to 3μm wide.

N-type poly resistors seem to exhibit larger random mismatches than P-type poly resistors. On one advanced bipolar process, N-doped poly resistors exhibited approximately twice the random mismatch of P-doped poly resistors having similar dimensions and sheet resistance.[7] This effect may stem from dopant segregation

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[5] Resistor matching is also treated in W. A. Lane and G. T. Wrixon, "The Design of Thin-Film Polysilicon Resistors for Analog IC Applications," *IEEE Trans. on Electron Devices*, Vol. 36, #4, 1989, pp. 738–744.

[6] A. C. Adams, "Dielectric and Polysilican Film Deposition," in S. M. Sze, ed., *VLSI Technology*, 2nd ed., (New York: McGraw-Hill, 1983), p. 244.

[7] M. Corsi, private communication, 1998.

at grain boundaries.[8] The exact explanation remains unclear, so it is not certain that P-type poly resistors will always exhibit less random mismatch than N-type poly resistors.

7.2.2. Process Biases

The dimensions of geometries fabricated in silicon never exactly match those in the layout database because the geometries shrink or expand during photolithography, etching, diffusion, and implantation. The difference between the drawn width of a geometry and its actual measured width constitutes the *process bias.* Process biases can introduce major systematic mismatches in poorly designed components. Consider the case of two matched poly resistors having widths of 2μm and 4μm, respectively. Suppose that poly etching introduces a process bias of 0.1μm. The ratio of the actual widths equals (2 + 0.1)/(4 + 0.1), or 0.512. This represents a systematic mismatch of no less than 2.4%! Since most processing steps have biases of at least 0.1μm, the layout designer must ensure that all matched devices are insensitive to process biases. In the case of resistors, process biases can be virtually eliminated by simply making both resistors the same width.

Process biases can also affect the length of a resistor. The length of most resistors is determined by the placement of their contacts. Suppose that these contacts have a process bias of 0.2μm. If one matched resistor was 20μm long and the other was 40μm long, then the mismatch due to this bias would equal (20 + 0.2)/(40 + 0.2), or 0.503. This represents a systematic mismatch of about 0.5%. The simplest way to avoid this bias consists of dividing both matched resistors into segments of the same size. If the resistors of the previous example were laid out in 20μm segments, then the ratio of the resistors would equal (20 + 0.2)/[2·(20 + 0.2)], or exactly 0.5. The same stratagem has already been shown to eliminate systematic mismatches due to contact resistances and nonlinear current flow at the ends of the resistors. Section 7.2.6 explains how to divide matched resistors into arrays of optimally sized segments.

Capacitors also experience systematic mismatches caused by process biases. Suppose a pair of poly-poly capacitors, one measuring 10×10μm and the other 10×20μm, both experience a poly etch bias of 0.1μm. The actual area of the 10×10μm capacitor equals $(10.1)^2$, or 102.1μm^2, while the actual area of the 10×20μm capacitor equals (10.1·20.1), or 203.01μm^2. The ratio of these two areas equals 0.5029, which represents a systematic mismatch of 0.6%.

In theory, matched capacitors become insensitive to process biases when their area-to-periphery ratios equal one another. In the case of two capacitors of the same value, this can be achieved by using the same geometry for both capacitors. Identical matched capacitors are usually laid out as squares because this reduces their area-to-periphery ratio, which in turn minimizes the contribution of peripheral fluctuations to their random mismatch. The problem becomes somewhat more difficult if the capacitors have values that are not in simple ratio. Although the smaller capacitor should still be laid out as a square, the larger capacitor must be laid out as a rectangle. Suppose the smaller capacitor, C_1, has dimensions L_1 by L_1

[8] J. C. C. Tsai, "Diffusion," in S. M. Sze, ed., p. 312.

(Figure 7.2). The larger capacitor, C_2, should have a length L_2 and a width W_2 equal to[9]

$$L_2 = \frac{C_2}{C_1}\left(1 + \sqrt{1 - \frac{C_1}{C_2}}\right) \qquad [7.7A]$$

$$W_2 = \frac{C_2}{C_1}\left(1 - \sqrt{1 - \frac{C_1}{C_2}}\right) \qquad [7.7B]$$

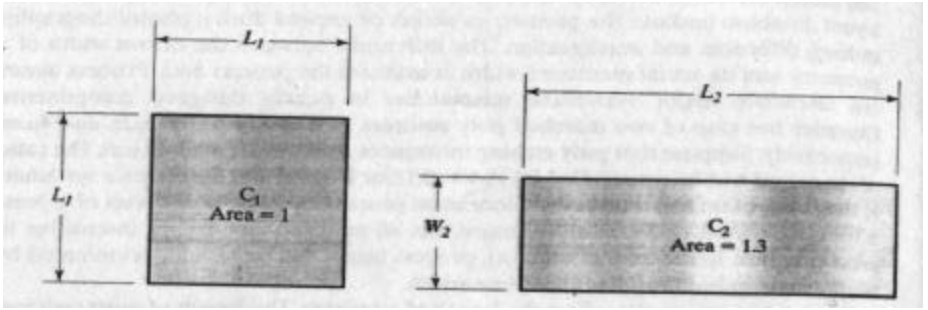


FIGURE 7.2 Matching capacitors using identical area-to-periphery ratios.

Although equations 7.7A and 7.7B theoretically eliminate systematic mismatches due to process bias, in practice things do not work out so nicely. Process biases are not constant quantities; they actually depend on the dimensions of the geometries in question. The process biases experienced by a rectangular capacitor do not precisely equal those experienced by a square capacitor. This problem becomes increasingly severe for larger ratios. Rectangular capacitors also increase the contribution of peripheral fluctuations to random mismatches. In practice, capacitors with ratios of more than 1.5:1 should not be constructed using equations 7.7A and 7.7B. In such cases, the designer should instead resort to using arrays of matched capacitor segments, or *unit capacitors*.[10]

Not all systematic mismatches are due to process biases. Other mechanisms that produce systematic mismatches include pattern shift, etch variations, diffusion interactions, mechanical stresses, thermal gradients, thermoelectrics, voltage modulation, charge spreading, and dielectric polarization. The following sections take up each of these topics in turn.

7.2.3. Pattern Shift

As discussed in Section 2.5.1, surface discontinuities left from the thermal annealing of the N-buried layer (NBL) propagate up through the monocrystalline silicon layer deposited during vapor-phase epitaxy. The resulting surface discontinuities become faintly visible under an optical microscope, particularly when lateral illumination is used. This image, called the *NBL shadow*, serves as a registration marker for the alignment of subsequent diffusions.

Process engineers have long been aware that surface discontinuities present in the substrate are not always faithfully reproduced in the final silicon surface. These discontinuities are frequently displaced laterally during epitaxial growth (Figure 7.3A). This effect is called *pattern shift*. Sometimes the various edges of

[9] Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Technology* (New York: McGraw-Hill, 1996), pp. 220–223.

[10] M. J. McNutt, S. LeMarquis, and J. L. Dunkley, "Systematic Capacitance Matching Errors and Corrective Layout Procedures," *IEEE J. Solid-State Circuits*, Vol. 29, #5, 1994, pp. 611–616.

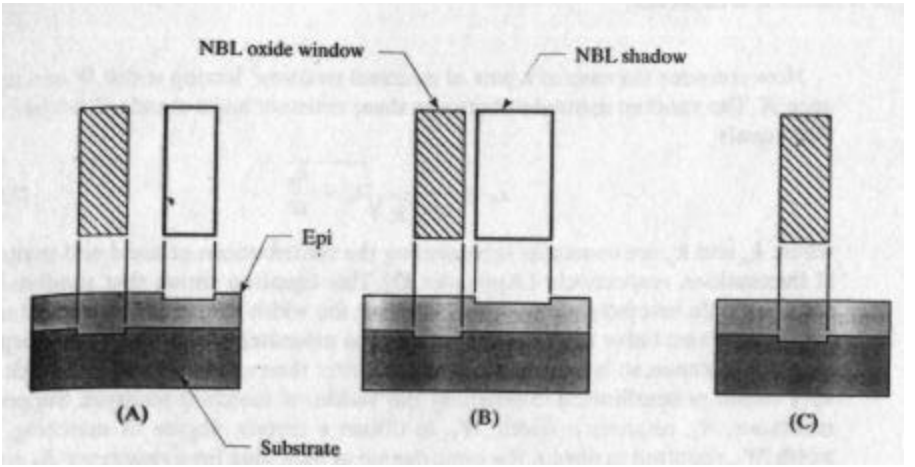


FIGURE 7.3 Effects of epitaxy on surface discontinuities: (A) pattern shift, (B) pattern distortion, and (C) pattern washout.

the discontinuity shift by different amounts. causing *pattern distortion* (Figure 7.3B). Occasionally the surface discontinuities completely vanish during the course of epitaxy, causing *pattern washout* (Figure 7.3C).

Pattern shift, distortion, and washout are all manifestations of the same underlying phenomenon. During vapor-phase epitaxy, reactant molecules adsorb on the silicon surface and move laterally until they find suitable locations where they can incorporate into the growing lattice. The exposed microsteps, formed by the intersection of the crystal lattice with the surface, encourage crystal growth in a specific direction and cause the surface topography to shift as epitaxy continues. Wafers that are (111)-oriented experience relatively severe pattern shift and distortion, which can be minimized by tilting the plane of the wafer by approximately 4° around a <110> axis.[11] Wafers that are (100)-oriented experience significant pattern distortion, but no pattern shift. The use of slightly tilted (100)-oriented wafers minimizes pattern distortion at the price of introducing pattern shift.

The magnitude of pattern shift depends upon the mobility of adsorbed reactants and the crystal orientation. Higher pressures, faster growth rates, and the presence of chlorine as a substituent in the reactant all favor increased pattern shift, while higher temperatures tend to reduce it. LPCVD deposition of dichlorosilane on (111) silicon tilted 4° will induce a pattern shift of 50 to 150% of the thickness of the epi along a <211> axis, while similar conditions using silicon tetrachloride will induce pattern shifts of 100 to 200% of the epi thickness.[12]

Due to the many variables involved, the direction and magnitude of pattern shift in a specific process can only be determined through experimental observation. A high-quality optical microscope with at least 100X magnification and a reflective illuminator are required. The shadow is usually clearest in the vicinity of minimum-geometry NPN transistors; it appears as a faint dark line not associated with any corresponding change in the oxide color. Once the shadow has been identified, the NBL shift can be estimated by comparison to features of known dimensions, such as contacts or narrow resistors. Metal lines are not recommended as a reference for comparisons because their process biases are often quite large. The deposition of interlevel oxide (ILO) obscures the NBL shadow, and planarization renders it

[11] W. R. Runyan and K. E. Bean, *Semiconductor Integrated Circuit Processing Technology* (Reading, MA: Addison-Wesley, 1994), p. 331.

[12] For further discussion, see Runyan, *et al.*, pp. 331–333.

completely invisible. Wafers used for measuring NBL shift must therefore be removed from the process prior to ILO deposition and planarization.

Pattern shift becomes a potential concern whenever matched devices are laid out in a process that employs a patterned buried layer, such as the NBL of standard bipolar and analog BiCMOS. If the NBL shadow intersects a component, it may interfere with diffusion and implantation and may cause subtle shifts in component value. Not all components are necessarily affected by pattern shift. Capacitors generally do not incorporate NBL, and polysilicon resistors usually reside over field oxide. On the other hand, diffused resistors are usually enclosed in tanks or wells containing NBL. HSR resistors are especially susceptible because the extremely thin high-sheet implant is less tolerant of slight surface discontinuities than are deeper diffusions.

Figure 7.4 depicts four matched base resistors laid out in a common tank containing NBL. Assuming this process exhibits a pattern shift to the right, then the NBL shadow intersects the leftmost resistor. There are several ways to avoid this intersection. The simplest approach consists of removing NBL from beneath the components. While this certainly eliminates the NBL shadow, it also needlessly increases the tank resistance and potentially leaves the circuit vulnerable to latchup. A better approach relies on knowledge of the direction of pattern shift. If the NBL shadow shifts to the right, then the overlap of the left edge of the NBL over the components can be increased so that the NBL shadow cannot fall across them, even with worst-case pattern shifts and misalignments. This usually requires that the NBL overlap the components by at least 120% of the nominal pattern shift. If no experimental data on the direction of the pattern shift exists, then the NBL must overlap all sides of the devices vulnerable to encroachment by the NBL shadow. In the layout in Figure 7.4, the left and right sides of the resistors are vulnerable, while the top and bottom are not. If no information on the magnitude of the pattern shift exists, then the NBL should overlap the components by at least 150% of the nominal epi thickness.

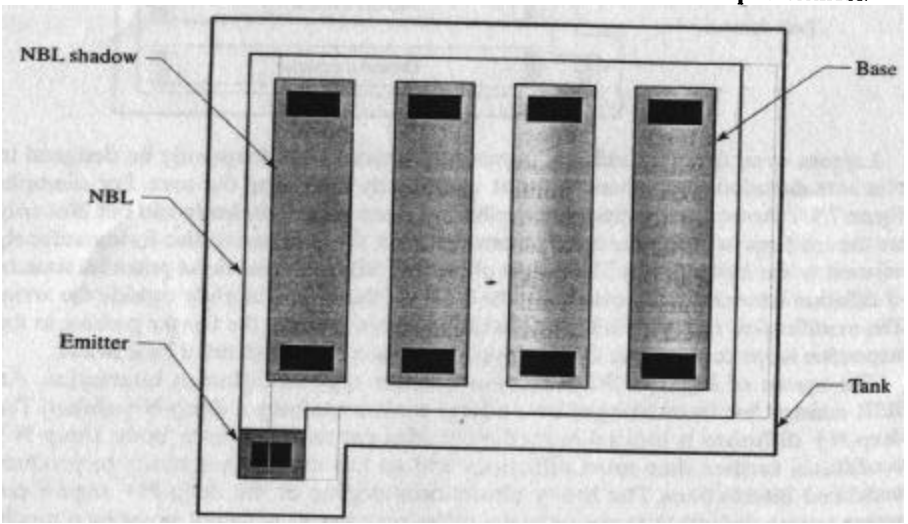


FIGURE 7.4 Layout showing an intersection of the NBL shadow with the leftmost base resistor.

7.2.4. Variations in Polysilicon Etch Rate

Poly resistors are created by etching a doped polysilicon film. The etching rate depends, at least to some extent, on the geometry of the poly openings. Larger openings grant more access to the etchant and thus clear more quickly than small open-

ings. Consequently, sidewall erosion occurs to a greater degree around the edges of a large opening than around the edges of a small one. This effect causes widely separated poly geometries to have smaller widths than closely packed geometries do. Consider the case of three polysilicon resistors with no other nearby regions of poly (Figure 7.5). The edges of the resistors facing outward form the sidewalls of a vast opening that etches quickly and clears early. The edges of the resistors facing inward form sidewalls of narrow slits that etch more slowly and clear later. The middle resistor lacks outward-facing edges, so it has a slightly larger final width than either of the other resistors.

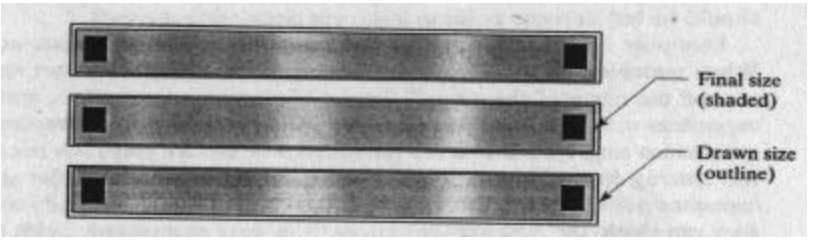


FIGURE 7.5 Variations in etch rate in an array of supposedly matched resistors. The exposed outer edges of the resistors experience overetching relative to the protected inner edges.

Although small, these variations in etch rate are sufficient to produce serious systematic mismatches. Suppose that a 10kÅ polysilicon film etches 90% anisotropically, resulting in an undercut of 0.1μm. The difference between the undercutting of the outward-facing and inward-facing edges is unlikely to be more than a small fraction of the total undercut, perhaps 0.02μm. As small as this value seems, it still represents 0.5% of the width of a 4μm resistor.

When a number of polysilicon strips are arrayed side-by-side, only the strips on the ends of the array experience etch rate variations. *Dummy resistors* (or *etch guards*) are often added to either end of an array of matched resistors to ensure uniform etching (Figure 7.6).[13] The dummy resistors may be constructed in one of two ways. *Unconnected dummies* are simply strips of polysilicon placed on either side of the array (Figure 7.6A). The spacing between the dummy segments and the adjacent resistors must match the spacing between the resistors of the array. The width of poly geometries has little effect on their etch rates, so the dummies can be made much narrower than the resistors they protect. This scheme has the slight disadvantage that the dummy segments remain electrically unconnected. Since the oxide isolating these segments is an exceptionally good insulator, a static electrical charge

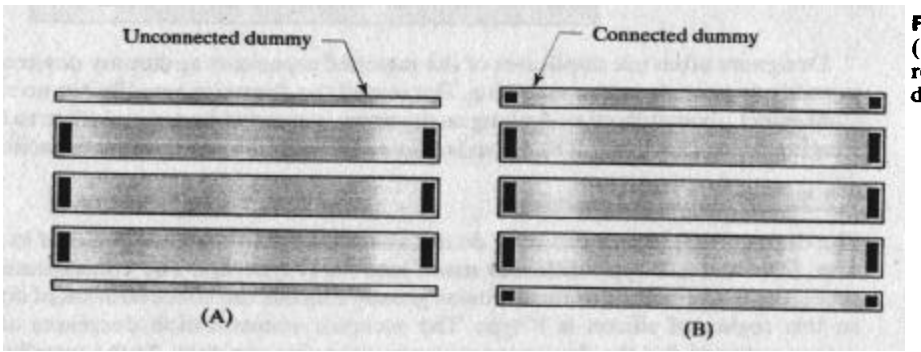


FIGURE 7.6 Examples of (A) unconnected dummy resistors and (B) connected dummy resistors.

[13] Y. Tsividis, pp. 229–231. Tsividis's structure includes dummies, but is not connected to neutralize thermoelectrics (Section 7.1.6).

can accumulate on the dummy segments. This charge might influence the behavior of adjacent resistors. Any possibility of electrostatic modulation can be eliminated by connecting the dummies to ground or to some other suitable low-impedance node (Figure 7.6B).

A less-desirable style of dummy resistor consists of a continuous ring of poly looped around the resistor array. Dry etching employs intense electromagnetic fields to generate and direct the reactive ions. These fields can interact with the loop of polysilicon to produce circulating currents that could affect etch rates during the final minutes of etching. Instead of an unbroken loop, consider using separate dummy segments like those in Figure 7.6. If a loop must be employed, then a gap should be left at some point to interrupt circulating currents.

Poly-poly capacitors experience the same etch rate variations as poly resistors. When matching arrays of capacitors, additional dummy capacitors should be placed around the edges of the array.[14] Figure 7.7 shows an array of six matched poly-poly capacitors with grounded dummies. Individual strips are again employed instead of a continuous ring. Notice that the poly-2 (shown in dark gray) has been drawn so that the spacing from dummy poly-2 to capacitor poly-2 matches the spacing between capacitor poly-2 regions. The dummies should always be electrically connected so that they can shield the matched capacitors from stray electrostatic fields (Section 7.2.8).

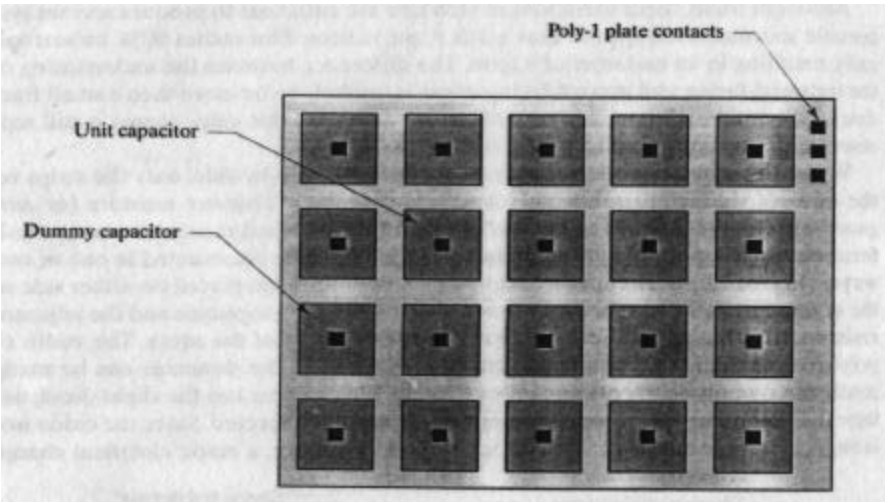


FIGURE 7.7 Matched capacitor array employing grounded dummies. The metal-2 electrostatic shield covering this array has been omitted for clarity.

Designers often use duplicates of the matched capacitors as dummy devices, presumably to provide better matching. The size of the dummies actually has no significant effect upon etch rates. As long as the array is covered by a metal plate to block fringing fields (Section 7.2.8), there is no need to use full-size dummy capacitors.

7.2.5. Diffusion Interactions

The dopants that form a diffusion do not all reside within the boundaries of its junction. Consider a P-type diffusion made into an N-type epi. The concentration of acceptors in the middle of the diffusion greatly exceeds the concentration of donors, so this region of silicon is P-type. The acceptor concentration decreases as one moves outward, but the donor concentration remains constant. At the *metallurgical*

[14] Y. Tsividis, p. 228.

junction, the acceptor concentration exactly equals the donor concentration. Beyond the junction, the acceptor concentration drops below the donor concentration and the silicon becomes N-type. The acceptor concentration falls to negligible levels some distance outside the junction. The portion of the dopant that lies outside the metallurgical junction is called the *tail* of the diffusion.

The tails of two adjacent diffusions will intersect one another. Assuming that both diffusions are of the same polarity, their tails add and each diffusion reinforces the other. Both diffusions will have slightly lower sheet resistances and slightly greater widths than they would have had in isolation from one another. Exactly the opposite situation occurs if the diffusions are of opposite polarities. The two intersecting tails counterdope one another, causing both diffusions to have slightly higher sheet resistances and slightly narrower widths.

The effects of diffusion interactions on matching resemble those discussed previously for variations in poly etch rate. The resistors occupying the ends of the array will have slightly different values than the resistors occupying the middle of the array. This source of systematic mismatch can be eliminated by adding dummy resistors to either end of the array. These diffused dummy resistors must have exactly the same width as the other resistors to ensure that their dopant profiles match. The dummy resistors should be connected to prevent the formation of floating diffusions that could exacerbate latchup sensitivity (Figure 7.8).

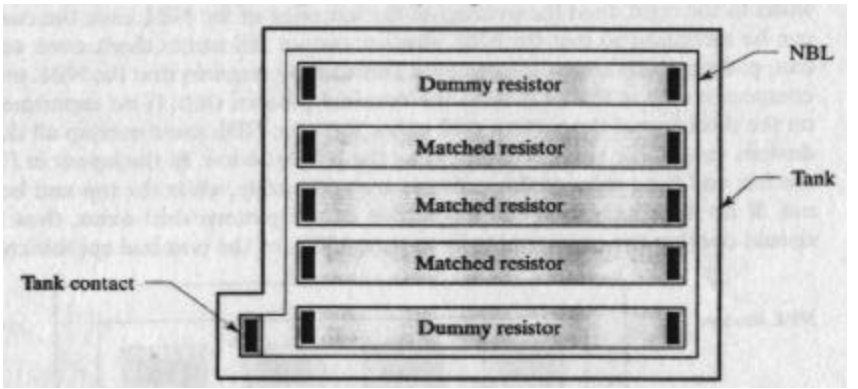


FIGURE 7.8 Matched array of diffused base resistors including grounded dummies.

Layouts, even those of ordinary unmatched resistors, can frequently be designed to eliminate diffusion interactions without significantly increasing die area. For example, Figure 7.9A shows a serpentine resistor that has been rather carelessly laid out. Not only are the spacings between the turns inconsistent, but the base heads also lie immediately adjacent to the resistor body. The layout of Figure 7.9B minimizes these potential sources of diffusion interactions by extending the heads of the resistor slightly outside the array. This modification requires little or no additional area because the tighter packing in the serpentine helps compensate for the room consumed by the extended base heads.

The layout of Figure 7.9C illustrates another type of diffusion interaction. An HSR resistor has been merged into a large tank containing a deep-N+ sinker. The deep-N+ diffusion is located immediately adjacent to the resistor body. Deep-N+ outdiffuses further than most diffusions and so has more opportunity to produce undesired interactions. The heavy phosphorus doping of the deep-N+ region can spawn lattice defects that can enhance diffusion rates in adjacent areas by a mechanism similar to emitter push (Section 2.4.2). Severe diffusion interactions may occur when these two mechanisms reinforce each other. Figure 7.9D shows a more prudent layout that places the deep-N+ sinker behind one head of the resistor, where it will have little or no effect on the resistance of the device.

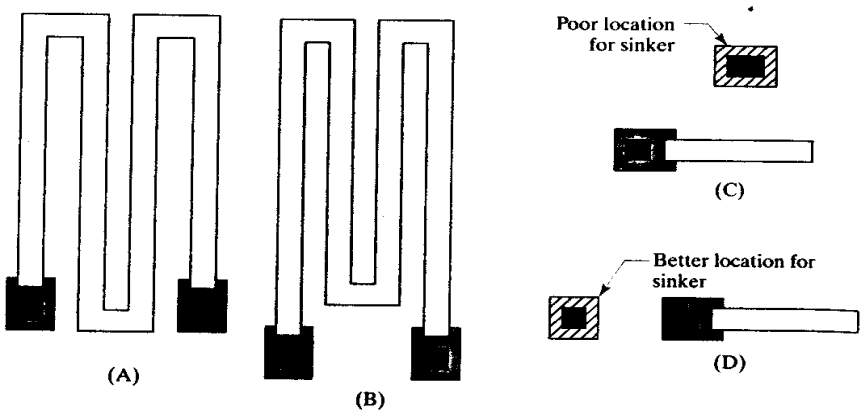


FIGURE 7.9 Examples of additional opportunities for reducing diffusion interactions: (A) poor serpentine resistor layout and (B) improved layout; (C) poor placement of deep-N+ sinker and (D) improved placement.

7.2.6. Stress Gradients and Package Shifts

Silicon is *piezoresistive* in that it exhibits changes in resistivity under stress. Variations in stress across the die will produce corresponding variations in resistor matching. Capacitors generally remain unaffected by stresses because the dimensions and permittivity of the dielectric are relatively insensitive to mechanical stress. Although well-matched capacitors usually exhibit less systematic mismatch than well-matched resistors, not all circuits can rely on matched capacitors. Layout techniques have been developed for minimizing the stress sensitivity of resistors. The severity of the problem varies from one design to the next because different forms of packaging produce higher or lower levels of stress.

Metal cans have been used to package semiconductors from the earliest days of the industry. Although they are expensive, they can provide a reliable low-stress means of packaging dice. In this type of package, the die rests on a metal plate called a *header*. After wirebonding, the package is hermetically sealed by welding a metal cap over the header. A metal can package induces little or no residual die stress as long as the die is mounted using epoxy rather than solder or gold eutectic. Although the metal header and the silicon die have vastly different coefficients of thermal expansion (Table 7.1), the epoxy absorbs the resulting strain and provides mechanical compliance. Precision integrated circuits that require extremely precise matching are often packaged in metal cans or in hermetically sealed ceramic packages that offer similar benefits.

TABLE 7.1 Coefficients of thermal expansion (CTE) for several materials used in packaging integrated circuits.[15]

Material	CTE ppm/°C
Epoxy encapsulation (typical)	24
Copper alloys	16–18
Alloy-42	4.5
Molybdenum	2.5
Silicon	2.5

[15] Values for epoxy, molybdenum, and silicon: R. E. Thomas, "Stress-Induced Deformation of Aluminum Metallization in Plastic Molded Semiconductor Devices," *IEEE Trans. on Components, Hybrids, and Manufacturing Technology*, Vol. CHMT-8, #4, 1985, pp. 427–434. Values for Alloy 42 and copper from "Leadframe Materials" *Semiconductor Reliability News*, Vol. 8, #9, September 1996, p. 5.

Plastic packages are much more widely used than either metal cans or ceramic packages. As Table 7.1 indicates, the coefficient of thermal expansion of plastic encapsulants is approximately ten times that of silicon. The epoxy resin flows into the mold at high temperature. As the encapsulated device cools, the difference between the coefficients of thermal expansion of silicon and epoxy generates residual stresses that remain permanently frozen into the packaged device. Measurements of electrical parameters before and after packaging will reveal differences called *package shifts* proportional to the level of residual stress. The input offset voltages of operational amplifiers and comparators and the output voltage of references often exhibit package shifts (Section 9.2.5). Package shifts set a lower limit on achievable accuracy that cannot be sidestepped through wafer-level trimming. Careful layout can usually reduce the sensitivity of a circuit to mechanical stress, which can in turn reduce the magnitude of the package shifts.

Power packaging requires an intimate thermal union between the die and its leadframe or its header in order to minimize heat build-up. The die attach for a power package consists of either silver-filled epoxy, solder, or gold eutectic. Silver-filled epoxies do not provide quite as good a thermal and electrical union as either of the other two alternatives, but epoxy mounting is desirable for precision devices because it produces lower residual stresses. Solder mounting is commonly employed in large metal tab or can packages. Since solder does not adhere to silicon, the back side of the die must be plated with a sputtered or evaporated metal film. Gold eutectic bonding uses a thin strip of gold foil called a *gold preform* placed between the die and the header. When heated, the gold preform alloys to both materials. Neither solder nor gold alloy has much mechanical compliance, so the thermal mismatch between the copper header and the silicon die generates extreme stresses.

Several methods exist for minimizing package stress. Although "low-stress" mold compounds exist, these do not seem to reduce packing stresses sufficiently to justify their use. A better procedure consists of coating each chip with polyimide resin prior to encapsulation. The polyimide overcoat provides mechanical compliance between the mold compound and the die. If used in conjunction with an epoxy die attach, polyimide overcoating can substantially reduce stress levels in plastic. The special equipment required and additional process time consumed make this an expensive proposition. Stresses due to solder or gold eutectic mounting can be minimized by constructing the header out of a material with a coefficient of thermal expansion similar to that of silicon, such as molybdenum or alloy-42 (a nickel-iron alloy containing 42% nickel). Molybdenum headers are expensive, while alloy-42 is brittle and exhibits poor thermal and electrical conductivity. The vast majority of products use plastic encapsulation in combination with copper alloy headers or leadframes, so the remainder of this section discusses the effects of this type of packaging.

Piezoresistivity

The piezoresistivity of (100)-oriented silicon varies with orientation and doping.[16] An N-type (100) silicon wafer exhibits maximum piezoresistivity along [100] directions and minimum piezoresistivity along <110> axes. N-type diffused and implanted resistors therefore exhibit minimum stress sensitivity if they lie along <110>

[16] Y. Kanda, "A Graphical Representation of the Piezoresistance Coefficients in Silicon," *IEEE Trans. on Electron Devices*, Vol. ED-29, #1, 1982, pp. 64–70.

axes. One of the <110> axes of the wafer lies parallel to the major wafer flat, while the other <110> axis lies perpendicular to it (Figure 7.10). Since dice are laid out in rows and columns relative to the wafer flat, the X- and Y-axes of the layout correspond to the desired <110> directions. The stress sensitivity of N-type monocrystalline resistors can therefore be minimized by laying them out either horizontally or vertically.

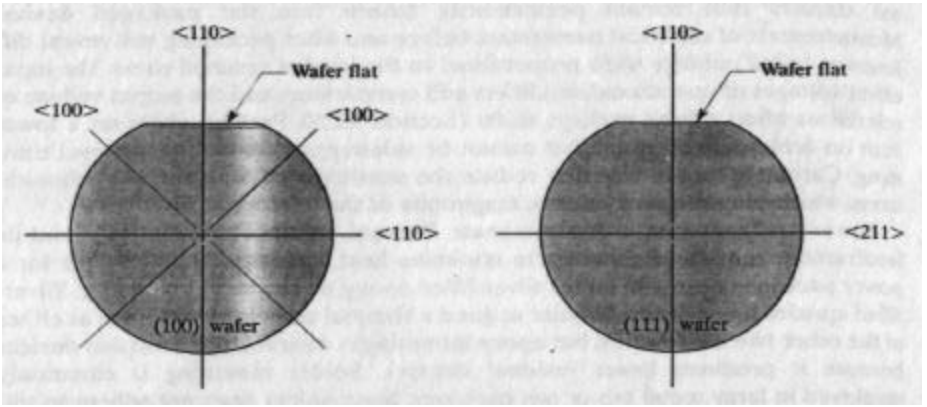


FIGURE 7.10 Identification of directions on (100) and (111) wafers.

A P-type (100) silicon wafer exhibits maximum piezoresistivity along <110> axes and minimum piezoresistivity along <100> axes. P-type diffused and implanted resistors therefore exhibit the least stress sensitivity if they lie along <100> axes. The <100> axes of a (100) wafer are rotated 45° to the wafer flat (Figure 7.10). P-type monocrystalline resistors therefore exhibit the least stress sensitivity if they are placed at 45° to the X- and Y-axes of the layout. When so oriented, the piezoresistivity of P-type monocrystalline resistors actually falls to zero. This does not occur with N-type resistors, which still retain some degree of piezoresistivity even when oriented in the optimum directions. This difference constitutes one reason for preferring P-type monocrystalline resistors to their N-type counterparts.

The piezoresistivity of a (111) wafer does not vary with direction. Although no reason exists to prefer one orientation over another, most resistors on (111) silicon are placed either vertically or horizontally to simplify packing and interconnection.

The piezoresistivity of monocrystalline silicon exhibits little dependence on doping concentrations as long as these do not exceed about 10^{18} atoms/cm^3. Almost all matched resistors use significantly lower dopant concentrations, so low-sheet and high-sheet materials exhibit no significant differences in piezoresistivity.

Polycrystalline silicon is an isotropic material, so its piezoresistivity is the same in all directions. The magnitude of this piezoresistivity drops as the resistivity of the poly increases.[17] Lightly doped poly of the sort normally used to make resistors has a relatively small (but nonzero) stress dependency. The [100]-oriented P-type diffused resistors on (100) silicon will have lower stress sensitivities than poly resistors, but the poly resistors may have better overall matching because they do not exhibit the voltage modulation problems that plague most types of diffused and implanted resistors (Section 7.2.8).

[17] H. Mikoshiba, "Stress-Sensitive Properties of Silicon-Gate MOS Devices," *Solid-State Electronics*, Vol. 24, 1981, pp. 221–232.

Gradients and Centroids

Figure 7.11 graphically illustrates the stress distribution across a typical integrated circuit. The drawing at the lower left is called an *isobaric contour plot.* The curved lines (called *isobars*) indicate the stress levels at various points on the die surface. Each isobar passes through a series of points of equal stress intensity. The stress intensity rises from a broad minimum in the middle of the die to maxima at the four corners. The graph above the contour plot shows the stress intensity along a line bisecting the die horizontally, while the graph at the right shows the stress intensity along a line bisecting the die vertically. By comparing the two graphs to the contour plot from which they were generated, the general nature of the latter should become apparent. Contour plots resembling this one are used in topographic mapping to display the three-dimensional shapes of hills and valleys. The distribution of stress on a die resembles a depression: it is lowest in the middle of the die and highest at the four corners.

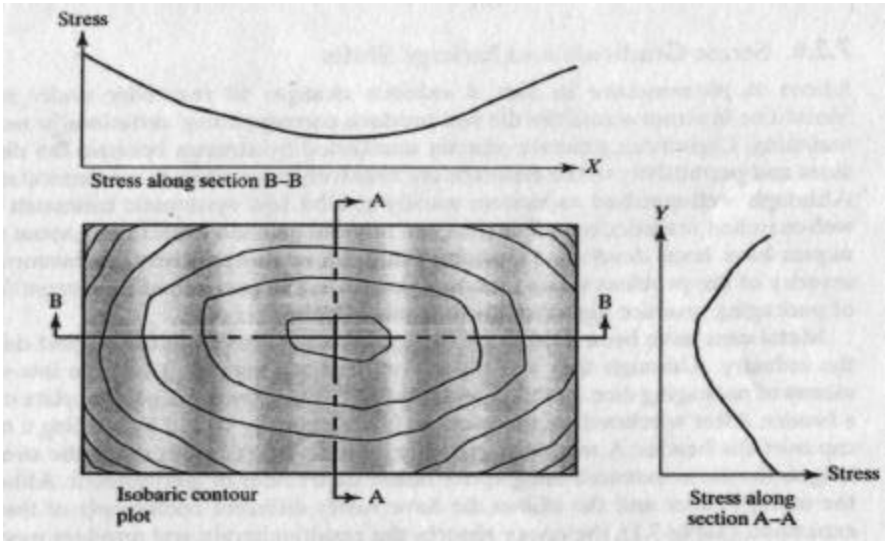


FIGURE 7.11 Isobaric contour plot of the stress distribution across the surface of a typical epoxy-mounted plastic-packaged (100) silicon die, together with two graphs showing the stress along section lines A–A and B–B.

The spacing of the isobars provides additional information about the stress distribution. The stress intensity changes rapidly where the isobars are spaced closely together, and slowly where they are spaced far apart. The rate of change of the stress intensity is called the *stress gradient.* This gradient is usually smallest in the middle of the die and slowly increases as one moves out toward the edges. The stress gradient is usually much greater at the extreme corners of the die than at any other point (Figure 7.12).

Matched devices should reside as close to one another as possible to minimize the difference in stresses between them. Although the finite size of the devices might seem to limit how closely they can be placed, certain layout techniques can produce remarkably small separations. The following analysis assumes that the stress gradient is approximately constant in the region between the matched devices. This is generally a reasonable assumption providing that the matched devices are placed to form as compact a structure as possible.

The stress difference between two matched devices is proportional to the product of the stress gradient and the separation between them. For the purposes of this

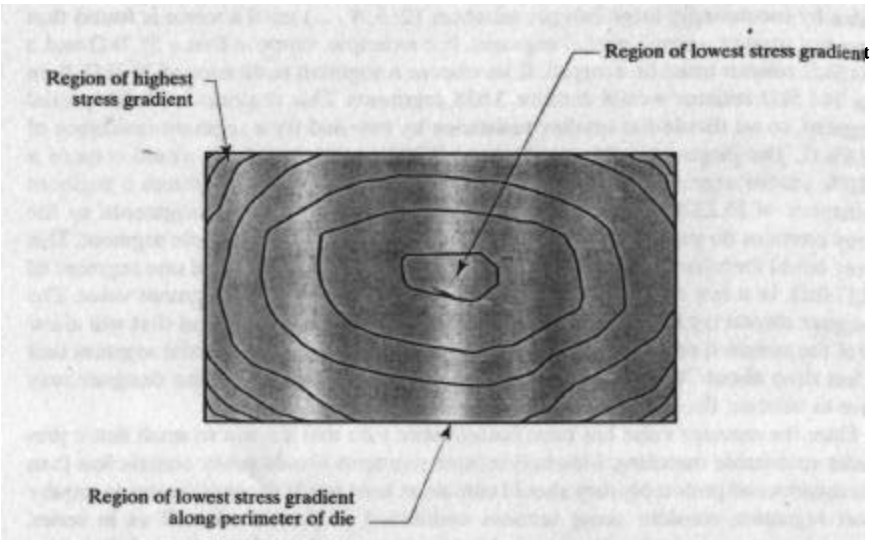


FIGURE 7.12 Isobaric contour plot showing regions of highest and lowest stress gradient.

calculation, the location of each device is computed by averaging the contribution of each portion of the device to the whole.[18] The resulting location is called the *centroid* of the device. The centroid of a rectangular device lies in its exact center. The centroids of other geometries can often be located by applying the *principle of centroidal symmetry,* which states that the centroid of a geometry must lie on any axis of symmetry of that geometry. Figure 7.13 shows how this principle can determine the centroids of a rectangle and a dogbone resistor. The centroid of practically any geometry used in layout can be determined in a similar manner.

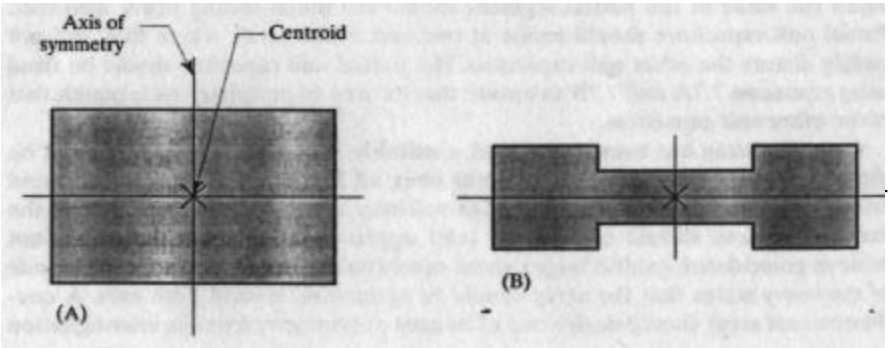


FIGURE 7.13 Locating (A) the centroids of a rectangle and (B) a dogbone resistor.

The effects of stress on resistors can be quantified in terms of piezoresistivity, centroid locations, and stress gradients. The magnitude of the stress-induced mismatch δ_s between two resistors equals

$$\delta_s = \pi_{cc} d_{cc} \nabla S_{cc} \qquad [7.8]$$

where π_{cc} is the piezoresistivity along a line connecting the centroids of the two matched devices, ∇S_{cc} is the stress gradient along this same line, and d_{cc} equals the

[18] Most texts on statics include a discussion of centroids and their relationship to the well-known principle of moments, *e.g.*, R. C. Hibbeler, *Engineering Mechanics: Statics,* 4th ed. (New York: Macmillian Publishing Co. 1998), p. 435.

distance between the centroids. This formula reveals several ways to minimize stress sensitivity. First, the designer can reduce the piezoresistivity, π_{cc}, by choosing a suitable resistance material or by orienting the resistors in the direction of minimum piezoresistivity. Second, the designer can reduce the magnitude of the stress gradient, ∇S_{cc}, by proper location of the devices and by selecting low-stress packaging materials. Third, the designer can reduce the separation between the centroids of the device, d_{cc}. The first two options have already been discussed, so we will now focus on reducing the separation of the centroids.

Common-centroid Layout

Suppose that a matched device is divided into sections. If these sections are all identical, and if they are arranged to form a symmetric pattern, then the centroid of the device will lie at the intersection of the axes of symmetry passing through the array. It is actually possible to arrange two arrayed devices so that they share common axes of symmetry. If this can be achieved, then the principle of centroidal symmetry ensures that the centroids of the two devices coincide. Figure 7.14A shows an example of such a *common-centroid* layout. The two devices are marked A and B, their axes of symmetry are shown as dotted lines. and their centroids are denoted by an "X" where the two axes of symmetry intersect.

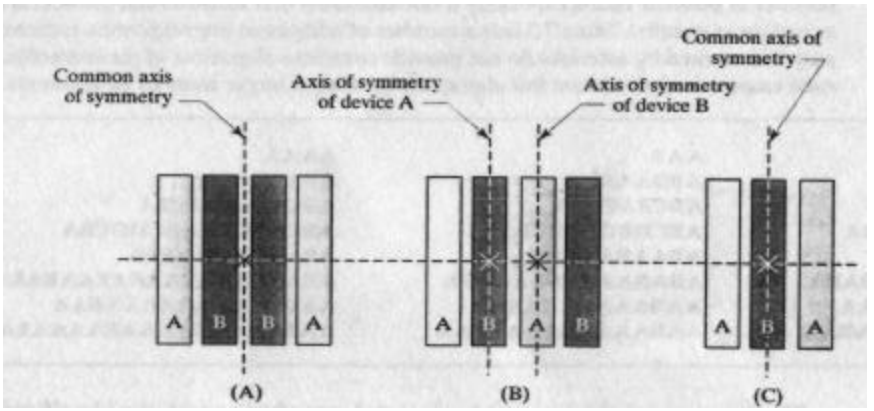


FIGURE 7.14 Examples of one-dimensional common-centroid arrays.

Equation 7.8 predicts that the stress-induced mismatch of a common-centroid layout equals zero because the separation between the centroids equals zero. This does not actually occur, because the stress gradient never remains precisely constant. Despite this limitation, common-centroid layout is still the single most powerful technique available for minimizing stress-induced mismatches. Well-designed common-centroid layouts can reduce the stress sensitivity of large devices by an order of magnitude or more.

Figure 7.14 shows three examples of common-centroid layouts produced by arraying segments of matched devices along one dimension. These types of layouts are usually called *interdigitated arrays* because the sections of one device interpenetrate the sections of the other like the intermeshed fingers of two hands. Figure 7.14A shows an interdigitated array consisting of two devices, each composed of two segments. If the devices are denoted by the letters A and B, then the arrangement of the segments follows the *interdigitation pattern* (or *weave*) ABBA. This pattern has an axis of symmetry that divides it into two mirror-image halves (AB and BA). A second axis of symmetry passes horizontally through the array, but this axis results from the symmetries of the individual segments rather than the symmetry of the interdigitation pattern.

Arrays that use the interdigitation pattern ABBA require dummies because the segments of one device occupy both ends of the array. Some designers prefer to use arrays that follow the pattern ABAB (Figure 7.14B) because they mistakenly believe that this pattern eliminates the need for dummies. This belief is founded on a misunderstanding of the function of the dummy devices. Etch variations and diffusion interactions depend on the arrangement of adjacent geometries. The addition of dummy devices ensures that each segment faces an identical arrangement of geometries. If the dummies are omitted, then the segments on the ends of the array face whatever geometries happen to reside nearby. The geometries adjacent to one end of the array are likely to differ from those next to the other. If this happens, then mismatches will result if dummies are omitted regardless of whether the array follows the pattern ABBA or ABAB. The pattern ABAB should be avoided because it does not completely align the centroids of the two devices, and the resulting separation of the centroids leaves the devices vulnerable to stress-induced mimatches.

Common-centroid layouts can also consist of devices of different sizes. Figure 7.14C shows an example that implements a 2:1 ratio using the pattern ABA. If the two devices on the end of the array are resistors, then they can connect either in series or in parallel. If they are capacitors, they can only connect in parallel because a series connection would introduce mismatches caused by the differences in parasitic capacitances between the upper and lower plates. More complicated patterns offer a larger number of possible ratios, especially if one considers that resistors can connect in series as well as in parallel. Table 7.2 lists a number of additional interdigitation patterns. The patterns marked by asterisks do not provide complete alignment of the centroids. In all such cases, one can achieve full alignment by using a larger number of segments.

A	AA	AAA	AAAA
AB*	ABBA	ABBAAB*	ABABBABA
ABC*	ABCCBA	ABCBACBCA*	ABCABCCBACBA
ABCD*	ABCDDCBA	ABCDBCADBCDA*	ABCDDCBAABCDDCBA
ABA	ABAABA	ABAABAABA	ABAABAABAABA
ABABA	ABABAABABA	ABABAABABAABABA	ABABAABABAABABAABABA
AABA*	AABAABAA	AABAAABAAABA*	AABAABAAAABAABAA
AABAA	AABAAAABAA	AABAAAABAAAABAA	AABAAAABAAAABAAAABAA

TABLE 7.2 Sample interdigitation patterns for arrays having one axis of symmetry.

The process of designing an interdigitated array begins with the identification of all of the components comprising the array. Matched devices occur in groups, and all of the devices in any one group must reside in the same array. A designer cannot identify the groups of matched components in a circuit without fully understanding how the circuit operates. The circuit designer must therefore identify the groups of matched components and pass this information to the layout designer.

Once the components comprising an array have been identified, they must be divided into segments. This process is not always a simple one. The designer should first check to see if all of the values have a *greatest common factor.* For example, two resistors having values of 10kΩ and 25kΩ have a greatest common factor of 5kΩ. The array can then consist of a number of segments each equal to the greatest common factor. For example, an array of a 10kΩ and a 25kΩ resistor could be laid out using seven 5kΩ segments.

In cases where a large common factor does not exist, try using the value of the smallest device as the value of a segment. Based on this value, determine the number of segments in the other devices. If any device requires a partial segment with a value less than about 70% of a complete segment, try dividing the smallest device

value by increasingly large integer numbers (2, 3, 4 . . .) until a value is found that does not require a small partial segment. For example, suppose that a 39.7kΩ and a 144.5kΩ resistor must be arrayed. If we choose a segment resistance of 39.7kΩ, then the 144.5kΩ resistor would require 3.638 segments. This requires a 63.8% partial segment, so we divide the smaller resistance by two and try a segment resistance of 19.85kΩ. The larger resistor would need 7.280 segments, which would require a 28.0% partial segment. Dividing the smaller value by three produces a segment resistance of 13.233kΩ. The larger resistor would require 10.920 segments, so the array contains no partial segment that is less than 70% of a complete segment. This array could therefore consist of thirteen segments of 13.233kΩ and one segment of 12.174kΩ. In a few cases, this procedure produces a very small segment value. The designer should try larger segment values to see if one can be found that will allow all of the matched resistors to be constructed without using any partial segment that is less than about 70% of a complete segment. In certain cases, the designer may have to tolerate the presence of a small partial segment.

Once the segment value has been found, make sure that it is not so small that it precludes reasonable matching. Matched resistor segments should never contain less than five squares, and preferably they should contain at least ten. If the array seems to require short segments, consider using sections connected in parallel as well as in series. Capacitor segments (unit capacitors) should not have dimensions of much less than $100\mu m^2$. Capacitors are always connected in parallel because a series connection inserts parasitic capacitances that disturb matching. There are a few cases in which series-connected capacitors may form part of a set of matched capacitors, but such instances should stem only from the necessities of circuit design, not from the expediencies of layout.

Partial resistor segments are best implemented using sliding contacts to enable all of the segments to have exactly the same geometry. This precaution ensures that etch variations and diffusion interactions do not cause mismatches between the partial segment and the remainder of the array. The sliding contact can also be used to adjust the value of the partial segment should the initial setting prove incorrect. Partial unit capacitors should reside at one end of the array, where they will not unduly disturb the other unit capacitors. The partial unit capacitor should be sized using equations 7.7A and 7.7B to ensure that its area-to-periphery ratio equals that of the other unit capacitors.

Once the array has been segmented, a suitable interdigitation pattern must be chosen. The best interdigitation patterns obey all four rules of common-centroid layout listed in Table 7.3. The *rule of coincidence* states that the centroids of the matched devices should coincide at least approximately. Patterns that do not achieve coincidence exhibit larger stress sensitivities than those that do. The *rule of symmetry* states that the array should be symmetric around both axes. A one-dimensional array should derive one of its axes of symmetry from its interdigitation

1. ***Coincidence:*** The centroids of the matched devices should coincide at least approximately. Ideally, the centroids should exactly coincide.
2. ***Symmetry:*** The array should be symmetric around both the X- and Y-axes. Ideally, this symmetry should arise from the placement of segments in the array and not from the symmetry of the individual segments.
3. ***Dispersion:*** The array should exhibit the highest possible degree of dispersion; in other words, the segments of each device should be distributed throughout the array as uniformly as possible.
4. ***Compactness:*** The array should be as compact as possible. Ideally, it should be nearly square.

TABLE 7.3 The four rules of common-centroid layout.

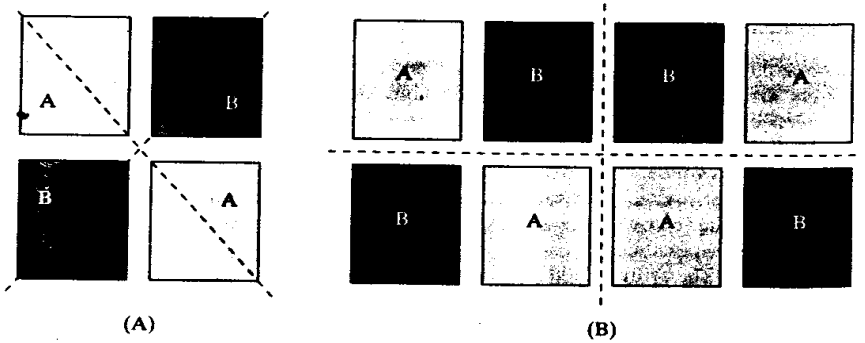
pattern. For example, an array using the pattern ABBA will have an axis of symmetry dividing it into two mirror-image halves (AB and BA). A one-dimensional array must rely on the symmetries of the individual segments to produce its second axis of symmetry. In the case of resistors and capacitors, this should not present a problem because all of the segments should have symmetric shapes.

The *rule of dispersion* states that the segments of each device should be distributed throughout the array as uniformly as possible. The degree of dispersion is often evident to the eye, but it can be partially quantified by counting the number of repeated segments (*runs*). For example, the pattern ABBAABBA contains three runs of two segments each, while the pattern ABABBABA contains only one run of two segments. The latter pattern is therefore more disperse than the former. Dispersion helps reduce the sensitivity of a common-centroid array to higher-order gradients (nonlinearities). Dispersion is therefore especially important for arrays subject to large stress gradients.

The *rule of compactness* states that the array should be as compact as possible. Ideally, it should be square, but in practice it can have an aspect ratio of 2:1 or even 3:1 without introducing any significant vulnerability. If the aspect ratio of the array exceeds 2:1, then consider breaking the array into a larger or smaller number of segments. If the array consists of a few long segments, try doubling the number of segments and halving the value of each. Arrays consisting of many short (or small) segments are excellent candidates for the two-dimensional arrays discussed below.

All of the common-centroid layouts discussed so far array the devices in only one dimension. Such a *one-dimensional array* derives one of its axes of symmetry from its interdigitation pattern and one of its axes of symmetry from the symmetry of its segments. The segments can also be arranged to form a *two-dimensional array* deriving both of its axes of symmetry from its interdigitation pattern. This type of arrangement generally provides better cancellation of gradients than one-dimensional arrays, primarily because of the superior compactness and dispersion possible within a two-dimensional array.

Figure 7.15A shows two matched devices, each composed of two segments arranged in an array of two rows and two columns. This arrangement is often called a *cross-coupled pair*. Resistors are rarely laid out as cross-coupled pairs because the resulting arrays usually have unwieldy aspect ratios. Capacitors often produce very compact cross-coupled pairs, as do diodes and transistors. If the matched devices are large enough to segment into more than two pieces, then the cross-coupled pair can be further subdivided as shown in Figure 7.15B. This array exhibits more dispersion than a cross-coupled pair and is therefore less susceptible to higher-order gradients. This two-dimensional interdigitation pattern, or *tiling*, can be indefinitely extended in both dimensions.



(A) (B)

FIGURE 7.15 Examples of two-dimensional common centroid arrays.

The rules for creating one-dimensional arrays also apply to two-dimensional arrays. The sections should be arranged so that the array has two or more axes of symmetry intersecting at the point where the centroids of the matched devices coincide. Table 7.4 lists a number of sample interdigitation patterns for two-dimensional arrays. Each row in the table consists of four examples of a given pattern. These include the simplest possible array, an extension of the array in one dimension, and extensions of the array in two dimensions. Although more complex variations are possible, most two-dimensional arrays are relatively simple because capacitors and transistors—the devices most often arrayed in two dimensions—do not lend themselves to subdivision into a large number of segments.

ABBA BAAB	ABBAABBA BAABBAAB	ABBAABBA BAABBAAB ABBAABBA	ABBAABBA BAABBAAB BAABBAAB ABBAABBA
ABA BAB	ABAABA BABBAB	ABAABA BABBAB ABAABA	ABAABAABA BABBABBAB BABBABBAB ABAABAABA
ABCCBA CBAABC	ABCCBAABC CBAABCCBA	ABCCBAABC CBAABCCBA ABCCBAABC	ABCCBAABC CBAABCCBA CBAABCCBA ABCCBAABC
AAB BAA	AABBAA BAAAAB	AABBAA BAAAAB AABBAA	AABBAA BAAAAB BAAAAB AABBAA

TABLE 7.4 Sample interdigitation patterns for two-dimensional common-centroid arrays.

Location and Orientation

Any residual stress sensitivities not canceled by common-centroid layout remain proportional to the magnitude of the stress gradient. Matched devices should therefore occupy areas of the die where the stress gradients are smallest. As Figure 7.11 suggests, the stress gradient typically falls to a minimum in a broad region near the center of the die. The best locations for matched devices are therefore near the middle of the die. The stress gradient along the periphery of the die reaches a similar broad minimum in the middle of each side, with the lowest values usually appearing in the middle of the longer sides. If matched devices must reside along the die periphery, then they are best located in the middle of one of the longer sides of the die. Matched components should never be placed near corners because both stress intensity and stress gradients reach their maximum values here.

The stress distribution on the surface of a die exhibits symmetries that can be exploited to further improve matching. Most dice exhibit a symmetric stress distribution around at least one axis. In the case of (100) silicon, the stress distribution is usually symmetric around both the horizontal and vertical axes. Critically matched common-centroid arrays should be oriented so that one of their axes of symmetry aligns with either the horizontal or the vertical axis of the die (Figure 7.16A).

The picture is less clear in the case of (111) silicon because one axis of symmetry of the die lies along a <110> axis while the other lies along a <211> axis (Figure 7.16B). Some authors have suggested that the stress distribution is more symmetric

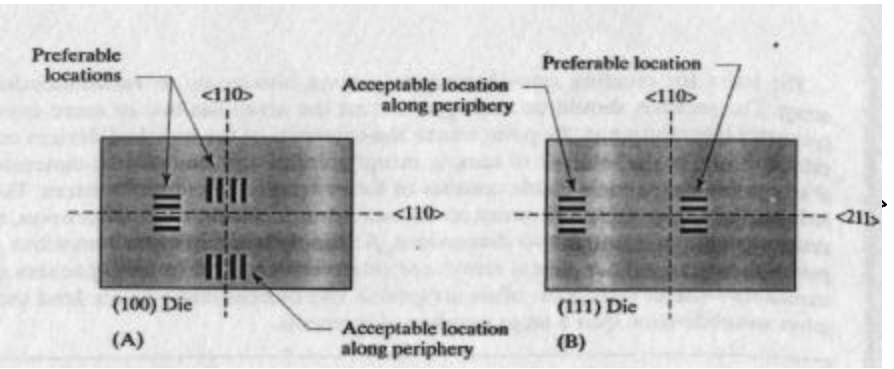


FIGURE 7.16 Locations for placing common centroid arrays on (100) and (111) dice, in the latter case assuming an axis of symmetry in the stress distribution around the <211> axis.

around the <211> axis than around the <110> axis,[19] so critically matched common-centroid arrays on (111) silicon should be oriented so that one of the axes of symmetry of the array aligns with the <211> axis of the die (Figure 7.16B).

The placement of the common-centroid array on an axis of symmetry of the stress distribution helps reduce residual mismatches by minimizing the stress gradient. If the stress distribution is symmetric around the chosen axis of symmetry, whatever stress-induced effects do occur will have opposite polarities on either side of this axis. Providing that the matched devices are also placed symmetrically around this same axis, the effects of stress on one half of the device will cancel the effects of stress on the other half. Whenever possible, critically matched devices should be placed to take advantage of this phenomenon.

The stress distribution on a die also depends on its size and shape. Larger dice generally exhibit higher levels of stress than small ones. Stress also tends to increase with aspect ratio, so elongated dice exhibit higher stress levels than square dice having similar areas. As previously mentioned, packaging also plays a major role in determining stress levels. Epoxy mounting provides mechanical compliance, which allows stresses to dissipate. Epoxy-mounted dice in metal cans or ceramic packages exhibit relatively little stress, regardless of die size or shape. The die area and aspect ratio become more important for parts encapsulated in plastic, or mounted with solder or gold eutectic. Table 7.5 offers some general guidelines for die aspect ratios in various types of packaging.

TABLE 7.5 Suggested die aspect ratios for analog layouts ($15kmil^2 \approx 9.7mm^2$).

Package Type	Die Size	Suggested Aspect Ratio	Maximum Aspect Ratio
Metal can/epoxy mount	Any	2:1 or less	Any
Plastic/epoxy mount	$<15kmil^2$	1.5:1 or less	3:1 or less
	$>15kmil^2$	1.5:1 or less	2:1 or less
Plastic/solder mount	$<15kmil^2$	1.5:1 or less	2:1 or less
	$>15kmil^2$	1.3:1 or less	1.5:1 or less

7.2.7. Temperature Gradients and Thermoelectrics

The electrical properties of many integrated components depend strongly on temperature. Most integrated resistors have temperature coefficients of 1000ppm/°C or more (Table 5.4). Assuming a temperature coefficient of 2500ppm/°C, a 1° temper-

[19] W. F. Davis, *Layout Considerations*, unpublished manuscript, 1981, pp. 66–67.

ature difference between two matched resistors produces a 0.25% mismatch. Thermal gradients of 1°C/mil (0.04°C/μm) can exist near a large power device.[20] To better understand how these thermal variations arise, we will briefly examine the concept of *thermal impedance.*

All electrical circuits dissipate some amount of power in the form of heat. This heat flows through the encapsulation out into the ambient environment. The average *junction temperature* of the die T_j equals

$$T_j = T_a + P_d\theta_{ja} \qquad [7.9]$$

where T_a is the ambient temperature of the environment, P_d is the power dissipated in the package, and θ_{ja} is a constant called the *junction-to-ambient thermal impedance.* The θ_{ja} for most plastic packages exceeds 100°C/W, limiting their power dissipation to about a watt. Specially constructed power packages exist that offer much lower thermal impedances (Table 7.6). These packages usually incorporate a metal tab or plate intended for mounting onto an external metal surface called a *heat sink.* Power packages are usually specified in terms of a *junction-to-case thermal impedance,* θ_{jc}. In this case, the average junction temperature, T_j, equals

$$T_j = T_c + P_d\theta_{jc} \qquad [7.10]$$

where T_c represents the case temperature of the package measured at a specified point on the heat tab or plate. Power packages often have remarkably low thermal impedances because of their special construction. Various manufacturers cite slightly different values due to variations in materials and manufacturing processes, but the values listed in Table 7.6 are representative of the industry.

TABLE 7.6 Typical thermal impedances for several common types of packages.[21]

Type of package	θ_{ja} (°C/W)	θ_{jc} (°C/W)
16-pin plastic dual in-line package (DIP)	110	
16-pin plastic surface-mount package (SOIC)	131	
3-lead plastic TO-220 power package		4.2
3-lead metal TO-3 can power package		2.7

One might expect the packages with the lowest thermal impedances to have the smallest thermal gradients, but in practice the exact opposite occurs. Power packages achieve their low thermal impedances by mounting the die on a heat sink. Heat flows vertically down to the heat sink and out of the package, rather than laterally across the die. Temperatures rise only where power is dissipated; other portions of the die remain at approximately the same temperature as the heat sink. Temperature differentials of up to 50° can appear across the surface of a die mounted in a power package; the thermal gradients are correspondingly large.

A package lacking a heat sink presents a very different picture. Silicon is a far better conductor of heat than epoxy, so heat flows laterally across the die until the entire die rises to a high temperature. Heat then percolates out from the die through

[20] See Figure 1 in R. J. Widlar and M. Yamatake, "Dynamic Safe-Area Protection for Power Transistors Employs Peak-Temperature Limiting," *IEEE J. Solid-State Circuits.* Vol. SC-22, #1, 1987, pp. 77–84.

[21] Values for 16-pin dip, 16-pin SOIC: *Power Supply Circuits Databook;* Texas Instruments #SLVD002, 1996, pp. 4–22. Values for TO-3, TO-220: *Power Products Data Book,* Texas Instruments #DB-029, 1990, pp. 4–72, 5–8. These values are broadly representative of the industry.

the plastic to the outside environment. The plastic package acts as a thermal insulation blanket that minimizes the magnitude of thermal gradients. Ordinary plastic packages rarely experience thermal differentials of more than a few degrees across the die unless the power dissipation of the circuit rapidly fluctuates.

Figure 7.17 shows an *isothermal contour plot* for a die containing one large heat source mounted in a power package. The curved lines on the surface of the die, called *isotherms*, represent adjacent points of equal temperature. Each isotherm represents a relatively large change in temperature, perhaps five degrees. The same general distribution of isotherms would also occur on a die in an ordinary plastic package, but the average die temperature would be much higher and the isotherms would represent smaller changes in temperature—perhaps one degree per isotherm.

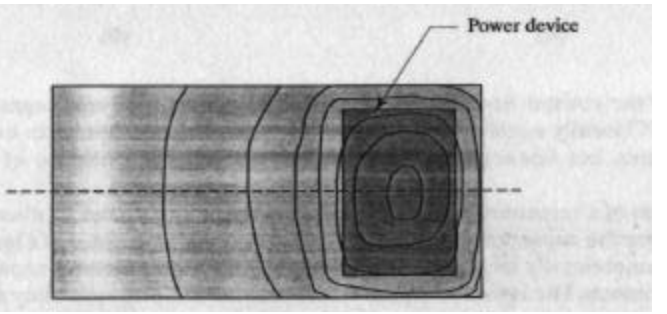


FIGURE 7.17 Isothermal contour plot of a die having only one major heat source. The axis of symmetry of the thermal distribution is marked by a dotted line.

The thermal gradients are largest around the perimeter of the power device and gradually decrease in magnitude as one moves away from it. Because the heat source has been placed symmetrically around the horizontal axis of the die, the heat distribution is also symmetric about this axis. The presence of this axis of symmetry can be used to improve the thermal matching of other components on the die.

Thermal Gradients

The relative spacing of the isotherms reflects the thermal gradient at each point on the die. The thermal gradient is large where the isotherms are spaced closely together, and it is small where they are spaced far apart. Thermal gradients are exactly analogous to the stress gradients discussed in the previous section. Assuming that the thermal gradient remains approximately constant in the vicinity of a pair of matched devices, then the thermally induced mismatch δ_T between the two devices equals

$$\delta_T = TC_1 d_{cc} \nabla T_{cc} \qquad [7.11]$$

where TC_1 is the linear temperature coefficient of the resistance material, d_{cc} is the distance between the centroids of the resistors, and ∇T_{cc} is the thermal gradient along a line connecting the centroids of the resistors.

Although common-centroid layouts are used to combat both stress and thermal gradients, their position and orientation differ depending on the application. The axes of symmetry of stress distributions are determined entirely by the packaging and therefore present rigid constraints on the layout. The axes of symmetry of thermal distributions are determined by the position and orientation of the power devices. The magnitude of thermally induced variations can be minimized by proper placement of the matched devices relative to the power devices.

Most dice contain only a few major heat sources, which are usually large bipolar or MOS power transistors. Whenever possible, these devices should lie upon an axis of the die in order to produce a symmetric thermal distribution. They should also lie

as far as possible from critical matched devices. Consider the case of a die containing one power device (Figure 7.18A). This power device would ideally occupy one end of the die and align around an axis of symmetry of the die. This arrangement is preferable to placing the power device centrally because it allows more separation between the power device and critical matched devices. The placement of the matched devices is a compromise between stress effects—which favor a central location—and thermal effects—which favor placement as far away from the power device as possible. The optimal arrangement places the matched devices about halfway across the portion of the die not occupied by the power transistor (Figure 7.18A). A larger separation between the power device and the matched pair can sometimes be achieved by elongating the die to an aspect ratio of 1.3 or even 1.5. Although elongation increases stress levels, the improvement in matching due to increased separation may actually outweigh the effect of increased stresses. If matched devices must reside along the periphery of the die, then they should occupy the middle of the side opposite the power device. In this case, the aspect ratio of the die should be moderated to limit the effects of stress on the less-optimal location of the matched devices. Although the effects discussed above are difficult to quantify, the arrangements advocated here have been successfully used on many designs.

The layout of Figure 7.18A can easily be extended to incorporate two power transistors instead of one. Ideally the transistors would be placed one behind another, both at one end of the die and both on the same axis of symmetry (Figure 7.18B). This yields a layout resembling that of Figure 7.18A. Unfortunately, this arrangement often produces difficulties in routing the leads from the power devices to their respective pins. Many designs place the two power devices in adjacent corners of the die located on the opposite end from the matched devices. This arrangement has the advantage of separating the heat sources from the matched devices by the largest possible distance. However, the disadvantage is that the heat distribution is now asymmetric unless the devices operate at identical power levels. Another possible layout for two heat sources is shown in Figure 7.18C. This arrangement places one power device on each end of the die and the matched devices in the middle. This arrangement will probably prove satisfactory as long as a separation of at least 20 to 30mils can be achieved. It has the advantage of preserving a thermal axis of symmetry regardless of the dissipation levels in the individual power devices, and it locates the matched devices in the center of the die where the stress gradients are lowest.

The layout of Figure 7.18C can be extended to include additional devices. Figure 7.18D shows an example containing four power devices. This arrangement usually suffers from a lack of separation between the power devices and the matched devices. This problem can be partially remedied by increasing the aspect ratio of the die to 1.5:1 or even 2:1. Even a large aspect ratio will not necessarily affect matching because the power devices occupy the ends of the die where the stresses are greatest. Aspect ratios larger than 1.5:1 are somewhat risky for solder or gold eutectic mounting if the die's longer dimension exceeds 150 mils (3.8mm). The stresses accumulating in the corners of such a long die may actually cause mechanical damage to the metal system or the bond wires. Epoxy die mounting provides additional mechanical compliance and therefore allows larger aspect ratios.

A variety of considerations often constrain the placement of power devices. These include the location of bondpads, the routing of power buses and the placement of control circuitry. The compromises required to satisfy all of these constraints usually lead to a less-than-optimal layout. This does not necessarily constitute an insurmountable problem because common-centroid layout techniques can greatly reduce the impact of the remaining thermal mismatches.

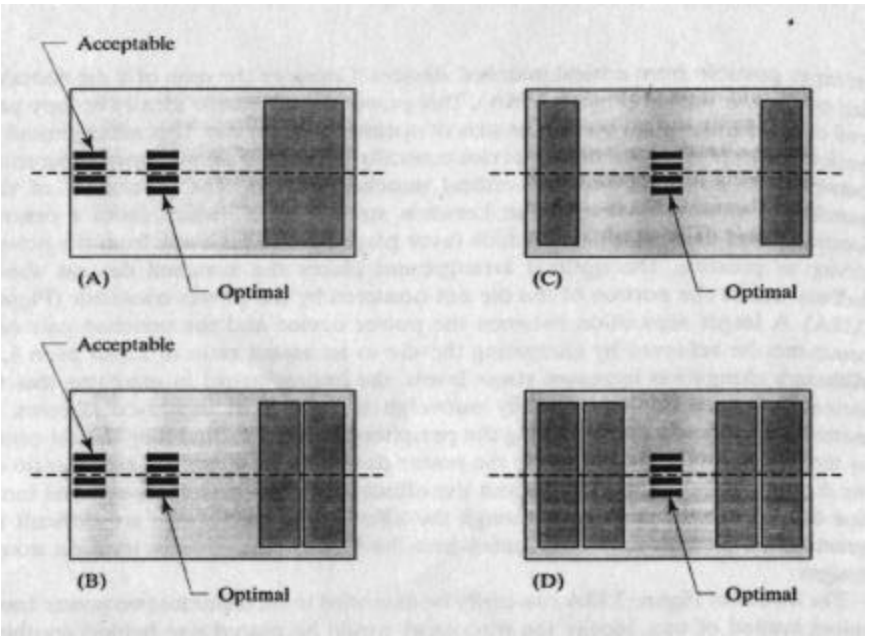


FIGURE 7.18 Various arrangements of one, two, and four power devices for optimal thermal matching. The power devices are shown as dark gray rectangles, and the axes of symmetry created by their placement are shown as dotted lines.

Thermoelectric Effects

Resistors display two distinct types of thermal variation. One is caused by the temperature coefficient of the resistance material. Common-centroid layout techniques can ensure that the average temperatures of two resistors track one another, so even materials with large temperature coefficients will match quite precisely. The other source of thermal variation is the *Seebeck effect*, also called the *thermoelectric effect*. As discussed in Section 1.2.5, a voltage differential called the *contact potential* arises whenever two dissimilar materials come in contact with one another. The contact potentials of metal/semiconductor junctions are strong functions of temperature, so if the contacts are held at different temperatures, a net voltage difference will appear across the resistor. This *thermoelectric potential* E_T equals

$$E_T = S\Delta T_c \qquad [7.12]$$

where S is the *Seebeck coefficient* (typically about 0.4mV/°C), and ΔT_c is the temperature difference between the two contacts of the resistor. A temperature difference of 1° across a resistor will thus generate a voltage differential of about 0.4mV between its contacts. This may appear inconsequentially small, but certain types of circuitry are extremely vulnerable to small voltage offsets. For example, a 0.4mV offset in a bipolar current mirror produces a 1.5% mismatch in the currents.

Common-centroid layout cannot eliminate thermoelectrics because they arise from differences in temperature between the ends of each resistor segment. Improperly arraying the device actually compounds the problem. The individual thermoelectric potentials generated by each segment of the resistor array of Figure 7.19A add to produce an overall thermoelectric potential far larger than that of any one segment. The thermoelectric potentials of the individual segments can be canceled by reconnecting them as shown in Figure 7.19B.

In order to obtain complete cancellation, the resistor should consist of an even number of segments, half connected in one direction and half connected in the other

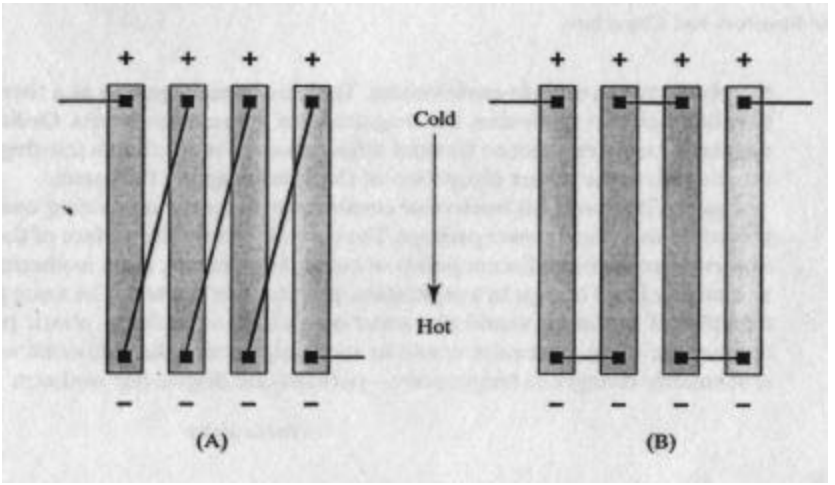


FIGURE 7.19 (A) Improper connection of resistor segments causes their thermoelectric potentials to add, while (B) proper connection of the segments cancels the thermoelectrics.

(Figure 7.19B). If the resistor has an odd number of segments, then one segment cannot be paired. Critically matched resistors should, if possible, consist of an even number of segments, but less-sensitive resistors can tolerate the presence of an unpaired segment.

The two contacts of a serpentine resistor should reside as close to one another as possible to minimize the impact of thermoelectrics. The serpentine resistor of Figure 7.20A will have unnecessarily large thermal variations due to an excessive separation between its contacts. The layout of Figure 7.20B reduces thermal variability and improves matching by bringing the resistor heads into closer proximity. However, this layout is vulnerable to misalignment errors. If the resistor body shifts downward relative to the resistor heads, then the length of the resistor increases by twice the misalignment. This vulnerability can be eliminated by orienting the resistor heads in opposite directions, so that any shift that increases the length of the resistor protruding from one head reduces the length protruding from the other. The layout of Figure 7.20C eliminates the misalignment vulnerability, but it places the base heads adjacent to stretches of the resistor body, which can lead to diffusion interactions. It is difficult to eliminate this minor defect without introducing more serious problems in the process.

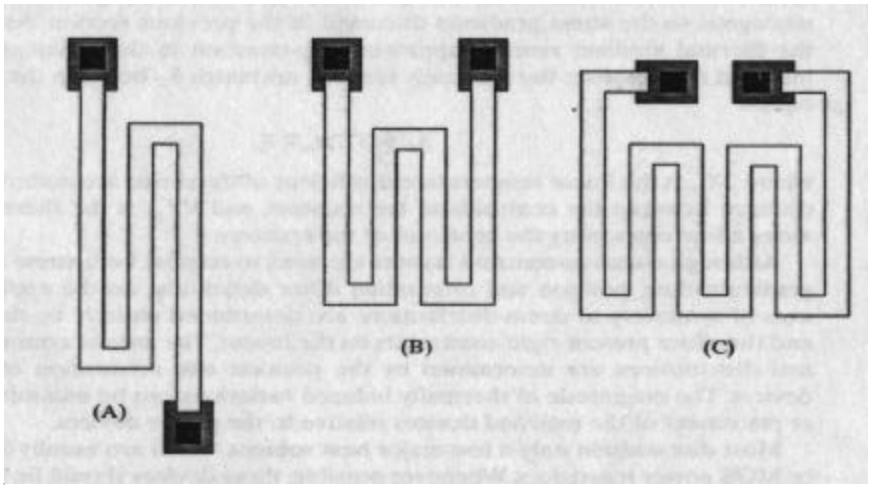


FIGURE 7.20 An HSR resistor with widely separated contacts (A) is prone to thermoelectric-induced offsets. Placing the contacts close together (B) minimizes thermoelectrics, but may increase variation due to misalignment. Placing the contacts close together and oriented in opposite directions (C) fixes both problems.

7.2.8. Electrostatic Interactions

Electrostatic fields can influence the value of both resistors and capacitors. An electrostatic field can cause depletion or accumulation of carriers within a resistive material. Most integrated resistors consist of lightly doped silicon and are therefore quite susceptible to voltage modulation. The electrostatic coupling of a capacitor to surrounding circuitry via fringing fields can cause unexpected variations in capacitance. Electrostatic fields can also couple noise into sensitive high-impedance nodes that often exist within arrays of matched resistors and capacitors.

The principal types of electrostatic interactions observed in resistors are voltage modulation, charge spreading, and dielectric polarization. The major electrostatic interactions in capacitors are fringing fields and dielectric relaxation. The following sections cover each of these mechanisms.

Voltage Modulation

The value of a resistor can be affected by the voltages present on adjacent nodes of the circuit. The value of a diffused resistor may vary with the voltage differential between the tank and the resistor body, an effect called *tank modulation* (Section 5.3.3). The mismatches caused by tank modulation in two or more diffused resistors cancel as long as the tank-to-body voltages of the resistors track one another. Matched resistors can safely reside in a common tank as long as they are of equal values and they experience the same bias. Otherwise, each resistor should occupy its own tank. The individual tanks must connect so that each resistor sees the same tank-to-body differential voltage. This is most easily accomplished by tying the positive end of each resistor to its respective tank. If the resistors are of different values, they all must be divided into segments of equal (or approximately equal) value, and each segment must reside in its own independently biased tank. Similarly, each section of an interdigitated resistor requires its own tank (Figure 7.21).

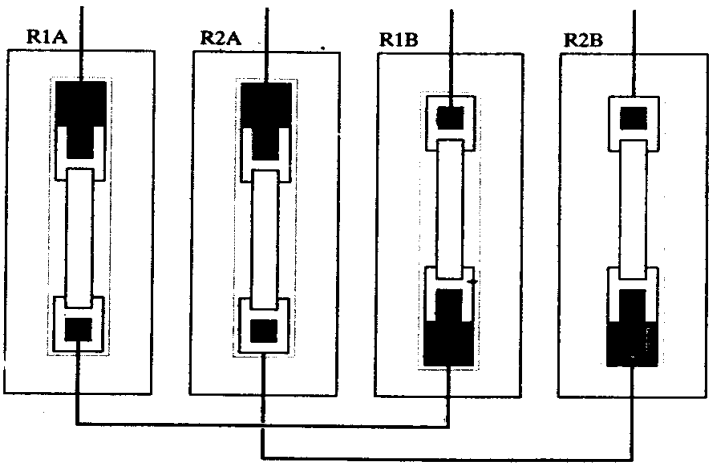


FIGURE 7.21 Two HSR resistors connected in order to cancel both thermoelectrics and tank modulation effects.

Separate tanks require enormous amounts of die area. Poly or thin-film resistors will surely provide a more compact solution. If deposited resistors are not available, consider whether the circuit can tolerate a small amount of voltage modulation. If the voltage across the matched resistors is directly (or even indirectly) trimmed, this may also compensate for voltage modulation. This is often the case for voltage references and regulators. The matched resistors should still be interdigitated to prevent thermal and stress gradients from causing package shifts and thermal drifts.

Many applications can tolerate a small amount of voltage modulation. The magnitude of the resulting systematic mismatches can be minimized by using relatively low-sheet diffusions, such as base or emitter, rather than high-sheet diffusions, such as HSR. For example, the voltage modulation of 160Ω/□ base equals about 0.1%/V while that of 2kΩ/□ HSR can approach 1%/V. Matched base resistors are usually merged into a common tank to save space, while matched HSR resistors frequently require separate tanks.

The proper determination of tank biasing requires a complete understanding of circuit specifications and design, so the circuit designer rather than the layout designer must determine the tank connections. These should appear on the schematic along with the type of resistance material required, the width of the resistor, and any special matching requirements. In cases where the connections of the resistors are not obvious, or appear to be in error, the layout designer should verify them before continuing.

Leads routed over resistors can also affect their operation. As a rule, leads that do not connect to matched resistors should not cross them. Not only may these leads capacitively couple noise into the resistor, but the electric field between the lead and the resistor can actually modulate the conductivity of the resistance material (a phenomenon called *conductivity modulation*). Emitter, base, and low-sheet poly ($R_s < 200\Omega/\square$) resistors rarely experience significant conductivity modulation. High-sheet resistors are more problematic; for example, metal-1 over 2kΩ/□ HSR can produce 0.1%/V of conductivity modulation. The impact of conductivity modulation depends on three factors: (1) the voltage difference between the lead and the underlying resistor, (2) the thickness of the intervening oxide, and (3) the area of intersection. A lead connected to an HSR resistor can safely route across the end of the resistor next to the head, while one routed entirely across the resistor array may cause problems because it has a larger area of intersection. Wires rarely need to route across resistors in a double-level metal process, but jumpers through resistor arrays are often unavoidable in single-level metal processes. For example, the interdigitated HSR resistor array shown in Figure 7.22 uses a jumper between segments R_{1A} and R_{1B} to allow a lead to exit from the left-hand terminal of R_2.

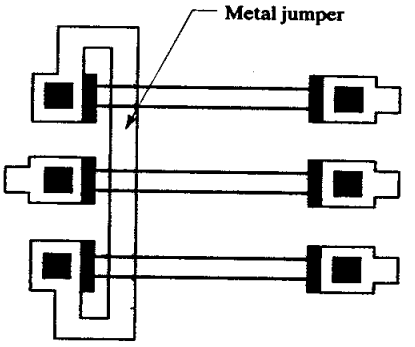


FIGURE 7.22 Portion of an interdigitated HSR array implemented in a single-level metal process showing the placement of a jumper between segments.

The jumper of Figure 7.22 is constructed so that it intersects each resistor segment in exactly the same manner. This precaution helps to minimize the mismatches produced by the stress of the aluminum lead on the underlying resistor.[22] Still,

[22] For a discussion of a similar stress-induced mismatch mechanism in MOS transistors, see H. Tuinhout, M. Pelgrom, R. P. de Vries, and M. Vertregt, "Effects of Metal Coverage on MOSFET Matching," *IEDM*, 1996, pp. 735–738.

the mere presence of a lead running over the resistor segments implies that stresses are imposed on the resistors, and therefore produces an inevitable degradation of matching. Whenever possible, one should not route any leads across critically matched resistors.

A more convenient or more compact layout often results if leads can cross resistors. A technique called *electrostatic shielding* (or *Faraday shielding*) can isolate a resistor from the influence of overlying leads. Electrostatic shielding not only prevents conductivity modulation but also provides considerable shielding against capacitive coupling.

Figure 7.23A illustrates the basic concept of an electrostatic shield. The shield is interposed between the two conductors—in this case the resistor and an overlying lead. The electrostatic interactions between the shield and the conductors on either side can be modeled as a pair of series-connected capacitors (Figure 7.23B). The AC voltage source, V_N, represents the time-varying voltage present on the overlying lead. Noise injected by V_N is attenuated by the RC filter formed by C_{P1} and R_1, where C_{P1} represents the capacitance between the overlying lead and the shield, and R_1 represents the resistance of the connection between the shield and AC ground. Whatever noise passes through C_{P1}–R_1 will be injected through C_{P2} onto R_2, where C_{P2} represents the capacitance between the shield and the sensitive node, and R_2 represents the resistance between the sensitive node and AC ground. The attenuation provided by the shield falls away with increasing frequency. Providing that the shield connects to a clean low-impedance node (such as signal ground), substantial attenuation may remain into the low RF region (1 to 10 MHz). At higher frequencies, it becomes increasingly difficult to guarantee a sufficiently low-impedance shield connection, so high-speed digital signals should not route across sensitive circuitry even if an electrostatic shield is present.

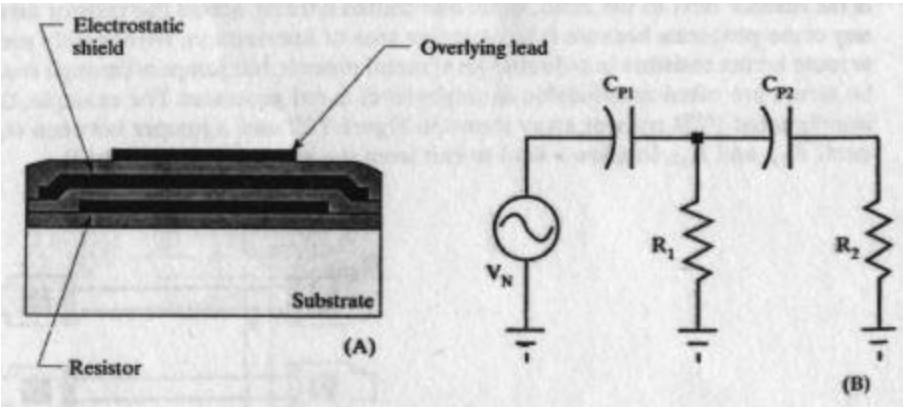


FIGURE 7.23 The concept of an electrostatic shield: (A) cross section and (B) equivalent circuit.

Figure 7.24 shows a practical example of an electrostatic shield. The poly resistor array includes dummies at either end, and both the shield and the dummies are connected to ground. Leads can cross the shielded resistors without modulating the conductivity of the poly resistors or injecting noise into them. Note that a fringing field exists around any conductor. In order to prevent this fringing field from coupling around the shielding, all leads should reside well away from the edges of the shield. An overhang of 5μm (shield-over-conductor) will intercept the majority of the fringing fields. Since metal can elastically deform, the electrostatic shield may also help minimize stresses generated in the poly resistors by the presence of the second-metal leads running across them.

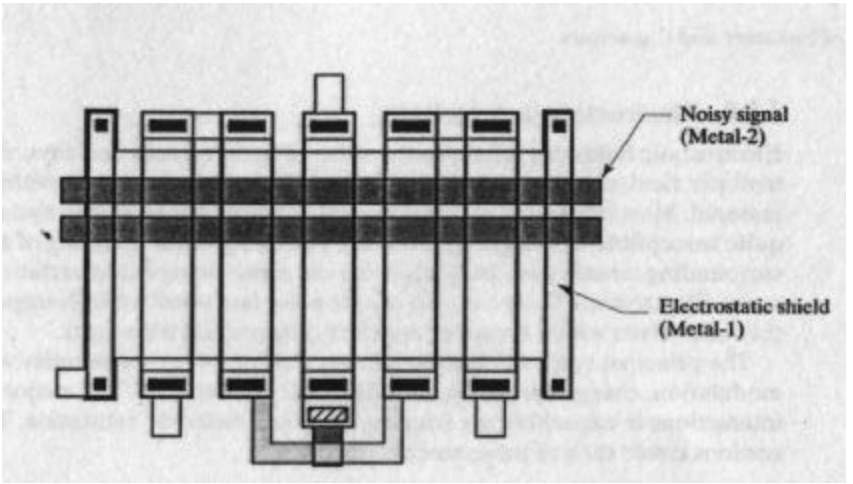


FIGURE 7.24 Example of electrostatic shielding applied to a matched poly resistor array.

Note that the electrostatic shield of Figure 7.24 covers the entire resistor array. Each resistor segment in the array sees a slightly different voltage. As long as the voltage difference across the array remains small and the sheet resistance of the resistors is less than about 500Ω/□, a common shield will suffice. If the resistors consist of high-sheet material, or if the voltage differential across the array exceeds a few volts, then the common electrostatic shield itself will cause objectionable conductivity modulation! In such cases, the shield should be divided into individual sections placed over each resistor segment. Each shield must overlap its respective resistor by several microns (after accounting for misalignment and outdiffusion) to ensure that fringing fields do not degrade its effectiveness. Sectioned shielding requires substantially more space than common shielding.

The substrate can also inject noise into deposited resistors and capacitors. One way to minimize this source of noise coupling consists of placing a well beneath the devices and connecting this well to an AC ground. Resistors and capacitors that are especially sensitive to noise can benefit from a combination of electrostatic shields above and below them.[23] A deep-N+ sinker placed beneath deposited devices and connected to an AC ground can provide electrostatic shielding while minimizing parasitic capacitance (by thickening the field oxide through dopant-enhanced oxidation).

Charge Spreading

The mechanisms behind charge spreading were discussed at length in Section 4.3.2. Briefly, circuit operation injects electrons into the oxide overlying the die. Although most of these electrons eventually return to the silicon, a few become trapped at the interface between the interlevel oxide and the protective overcoat, or between the protective overcoat and the mold compound. These electrons constitute a mobile charge capable of varying resistor values through conductivity modulation. The electric field required to cause a fractional-percent variation of a high-sheet resistor is an order of magnitude smaller than that required to invert the surface of the silicon. Matched high-sheet resistors are therefore extremely susceptible to long-term drifts caused by charge spreading. Base resistors are much less susceptible to charge

[23] K. Yamakido, T. Suzuki, H. Shirasu, M. Tanaka, K. Yasunari, J. Sakaguchi, and S. Hagawara, "A single-chip CMOS filter/CODEC," *IEEE J. Solid-State Circuits*, Vol. SC-16, 1981, pp. 302–307.

spreading due to their lower sheet resistance, and only precisely matched base resistors are significantly affected. High voltages, moisture, and mobile ion contamination amplify the effects of charge spreading. Designs that operate at voltages exceeding half of the thick-field threshold or that are fabricated on standard bipolar should be examined for potential charge spreading vulnerabilities.

Electrostatic shielding can minimize or even eliminate the effects of charge spreading on matching. The electrostatic shield also serves as a field plate, counteracting surface inversion across high-voltage tanks. The field plate must connect to a potential not greatly different from the tank bias, as described in Section 4.3.2. It is often connected to the more positive end of the resistor. Field plates may actually increase noise coupling into high-impedance resistors due to leads running above the field plate or due to fringing fields from adjacent components. Noisy signals must not be routed across field plates unless the field plates connect to low-impedance nodes that are relatively insensitive to capacitive coupling.

Figure 7.25 shows the same resistor array as Figure 7.21. Each resistor segment has been provided with an individual field plate protecting it against the effects of charge spreading. The field plates flange over the bodies of the resistors far enough to prevent channel formation. The gaps in the field plates have not been channel-stopped because the proximity of an adjacent diffusion could cause diffusion interactions. If channel stops are required, they should be carefully replicated on each section so that all of the resistors experience the same interactions. In most cases, channel stops are unnecessary as long as the field plates are properly flanged. Although diffused HSR resistors can rival the matching of deposited resistors, the area required for separate tanks and field plates makes them rather uneconomical.

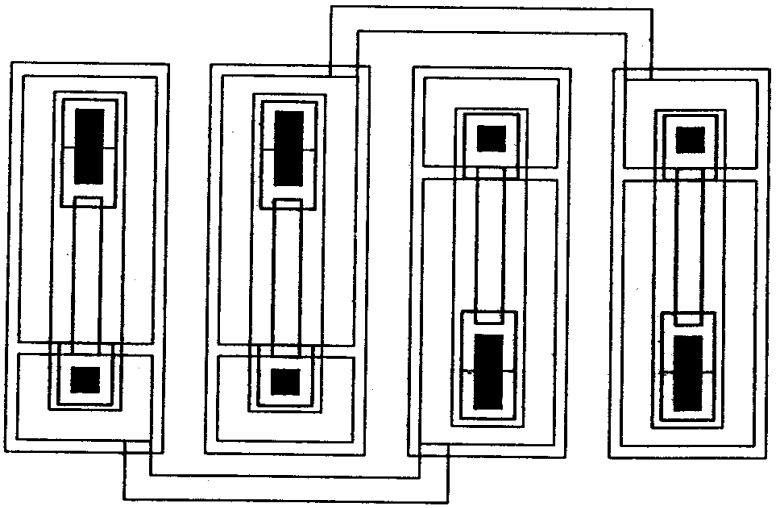


FIGURE 7.25 HSR resistor array, field-plated to minimize charge spreading. With the exception of its metallization pattern, this array matches the one in Figure 7.21.

Dielectric Polarization

Electrostatic fields can also arise due to the movement of charges within an insulator, a phenomenon called *dielectric polarization.* Oxides contaminated by alkali metal ions such as sodium or potassium exhibit a large degree of polarizability due to the mobility of these ions within the oxide. As discussed in Section 4.2.2, these *mobile ions* slowly redistribute themselves under the influence of external electrical fields. The electric field seen at the surface of the silicon shifts over time as the

mobile ions gradually assume a new configuration. If the external field suddenly vanishes, the new distribution of mobile ions generates a weak residual electric field oriented in the opposite direction to the original. This residual field gradually relaxes as the mobile ions return to their original distribution. The slow variation in field intensity seen beneath the oxide can modulate the value of a high-sheet resistor. The resulting *long-term drifts* are extremely undesirable.

The addition of phosphorus to silicon dioxide effectively immobilizes alkali metal ions, presumably through a sequestration mechanism involving phosphate groups. Phosphosilicate glass (PSG) thus exhibits much less polarization when contaminated with alkali metal ions than does pure oxide. Unfortunately, the phosphate groups themselves are slightly polarizable.[24] Phosphosilicate and borophosphosilicate glasses are subject to low levels of dielectric polarization in the presence of external electrical fields, and this in turn gives rise to hysteretic voltage modulation.

Dielectric polarization normally affects only high-sheet resistors. The polarization rates are usually far too slow to affect capacitors, and the resulting fields are too weak to affect resistors with sheets of less than about 500Ω/□. A dielectric polarization of approximately 0.1% has been observed in 2kΩ/□ high-sheet resistors constructed on a standard bipolar process using heavily phosphorus-doped BPSG.[25]

As the above example suggests, field plating is not a panacea for dielectric polarization. Field plates may actually intensify the phenomenon because they induce a deliberate electric field across the interlevel oxide. On the other hand, leaving the field plates off the resistors renders them vulnerable to charge spreading. This dilemma is best solved by avoiding the use of high-sheet resistors entirely. If this is impractical, then *split field plates* should be used. Figure 7.26 shows an example of a split field plate applied to a pair of matched high-sheet resistors similar to those shown in Figure 7.25.

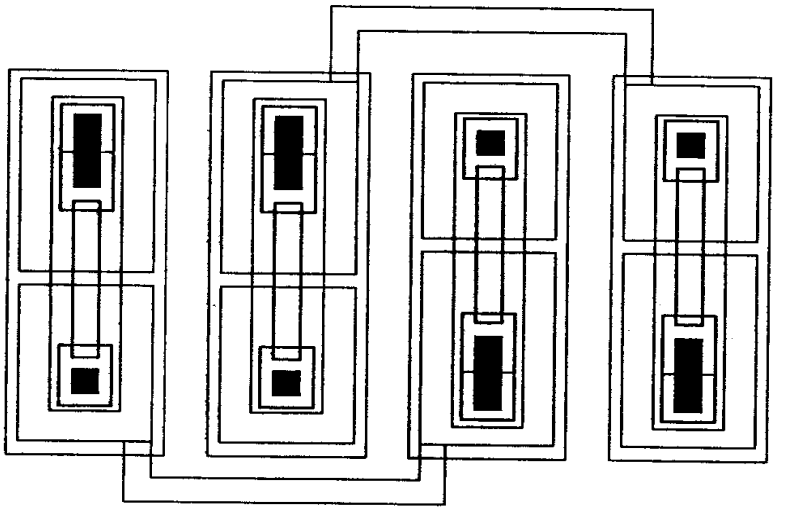


FIGURE 7.26 HSR resistor array field-plated to minimize dielectric polarization as well as to charge spreading and thermoelectrics (compare with Figure 7.25).

[24] E. H. Snow and B. E. Deal, "Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon," *J. Electrochem. Soc.*, Vol. 113, #3, 1966, pp. 263–269.

[25] F. W. Trafton, private communication.

Split field plates differ from conventional field plates in the location of their gaps. In a conventional field plate, as much of the plate as possible connects to the positive end of the resistor to offer maximum protection against surface inversion. In a split field plate, each resistor segment requires two field plates, one connecting to either end of the resistor. The gap between the two plates falls in the exact center of the resistor. The split field plate subjects half of the resistor to an electric field equal and opposite to that seen by the other half. The dielectric polarization in each half of the resistor exactly cancels the polarization in the other. Split field plates also reduce voltage nonlinearity effects caused by the field plates, because the accumulation effects beneath one plate balance the depletion effects under the other.[26] Split field plates can be applied to resistors occupying a common tank, but each segment must have its own split field plate.

Split field plates are recommended for all applications where resistors having sheet resistances in excess of 1kΩ/□ must match to better than ±0.5%. Split field plates are not necessary for base resistors since the lower sheet resistance of this diffusion generally renders dielectric polarization negligible. They are likewise not necessary for the majority of polysilicon resistors because these usually exhibit sheet resistances less than or equal to 1kΩ/□.

Dielectric Relaxation

Capacitors are also susceptible to dielectric polarization in the form of a hysteretic effect called *dielectric relaxation* or *soakage*. Suppose that the capacitor is suddenly charged to produce a corresponding electric field between its electrodes. As the dielectric polarizes, the electric field intensity gradually decreases (or *relaxes*) to a lower value. The relaxation of the electric field causes a corresponding droop in capacitor voltage. After the capacitor is suddenly discharged and then disconnected, the polarization dissipates and a reverse bias gradually accumulates across the capacitor. Charge storage capacitors (such as those used in timers and sample-and-hold circuits) are especially intolerant of dielectric relaxation errors.

Charge spreading can affect capacitors in much the same manner as dielectric polarization. When the capacitor is charged, the shifting electrostatic fields cause a gradual redistribution of charges along insulating interfaces. This results in a change in the electric field intensity that is similar to what occurs in dielectric relaxation. Charge spreading can occur along the interfaces of a composite dielectric, such as the oxide-nitride-oxide sandwich used to fashion ONO capacitors. The movement of charges along the interfaces of the capacitor dielectric can occur very rapidly, so variations in capacitor value may occur at frequencies in excess of 1MHz.

High-quality oxide dielectrics are preferred for critically matched capacitors, particularly for those that operate at high frequencies. The use of a grown oxide dielectric usually reduces dielectric relaxation to negligible levels.[27] Charge spreading and polarization phenomena arising outside the capacitor structure can be eliminated using electrostatic shielding. Figure 7.27 shows one method of shielding a poly-poly

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[26] J. Victory, C. C. McAndrew, J. Hall, and M. Zunino, "A Four-Terminal Compact Model for High-Voltage Diffused Resistors with Field Plates," *IEEE J. Solid-State Circuits*, Vol. 23, #9, 1998, pp. 1453–1458.

[27] LPCVD oxides also exhibit little dielectric relaxation, but the same is not true of TEOS oxides: J. W. Fattaruso, M. De Wit, G. Warwar, K. S. Tan, and R. K. Hester, "The Effect of Dielectric Relaxation on Charge-Redistribution A/D Converters," *IEEE J. Solid-State Circuits*, Vol. 25, #6, 1990, pp. 1550–1561.

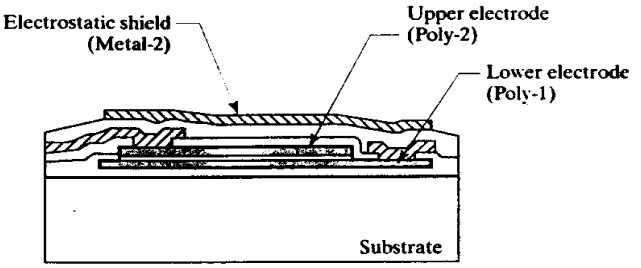

FIGURE 7.27 Cross section of a poly-poly capacitor incorporating an electrostatic shield plate. Note the overlap of the electrostatic plate over the upper electrode.

capacitor. The sensitive high-impedance node connects to the upper electrode of the capacitor. An electrostatic shield constructed from second-level metal completely covers the upper electrode. This electrostatic shield connects to the lower electrode of the capacitor to form a sandwich-capacitor structure. The sensitive node is now entirely enclosed within an electrostatic shield. Both the lower capacitor electrode and the electrostatic shield should overhang the upper capacitor electrode by at least 3 to 5μm to suppress fringing fields. This structure is relatively insensitive to dielectric polarization and charge spreading providing that both the capacitor oxide and the interlevel oxide above the upper electrode are not phosphorus-doped.

7.3 RULES FOR DEVICE MATCHING

The previous sections have discussed the various mechanisms responsible for causing mismatches. This information would ideally be used to formulate a set of quantitative rules for each process. The layout designer could then apply these rules to obtain matched devices of any desired degree of accuracy. In practice, the time and effort required to generate quantitative matching rules are usually prohibitive. This section therefore presents a set of qualitative rules applicable to many processes. In the absence of more precise matching data, these rules can be used to lay out structures with at least a modest degree of confidence.

The following rules employ the terms *minimal, moderate,* and *precise* to denote increasingly precise degrees of matching. These terms have the following meanings:

- **Minimal Matching:** Approximately ±1% three-sigma mismatch, or 6 to 7 bits of resolution. Suitable for general-purpose use, such as for degenerating current mirrors in biasing circuitry.
- **Moderate Matching:** Approximately ±0.1% three-sigma mismatch, or 9 to 10 bits of resolution. Suitable for ±1% bandgap references, op-amp and comparator input stages, and most other analog applications.
- **Precise Matching:** Approximately ±0.01% three-sigma mismatch, or 13 to 14 bits of resolution. Suitable for precision A/D and D/A converters and for all other applications requiring extreme precision. Capacitors can more easily obtain this level of matching than resistors.

7.3.1. Rules for Resistor Matching

Minimal matching can be obtained without much difficulty, and moderate matching can be reliably obtained using interdigitation. Precisely matched resistors are difficult to construct due to variations in contact resistance and the presence of thermal

and stress gradients. The following rules summarize the most important principles of resistor design:[28]

1. Construct matched resistors from a single material.
   Resistors constructed from different materials do not even approximately match one another. Process variations will cause unpredictable shifts in the value of one resistor relative to the other, and the differing temperature coefficients of the two materials prevent them from tracking over temperature. *Do not construct matched resistors from different materials!*
2. Make matched resistors the same width.
   Uncorrected process biases will cause systematic mismatches in resistors of different widths. If for some reason one resistor must be made wider than another, consider constructing the wider resistor from a number of sections connected in parallel. Width effects are not entirely independent of temperature and stress, so even if moderately or precisely matched resistors are trimmed, they should still consist of sections of a uniform width.
3. Make matched resistors sufficiently wide.
   In the absence of experimental data, assume that minimal matching of resistors containing 30 or more squares requires 150% of the minimum allowed width of the deposition or diffusion, moderate matching requires 200%, and precise matching requires 400%. For example, if the minimum drawn width of a poly line equals 2μm, then minimal matching requires 3μm, moderate matching 4μm, and precise matching 6μm. If the smaller of the matched resistors contains less than 20 to 30 squares, consider increasing the width of the resistors (see Equations 7.6A and 7.6B). If the smallest resistor contains more than 100 squares, consider reducing the resistor width. In no case, however, should one reduce the width of matched deposited resistors below about 2μm because of the potential for excessive variability caused by granularity effects.
4. Where practical, use identical geometries for resistors.
   The existence of corner and end effects precludes precise matching of resistors having different geometries. Resistors having the same width, but different lengths or shapes, can easily experience mismatches of ±1% or more. Matched resistors should be divided into sections as discussed in Section 7.2.6. Sectioning is not necessary for minimal (and even moderate) matching if the parameters controlled by the resistors are trimmed at wafer probe. Wafer-level trimming compensates for most (but not all) variations in resistors caused by geometric factors. Allow an extra 1 to 2% of trim range for unexpected mismatches between resistors of different geometries.
5. Orient matched resistors in the same direction.
   Resistors oriented in different directions may vary by several percent. Diffused resistors show the largest orientation mismatches, but even polysilicon resistors are affected to some degree. Most resistors should be oriented vertically or horizontally. P-type diffused resistors on (100)-oriented silicon may experience less stress-induced variation if they are oriented at 45° to the X- and Y-axes.
6. Place matched resistors in close proximity.
   Mismatches increase with separation. Minimally matched resistors can be spaced a few mils apart, moderately matched resistors should be placed adja-

[28] Tsividis provides a list of ten general matching rules, entries in which correspond to numbers 1–3, 5, 6, and 13 in the list provided in the text: Tsividis, pp. 234–236.

cent to each other, and precisely matched resistors must be interdigitated. Dice larger than about 25kmil^2 (16mm^2), dice that dissipate more than 250mW, dice in heat-sunk packages, designs that experience junction-to-ambient temperature rises in excess of 20°C, and dice mounted using solder or gold eutectics will experience larger mismatches. If any of these conditions apply, then minimally matched resistors should be placed adjacent to each other, and moderately or precisely matched resistors should be arrayed and interdigitated. All resistors in high-stress locations (corners or edges) or within 10mils (250μm) of a power device dissipating more than 100mW should be interdigitated.

7. Interdigitate arrayed resistors.
   Arrayed resistors should be interdigitated to produce a common centroid layout. The resulting array should have an aspect ratio no greater than 3:1, and each resistor segment should be at least five times (and preferably ten times) longer than it is wide. The interdigitation pattern should obey the rules of common-centroid layout (Table 7.3). Arrangements having an even number of segments per resistor are preferable to those having an odd number because even numbers of segments offer better rejection of thermoelectrics. Consider connecting some segments in parallel if this will reduce the total area of the array. If the array requires a large number of segments, consider arranging these into multiple banks connected to form a two-dimensional array.
8. Place dummies on either end of a resistor array.
   Arrayed resistors should include dummies. Poly dummies need not have the same width as the other segments. Diffused dummies should always have the same geometry as adjacent segments. Remember to keep the spacing between adjacent segments constant, and equal to the spacing between the dummies and their neighboring resistor segments. Whenever possible, connect dummy resistors to a quiet low-impedance node.
9. Avoid short resistor segments.
   Very short resistor segments may introduce considerable variation due to contact resistance. Moderately matched resistor segments should contain no fewer than five squares, and precisely matched resistors should contain no fewer than ten. Precisely matched poly resistors should have a total length of no less than 50μm to minimize nonlinearities caused by granularity.
10. Connect matched resistors in order to cancel thermoelectrics.
    Arrayed resistors should always be connected so that equal numbers of segments are oriented in either direction. If the array contains an odd number of segments, then one must remain unpaired. A single unpaired segment does not produce much mismatch, but arrays should, if possible, contain no unpaired segments. Serpentine resistors should be constructed so that their heads lie near one another, because this improves thermoelectric cancellation.
11. If possible, place matched resistors in low stress areas.
    The stress distribution reaches a broad minimum in the middle of the die. Any location ranging from the center halfway out to the edges will lie within this broad minimum. If precisely matched resistors must reside close to an edge, then they should be placed near the middle of one side of the die, preferably a longer side. The stress distribution reaches a maximum in the die corners, so avoid placing matched devices anywhere nearby.
12. Place matched resistors well away from power devices.
    For purposes of discussion, any device dissipating more than 50mW is a power device, and any device dissipating more than 250mW is a major power device.

Precisely matched resistors should reside on an axis of symmetry of the major power devices using one of the optimal symmetry arrangements of Section 7.2.6. Such resistors should also reside no less than 200 to 300μm (8 to 12mils) away from the closest power device. P-type diffused resistors may exhibit less package shift if placed diagonally on (100)-oriented silicon, but this arrangement precludes placement on an axis of symmetry of the power device. If large thermal gradients are expected, then these resistors should be arrayed vertically or horizontally to allow symmetrical placement because the thermal gradients are likely to produce more mismatch than stress gradients. For moderate matching, the matched devices need not lie on an axis of symmetry of the major power devices. They should, however, reside no less than 200 to 300μm away from major power devices and at least 100μm away from smaller power devices. Minimal matching can be achieved anywhere on the die, but if the devices must reside next to a major power device, then they must be interdigitated.

13. Place precisely matched resistors on axes of symmetry of the die.
On (100) silicon, precisely matched resistors should be placed so that the axis of symmetry of the resistor array aligns with one of the two axes of symmetry of the die. P-type diffused resistors may benefit from a diagonal orientation that minimizes their stress sensitivity. On (111) silicon, the axis of symmetry of the array should align to the <211> axis of symmetry of the die. If large numbers of matched devices exist, reserve the optimal locations for the most critical devices.
14. Consider tank modulation effects.
Tank modulation becomes significant for precisely matched resistors having sheet resistances of 100Ω/□ or more, moderately matched resistors having sheet resistances of 500Ω/□ or more, and minimally matched resistors having sheet resistances of 1kΩ/□ or more. Substitute poly resistors for diffused resistors where possible. If diffused resistors must be employed, then consider whether use of a lower sheet material will allow merging the matched resistors into a common tank. For example, moderately matched resistors can be constructed from 160Ω/□ base diffusions placed in the same tank. Trimmed resistors subject to known and controlled voltage biases can usually occupy a common tank regardless of their sheet resistance because trimming largely compensates for the effects of tank modulation.
15. Sectioned resistors are superior to serpentines.
Serpentine resistors are suitable for constructing large, minimally matched resistors or for constructing minimally matched resistors that will be trimmed. All other resistors should use arrays of sections.
16. Use poly resistors in preference to diffused ones.
Polysilicon resistors can be made much narrower than most types of diffused resistors, and, providing that they are sufficiently long, their small widths will not cause any significant increase in mismatch. Also, poly resistors do not require tanks and are therefore immune to tank modulation.
17. Place deposited resistors over field oxide.
Deposited materials, including polysilicon, experience increased variation when crossing oxide steps. Even minimally matched deposited resistors should not cross oxide steps or other surface discontinuities.
18. Choose P-type poly resistors in preference to N-type poly resistors.
Empirical results suggest that boron-doped poly resistors match better than those doped with phosphorus or arsenic. Since the reasons for this difference

are not fully understood, it is possible that some poly resistors may not follow this rule.

19. Do not allow the NBL shadow to intersect matched diffused resistors.
The NBL shadow should not intersect any precisely matched diffused resistor, or any moderately matched shallow diffused resistor (such as HSR). If the direction of NBL shift is unknown, allow adequate overlap of NBL over the resistor on all applicable sides. If the magnitude of the NBL shift is unknown, then overlap NBL over the resistor by at least 150% of the maximum epi thickness.

20. Consider field plating and electrostatic shielding.
Field plate any matched resistor operating above 50% of the thick-field threshold. Field plate all moderately matched diffused resistors having sheet resistances of 500Ω/□ or more. Consider split field plates for precisely matched diffused resistors having sheet resistances of 500Ω/□ or more. Precisely matched polysilicon resistors with sheet resistances of 500Ω/□ or more should have electrostatic shields placed over them where possible.

21. Avoid routing unconnected leads over matched resistors.
Whenever possible, unconnected leads should not run over matched resistors. Unconnected leads can run across minimally matched resistors having sheet resistances of less than 500Ω/□ or moderately matched resistors having sheet resistances of less than 100Ω/□, but the designer should carefully scrutinize all such layouts for potential noise coupling. Leads can run over electrostatic shields and field plates, providing that the latter connect to low-impedance nodes that can absorb the anticipated levels of noise injection. Beware of running high-speed digital signals across matched resistors regardless of whether field plates or electrostatic shielding exists.

22. If leads cross resistors, they should cross all resistor segments in the same manner.
The presence of a lead above a resistor generates mechanical stresses that may alter the value of the resistor. The effects of stress on mismatch will be minimized as long as the lead crosses the resistor array orthogonally, in order to intersect each resistor segment at the same point and with the same area of intersection. Even with this precaution, the presence of the lead will inevitably impair matching, so critically matched resistors should remain uncovered, if possible. Note that this rule cannot always be obeyed, particularly in the case of single-level metal designs and for resistors with sliding contacts.

23. Avoid excessive power dissipation in matched resistors.
Power dissipated within matched resistors can generate thermal gradients that can degrade matching. As a guideline, one should avoid dissipating more than 1mW/mil^2 (1.5μW/μm^2) in precisely matched resistors. Moderately matched resistors can tolerate several times this level of power dissipation. Resistors that dissipate larger amounts of power should be interdigitated. High currents in narrow resistors may also induce velocity saturation nonlinearities (Section 5.3.3).

7.3.2. Rules for Capacitor Matching

Properly constructed capacitors can obtain a degree of matching unequaled by any other integrated component. Matched capacitors form the basis of most data conversion products such as analog-to-digital (A/D) and digital-to-analog (D/A) converters. Untrimmed oxide-dielectric capacitors packaged in plastic can achieve ±0.01% matching. This suffices to allow construction of 14-bit and perhaps even

15-bit converters. Beyond this, some type of wafer-level trimming is required to maintain accuracy. Matching of ±0.001% can be obtained using trimmed oxide-dielectric capacitors packaged in plastic, making possible 16 to 18-bit monolithic converters. Higher-precision products usually employ hybrid assemblies rather than single-die circuits.

Precisely matched capacitors usually employ a thick oxide dielectric in conjunction with deposited electrodes. Junction capacitors have difficulty maintaining even minimal matching due to their extreme temperature dependence and the effects of outdiffusion. Composite dielectrics are inferior to pure oxide dielectrics because the multiple steps required to produce the composite increase its variability. Dielectric relaxation can also degrade matching in composite dielectrics at higher frequencies. Thick oxide dielectrics are favored over thin ones because they are more tolerant of changes in oxide thickness. A ±10Å variation in a 100Å oxide represents ±10% of the oxide thickness, while the same variation in a 500Å oxide represents only ±2% of its thickness. Silicided polysilicon (*polycide*) is sometimes used for constructing the lower plates of matched capacitors because its low resistance minimizes depletion effects and because this material can withstand the high temperatures required to densify the deposited-oxide dielectric. Aluminum is the material of choice for the upper plate due to the absence of depletion effects in this material. Capacitors constructed using unsilicided poly electrodes experience significant surface depletion, even when the poly is heavily doped. These capacitors therefore exhibit temperature coefficients several times as large as metal-polycide capacitors. Despite these problems, poly-poly capacitors can still obtain adequate matching for all but the most precise applications.

The following rules summarize the most important principles of constructing matched deposited-electrode capacitors:[29]

1. Use identical geometries for matched capacitors.
   Capacitors of different sizes or shapes match poorly, so matched capacitors should always use identical geometries. If the capacitors are not the same size, then each should consist of a number of segments (or *unit capacitors*), all of which are copies of the same geometry. The larger capacitor should consist of multiple segments in parallel, while the smaller capacitor should have fewer segments in parallel. Unit capacitors should not connect in series because differences between the parasitic capacitances of the upper and lower plates will produce systematic mismatches. If the required ratio does not lend itself to division into an integer number of unit capacitors, then one nonunitary capacitor should be inserted into the larger of the matched capacitors. The aspect ratio of this nonunitary capacitor should not exceed 1.5:1 (Section 7.2.2).
2. Use square geometries for precisely matched capacitors.
   Peripheral variations are a major source of random mismatch in capacitors. The smaller the periphery-to-area ratio, the higher the obtainable degree of matching. The square has the lowest periphery-to-area ratio of any rectangular geometry and therefore yields the best matching. Rectangular capacitors with moderate aspect ratios (2:1 or 3:1) can be used to construct moderately matched capacitors, but precisely matched capacitors should always be square. Oddly shaped geometries should be avoided because it is difficult to predict the magnitude of their peripheral variations.

[29] Some of these rules follow guidelines proposed by M. J. McNutt, et. al., p. 615.

3. Make matched capacitors as large as practical.
   Increasing the size of capacitors reduces random mismatch. An optimal capacitor size exists, beyond which gradient effects cause increasing variability. The optimum dimensions of square capacitors in several CMOS processes are reported to lie between $20 \times 20\mu m$ and $50 \times 50\mu m$.[30] Capacitors larger than about $1000\mu m^2$ should be divided into multiple unit capacitors, as proper cross-coupling will minimize gradient effects and improve overall matching.
4. Place matched capacitors adjacent to one another.
   Matched capacitors should always reside next to one another. If a large number of capacitors are involved, they should be arranged to form a rectangular array having as small an aspect ratio as possible. For example, if thirty-two matched capacitors are required, then consider using a 4×8 array. Alternatively, a 5×7 array could be constructed and the three unused capacitors connected as dummies. Adjacent rows of unit capacitors should have equal spacings between them, as should adjacent columns of unit capacitors. The row and column spacings need not be the same.
5. Place matched capacitors over field oxide.
   Any surface discontinuities in the thick-field oxide will cause corresponding variations in the topography of the capacitor dielectric. Matched capacitors should always reside over field oxide well away from the edges of moat regions and diffusions.
6. Connect the upper electrode of a matched capacitor to the higher-impedance node.
   The higher-impedance node of the circuit usually connects to the upper electrode, because this generally exhibits less parasitic capacitance than the lower electrode. Substrate noise also couples more strongly to the lower electrode than to the upper electrode. Some arrays may require the high-impedance node of the circuit to connect to the lower plate in order to allow an array of unit capacitors to share a common lower plate. If substrate noise coupling is a concern, consider placing a well under the entire array. This well should connect to a clean analog reference voltage, such as signal ground, so that it can serve as an electrostatic shield for the lower electrode(s) of the capacitor array.
7. Place dummy capacitors around the outer edge of the array.
   Dummy capacitors will shield the matched capacitors from lateral electrostatic fields and will eliminate variations in etch rates. The dummy capacitors need not have the same width as the capacitors of the array as long as an electrostatic shield covers the array. Otherwise, fringing fields can easily extend 30 to $50\mu m$, and arrays of identical dummy capacitors must extend at least this far to ensure precise matching. Moderate matching generally requires only a minimum-width ring of dummy capacitors, and minimal matching does not require dummy capacitors at all. Both electrodes of each dummy capacitor must be connected to prevent static charges from accumulating on the dummy electrodes and interfering with the operation of adjacent devices. The spacing between the dummy capacitors and the adjacent unit capacitors should equal the spacing between rows of unit capacitors.
8. Electrostatically shield matched capacitors.
   Electrostatic shielding provides several benefits. First, it contains fringing fields to the capacitor array, thereby eliminating the need for wide arrays of

[30] Shyu, Temes, and Yao, p. 1075.

dummy capacitors. Second, it allows leads to route over the capacitors without causing mismatch or noise injection. Third, it prevents electrostatic fields from adjacent circuitry from interfering with the matched capacitors. Fourth, it reduces the effects of packaging stress on the underlying capacitors. All precisely matched capacitors should be electrostatically shielded, and this shielding should extend over the dummies placed around the matched capacitors to seal the array against the entry of electrostatic fields. Even minimally matched capacitors can benefit from electrostatic shielding; if no dummy capacitors are used, then the shield should overlap the capacitors by at least 3 to 5μm.

9. Cross-couple arrayed capacitors.
   Capacitor arrays lend themselves to cross-coupling because the unit capacitor forms a compact square rather than an elongated rectangle. The array typically consists of several rows and columns of capacitors. Even in the case of two matched capacitors of equal values, a very compact cross-coupled array can be constructed by dividing each capacitor into two halves. Cross-coupling minimizes the effects of oxide gradients on capacitor matching and provides protection against stress and thermal gradients. The centroids of the matched capacitors should precisely align. In practice, this is difficult to achieve with larger capacitor arrays, so the designer must often settle for less-than-optimal interdigitation patterns.
10. Consider the capacitance of leads connecting to the capacitor.
    The leads that connect a matched capacitor into the circuit will contribute some capacitance of their own. This capacitance becomes of concern when one tries to construct moderately or precisely matched arrays of capacitors. Each unit capacitor should have two minimum-width leads connecting to its top electrode, so that each capacitor will have equal overall lead capacitance. If an array contains a nonunitary capacitor, ideally its number of leads should be equal to twice the ratio of its capacitance to the unit capacitance, but this is often difficult to achieve in practice. The total lead area on each capacitor should be computed, and additional leads should be inserted until the ratio of the lead capacitance equals the ratio of the intended capacitors.
11. Do not run leads over matched capacitors unless they are electrostatically shielded.
    The capacitance between the overlying lead and the upper plate of the capacitor will induce a mismatch between the matched capacitors unless the area of the lead overlying each capacitor is identical. Even then, fringing fields and electrostatic noise coupling will degrade the performance of the matched capacitors. If leads must run over matched capacitors, an electrostatic shield should be inserted between the capacitors and the leads.
12. Use thick-oxide dielectrics in preference to thin-oxide or composite dielectrics.
    Thick-oxide dielectrics exhibit less mismatch due to dimensional variations, so they are preferable to thin-oxide dielectrics. Composite dielectrics, such as oxide-nitride-oxide sandwich dielectrics, have more mismatch than homogeneous dielectrics because multiple processing steps all affect their final capacitance per unit area. While minimal and moderate matching can be obtained using thin-oxide or composite dielectrics, precise matching usually requires thick-oxide dielectrics.
13. If possible, place capacitors in areas of low stress gradients.
    The stress distribution reaches a broad minimum in the middle of the die. Any location ranging from the center of the die halfway out to the edges lies within this broad minimum. Avoid placing capacitors along the edges of the die, and

especially in the corners of the die, as the stress in these regions is substantially greater than elsewhere.

14. Place matched capacitors well away from power devices.
The temperature coefficient of heavily doped poly-poly capacitors is relatively low (perhaps 50ppm/°C), and the temperature coefficient of metal-polycide or metal-metal capacitors is even lower. The direct impact of temperature on matched capacitors is much smaller than on resistors. Matched capacitors should still reside at least 200 to 300μm away from power devices that dissipate 250mW or more.

15. Place precisely matched capacitors on axes of symmetry of the die.
On (100) silicon, precisely matched capacitor arrays should be placed so that the axis of symmetry of the array aligns with one of the two axes of symmetry of the die. On (111) silicon, the axis of symmetry of the array should preferably lie on the <211> axis of symmetry of the die. If large numbers of matched devices are required, reserve the optimal locations for the most critically matched devices.

7.4 SUMMARY

Most integrated circuits contain numerous matched resistors and capacitors. The layout designer should determine which components must match, and with what degree of precision. Using this information, a die floor plan can be constructed showing the relative locations of power devices and matched components. The most critically matched devices should occupy locations near the middle of the die on an axis of symmetry of the power devices. Even if no power devices are present on the die, stress considerations still dictate the placement of the most sensitive matched components near the middle of the die. Preliminary die planning before layout begins will pay dividends in the form of easier circuit construction and interconnection as well as better performance.

Matched devices should never reside in the corners of the die, or near a major heat source. Sometimes matched resistors must be placed along a die edge to facilitate the placement of trimpads for fuses or Zener zaps. In this case, the resistors are best placed near the middle of one of the sides of the die.

The matching of resistors and capacitors is very much a function of how well these components are laid out. Two resistors haphazardly laid some distance away from one another using different sizes and shapes oriented in different directions can easily mismatch by several percent. If the same resistors are constructed as an array of interdigitated sections, then they will certainly match to better than ±0.1%.

The exact degree of matching achievable from any given layout is difficult to determine. The hard data required to quantitatively evaluate matching performance is rarely available in a manufacturing environment, so the layout designer must make decisions based on limited information. Although this is a difficult and sometimes frustrating process, the designer can greatly improve the performance of many circuits by following the principles discussed in this chapter.

7.5 EXERCISES

Refer to Appendix C for layout rules and process specifications.

7.1. A pair of capacitors were designed to have values of 5pF and 2.5pF. Measurements on ten units provide the following pairs of values: (5.19pF, 2.66pF), (5.21pF, 2.67pF), (5.19pF, 2.65pF), (5.23pF, 2.66pF), (5.21pF, 2.68pF), (5.12pF, 2.67pF), (5.25pF, 2.68pF), (5.15pF, 2.63pF), (5.21pF, 2.61pF), (5.28pF, 2.61pF). What is the three-sigma worst-case mismatch between these two capacitors?

7.2. A twelve-wafer lot of wafers numbered 1, 2, 3 . . . 12 are available for use as samples in an experimental determination of mismatch. Provide detailed instructions for selecting a sample of 30 units from this lot.

7.3. A pair of 3pF capacitors have a measured standard deviation of mismatch of 0.17%. How large must the capacitors be made to ensure that they will achieve an estimated six-sigma worst-case mismatch of ±0.5%? Assume that systematic mismatches are negligible.

7.4. A certain design contains a pair of 3μm-wide resistors that have a measured standard deviation of mismatch of 0.32% and a measured systematic mismatch of +0.10%. Assuming that the systematic mismatch does not vary with width, how wide would the resistors have to be made to achieve an estimated three-sigma mismatch of ±0.5%?

7.5. Divide the following matched resistances into segments following the rules of Section 7.2.2, assuming a sheet resistance of 500Ω/□. In each case, state the number of segments in each resistor, and the segment resistances.
- a. 10kΩ and 15kΩ.
- b. 7.5kΩ and 11kΩ.
- c. 3.66kΩ and 11.21kΩ.
- d. 75.3kΩ and 116.7kΩ.

7.6. Divide the following matched capacitors into unit capacitances following the rules of Section 7.2.2, assuming an areal capacitance of 1.7fF/μm^2. State the number of unit capacitors in each device, the unit capacitor values, and their dimensions.
- a. 4.0pF and 8.0pF.
- b. 1.8pF and 4.2pF.
- c. 3.7pF and 5.1pF.
- d. 25pF and 25pF.

7.7. Choose an optimal orientation for each of the following types of resistors:
- a. Standard bipolar HSR resistors.
- b. Analog BiCMOS N-well resistors.
- c. P-type polysilicon resistors.
- d. Nichrome thin-film resistors (nichrome is a polycrystalline metal alloy).

7.8. Devise one-dimensional interdigitation patterns for each of the following cases:
- a. Two resistors with a ratio of 4:5.
- b. Two resistors with a ratio of 2:7.
- c. Three resistors with a ratio of 1:3:5.
- d. Four resistors with a ratio of 1:2:4:8.

7.9. Lay out a resistor divider consisting of two 3kΩ, 8μm-wide base resistors placed in a common tank. Include all necessary metallization, including a separate lead for the tank contact.

7.10. Construct a resistor divider consisting of two 25kΩ, 8μm-wide HSR resistors.

7.11. The divider of Exercise 7.10 forms part of a die having dimensions of 2150μm by 1760μm. These dimensions do not include scribe streets and seals, which may be ignored for the purposes of this exercise. Draw a rectangle having these dimensions and place the divider in the best possible location for optimal matching. Assume the design contains no major heat sources.

7.12. Repeat Exercise 5.13, laying out the resistors to obtain precise matching. One of the resistors would normally contain a single segment; replace this resistor with a series-parallel network containing an even number of 1kΩ segments.

7.13. Suppose the trim network in Exercise 7.12 forms part of a die having an active area of 5.3mm^2, of which a power transistor consumes 3.6mm^2. This area does not include scribe streets and seals, which need not be considered for this exercise. Choose an aspect ratio for the die and construct a rectangle having the requisite area. Place another rectangle in the layout to denote the location of the power device. Now locate the trim network in an optimal location along one side of the die. Place the trimpads

as close to the edge of the die as possible. Space all metallization at least 8μm from the edge of the die.

7.14. Construct a capacitor array using analog CMOS poly-poly capacitors. The capacitors should have the following values: 0.5pF, 1pF, 2pF, 4pF, and 8pF. Assume that all capacitors share a common poly-1 plate, and bring a lead from each capacitor's poly-2 plate out to the edge of the array. Use copies of the unit capacitors as dummies and cover the array with a metal-2 shield. Take whatever other measures are required for precise matching.