The ART of ANALOG LAYOUT

Alan Hastings



Library of Congress Cataloging-in-Publication Data

Hastings, Alan (Ray Alan)

The art of analog layout / Alan Hastings.

p. cm

Includes bibliographical references and index.

ISBN 0-13-087061-7

1. Integrated circuits—Design and construction. 2. Layout (Printing) I. Title.

TK7874.H3926 2001 621.3815—dc21

00-045307

Vice president and editorial director, ECS: Marcia Horton

Publisher: Tom Robbins

Associate editor: Alice Dworkin Editorial assistant: Jessica Power

Production editor: Carlisle Communications, Ltd.

Executive managing editor: Vince O'Brien

Managing editor: David A. George

Art director: Jayne Conte

Cover design: Joseph Sengotta Art editor: Adam Velthaus

Manufacturing manager: Trudy Pisciotti

Manufacturing buyer: Dawn Murrin

Assistant vice president of production and manufacturing, ESM: David W. Riccardi



Copyright © 2001 by Prentice-Hall, Inc. Upper Saddle River, New Jersey 07458.

All rights reserved. No part of this book may be reproduced, in any form or by any means, without the permission in writing from the publisher.

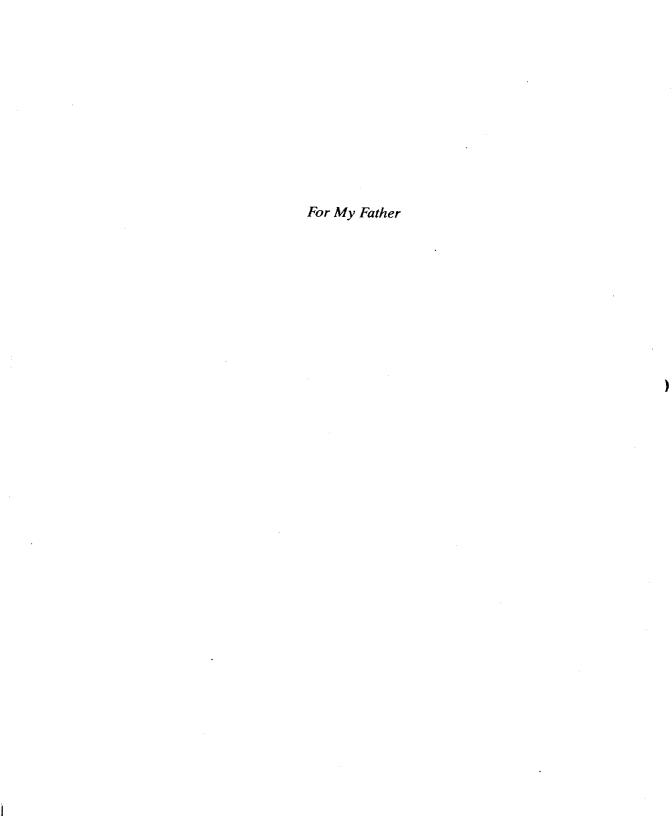
The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development. research, and testing of the theories to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to the documentation contained in this book.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-087061-7

Prentice-Hall International (UK) Limited, London
Prentice-Hall of Australia Pty. Limited, Sydney
Prentice-Hall Canada Inc., Toronto
Prentice-Hall Hispanoamericana, S.A., Mexico
Prentice-Hall of India Private Limited, New Delhi
Prentice-Hall of Japan. Inc., Tokyo
Pearson Education Asia Pte. Ltd., Singapore
Editora Prentice-Hall do Brasil, Ltda., Rio de Janeiro



Contents

Preface	e xvii
Acknov	vledgments xix
1 D	evice Physics
	Semiconductors 1
	1.1.1 Generation and Recombination
	1.1.2 Extrinsic Semiconductors 6
	1.1.3 Diffusion and Drift 9
1.2	PN Junctions 10
	1.2.1 Depletion Regions 10
	1.2.2 PN Diodes 13
	1.2.3 Schottky Diodes 15
	1.2.4 Zener Diodes 17
	1.2.5 Ohmic Contacts 19
1 3	
1.5	Bipolar Junction Transistors 20
1.4	1.3.2 I-V Characteristics 23
1.4	MOS Transistors 24
	1.4.1 Threshold Voltage 27
	1.4.2 I-V Characteristics 29
	JFET Transistors 31
1.6	Summary 33
1.7	Exercises 34

Ser	niconductor Fabrication		
2.1	Silicon Manufacture 36		
	2.1.1 Crystal Growth 37		
	2.1.2 Wafer Manufacturing 38		
	2.1.3 The Crystal Structure of Silicon 38		
2.2	Photolithography 40		
	2.2.1 Photoresists 40		
	2.2.2 Photomasks and Reticles 41		
	2.2.3 Patterning 42		
2.3	Oxide Growth and Removal 42		
	2.3.1 Oxide Growth and Deposition 43		
	2.3.2 Oxide Removal 44		

2.3.3 Other Effects of Oxide Growth and Removal 46

3

2.4	Diffusion and Ion Implantation 49
	2.4.1 Diffusion 50
	2.4.2 Other Effects of Diffusion 52
	2.4.3 Ion Implantation 53
2.5	
	2.5.1 Epitaxy 56
	2.5.2 Polysilicon Deposition 58
2.6	Metallization 58
	2.6.1 Deposition and Removal of Aluminum 59
	2.6.2 Refractory Barrier Metal 60
	2.6.3 Silicidation 62
	2.6.4 Interlevel Oxide, Interlevel Nitride, and Protective Overcoat 63
2.7	Assembly 64
	2.7.1 Mount and Bond 66
	2.7.2 Packaging 69
2.8	
2.9	Exercises 69
<i>Rej</i> 3.1	Standard Bipolar 72 3.1.1 Essential Features 72 3.1.2 Fabrication Sequence 73 Starting Material 73 N-Buried Layer 73 Epitaxial Growth 74 Isolation Diffusion 74 Deep-N+ 74 Base Implant 75 Emitter Diffusion 75 Contact 76 Metallization 76
	Protective Overcoat 77
	3.1.3 Available Devices 77
	NPN Transistors 77
	PNP Transistors 79
	Resistors 81
	Capacitors 83
	3.1.4 Process Extensions 84
	Up-down Isolation 84
	Double-level Metal 84
	Schottky Diodes 85
	High-Sheet Resistors 86
	Super-beta Transistors 86
32	Polysilican Gata CMOS PT

3.2.1 Essential Features 88

3.2.2	Fabrication Sequence 89
	Starting Material 89
	Epitaxial Growth 89
	N-well Diffusion 89
	Inverse Moat 90
	Channel Stop Implants 90
	LOCOS Processing and Dummy Gate Oxidation 91
	Threshold Adjust 92
	Polysilicon Deposition and Patterning 93
	Source/Drain Implants 93
	Contacts 94
	Metallization 94
	Protective Overcoat 94
3.2.3	Available Devices 95
	NMOS Transistors 95
	PMOS Transistors 97
	Substrate PNP Transistors 98
	Resistors 98
	Capacitors 100
3.2.4	Process Extensions 100
	Double-level Metal 100
	Silicidation 101
	Lightly Doped Drain (LDD) Transistors 101
	Extended-Drain, High-Voltage Transistors 103
Ana	log BiCMOS 104
3.3.1	Essential Features 104
3.3.2	Fabrication Sequence 106
	Starting Material 106
	N-buried Layer 106
	Epitaxial Growth 106
	N-well Diffusion and Deep-N+ 107
	Base Implant 107
	Inverse Moat 108
	Channel Stop Implants 108
	LOCOS Processing and Dummy Gate Oxidation . 108
	Threshold Adjust 109
	Polysilicon Deposition and Pattern 109
	Source/Drain Implants 109
	Metallization and Protective Overcoat 110
	Process Comparison 110
3.3.3	Available Devices 111
	NPN Transistors 112
	PNP Transistors 112
	Resistors 115
Summe	nary 115

3.3

3.5 Exercises 116

Λ	l 177.	
٦	r Fu	ilure Mechanisms
	4.1	Electrical Overstress 118
		4.1.1 Electrostatic Discharge (ESD) 118
		Effects 120
		Preventative Measures 120
		÷.1.2 Electromigration 121
		Effects 121
		Preventative Measures 122
	4.0	-1.3 The Antenna Effect 122
	4.2	Contamination 124
		4.2.1 Dry Corrosion 124
		Effects 124
		Preventative Measures 125
		4.2.2 Mobile Ion Contamination 125
		Effects 125
	4.0	Preventative Measures 126
	4.3	Surface Effects 128
		4.3.1 Hot Carrier Injection 128
		Effects 128
		Preventative Measures 130
		4.3.2 Parasitic Channels and Charge Spreading 131
		Effects 131
		Preventative Measures (Standard Bipolar) 133
		Preventative Measures (CMOS and BiCMOS) 137
	4.4	Parasitics 139
		4.4.1 Substrate Debiasing 140
		Effects 140
		Preventative Measures 142
		4.4.2 Minority-Carrier Injection 143
		Effects 143
		Preventative Measures (Substrate Injection) 146
		Preventative Measures (Cross-injection) 151
	4.5	Summary 153
	4.6	Exercises 153
5	Res	istors
	5.2	Resistivity and Sheet Resistance 156 Resistor Layout 158
	5.4	Resistor Layout 158

- 5.3 Resistor Variability 162
 - 5.3.1 Process Variation 162
 - 5.3.2 Temperature Variation 163
 - 5.3.3 Nonlinearity 163
 - 5.3.4 Contact Resistance 166
- 5.4 Resistor Parasitics 167

7.2 Causes of Mismatch 217

Process Biases 219

Pattern Shift 220

Random Statistical Fluctuations 217

7.2.1

7.2.2

7.2.3

		7.2.4 Variations in Polysilicon Etch Rate 222
		7.2.5 Diffusion Interactions 224
		7.2.6 Stress Gradients and Package Shifts 226 Piezoresistivity 227
		Gradients and Centroids 229
		Common-centroid Layout 231
		Location and Orientation 235
		7.2.7 Temperature Gradients and Thermoelectrics 236
		Thermal Gradients 238
		Thermoelectric Effects 240
		7.2.8 Electrostatic Interactions 242
		Voltage Modulation 242
		Charge Spreading 245
		Dielectric Polarization 246
		Dielectric Relaxation 248
	7.3	Rules for Device Matching 249
		7.3.1 Rules for Resistor Matching 249
		7.3.2 Rules for Capacitor Matching 253
	7.4	Summary 257
	7.5	Exercises 257
8	Ri	polar Transistors
•	8.1	
	0.1	Topics in Bipolar Transistor Operation 260 8.1.1 Beta Rolloff 262
		8.1.2 Avalanche Breakdown 262
		8.1.3 Thermal Runaway and Secondary Breakdown 264 8.1.4 Saturation in NPN Transistors 266
		The state of the s
	8.2	
	0.2	- Form Dinam Signal Mandistora 2/4
		8.2.2 The Standard Bipolar Substrate PNP Transistor 279
		The state of the s
		Construction of Small-signal Substrate PNP Transistors 28. 8.2.3 The Standard Bipolar Lateral PNP Transistor 283
		200
		Construction of Small-signal Lateral PNP Transistors 285 8.2.4 High-voltage Bipolar Transistors 291
	83	Alternation S. III is a property of the control of
	O.D.	8.3.1 Extensions to Standard Bipolar 293
		8.3.2 Analog BiCMOS Bipolar Transistors 294
		8.3.3 Bipolar Transistors in a CMOS Process 297
		0.7.4 1.1 1.1 1
	8.4	Summary 302 Summary 302
	8.5	Exercises 303

9	App	lications of Bipolar Transistors
	9.1	Power Bipolar Transistors 306
		9.1.1 Failure Mechanisms of NPN Power Transistors 307
		Emitter Debiasing 307
		Thermal Runaway and Secondary Breakdown 309
		9.1.2 Layout of Power NPN Transistors 311
		The Interdigitated-emitter Transistor 311
		The Wide-emitter Narrow-contact Transistor 314
		The Christmas-tree Device 315
		The Cruciform-emitter Transistor 316
		Power Transistor Layout in Analog BiCMOS 317
		Selecting a Power Transistor Layout 318
		9.1.3 Saturation Detection and Limiting 319
	9.2	Matching Bipolar Transistors 322
		9.2.1 Random Variations 323
		9.2.2 Emitter Degeneration 325
		9.2.3 NBL Shadow 327
		9.2.4 Thermal Gradients 328
		9.2.5 Stress Gradients 332
	9.3	Rules for Bipolar Transistor Matching 334
		9.3.1 Rules for Matching NPN Transistors 335
		9.3.2 Rules for Matching Lateral PNP Transistors 337
	9.4	_
	9.5	Exercises 340
_	,,,	
0	Dio	des
	10.1	Diodes in Standard Bipolar 343
		10.1.1. Diode-connected Transistors 343
		10.1.2 Zener Diodes 346
		Surface Zener Diodes 347
		Buried Zeners 349
		10.1.3 Schottky Diodes 352
	10.2	• • • • • • • • • • • • • • • • • • •
	10.3	
	20.0	10.3.1 Matching PN Junction Diodes 359
		10.3.2 Matching Zener Diodes 360
		10.3.3 Matching Schottky Diodes 361
	10.4	-
		Exercises 362
	10.5	
_		

MOS Transistors

11.1 Topics in MOS Transistor Operation 364
11.1.1 Modeling the MOS Transistor 364

Device Transconductance 365

Threshold Voltage 367

12

	11.1.2 Parasitics of MOS Transistors 370
	Breakdown Mechanisms 372
	CMOS Latchup 375
11.2	- anglish Toly Gute CiviOs Italisisiolis 3/6
	11.2.1 Coding the MOS Transistor 377
	Width and Length 378
	11.2.2 N-well and P-well Processes 379
	11.2.3 Channel Stops 381
	11.2.4 Threshold Adjust Implants 383
	11.2.5 Scaling the Transistor 386
	11.2.6 Variant Structures 388
	Serpentine Transistors 391
	Annular Transistors 391
	11.2.7 Backgate Contacts 303
11.3	Summary 396
11.4	Exercises 396
An	plications of MOS Transistors
12.1	Extended-voltage Transistors 399
14.1	1311 100 1000
	13.1.3
	405
	Extended-drain NMOS Transistors 403
	Extended-drain PMOS Transistors 405
12.2	12.1.3 Multiple Gate Oxides 405
12.4	Power MOS Transistors 407
	Thermal Runaway 407
	Secondary Breakdown 408
	Rapid Transient Overload 408
	MOS Switches versus Bipolar Switches 409
	12.2.1 Conventional MOS Power Transistors 410
	The Rectangular Device 411
	The Diagonal Device 413
	Computation of R _M 413
	Other Considerations 414
	Nonconventional Structures 416
	12.2.2 DMOS Transistors 417
	The Lateral DMOS Transistor 418
	The DMOS NPN 420
12.3	The JFET Transistor 422
	12.3.1 Modeling the JFET 422
	12.3.2 JFET Layout 423
12.4	MOS Transistor Matching 426
	12.4.1 Geometric Effects 427
	Gate Area 428

Gate Oxide Thickness 428

	Channel Length Modulation 429
	Orientation 429
	12.4.2 Diffusion and Etch Effects 430
	Polysilicon Etch Rate Variations 430
	Contacts Over Active Gate 431
	Diffusions Near the Channel 432
	PMOS versus NMOS Transistors 432
	12.4.3 Thermal and Stress Effects 433
	Oxide Thickness Gradients 433
	Stress Gradients 433
	Metallization-induced Stresses 434
	Thermal Gradients 434
	12.4.4 Common-centroid Layout of MOS Transistors 435
12.5	Rules for MOS Transistor Matching 439
12.6	Summary 442
12.7	Exercises 443
_	cial Topics
13.1	g
	13.1.1 Flawed Device Mergers 446
	13.1.2 Successful Device Mergers 450
	13.1.3 Low-risk Merged Devices 452
	13.1.4 Medium-risk Merged Devices 453
	13.1.5 Devising New Merged Devices 455
13.2	Guard Rings 455
	13.2.1 Standard Bipolar Electron Guard Rings 456
	13.2.2 Standard Bipolar Hole Guard Rings 457
	13.2.3 Guard Rings in CMOS and BiCMOS Designs 458
13.3	
	13.3.1 Mock Layouts and Stick Diagrams 461
	13.3.2 Techniques for Crossing Leads 463
12.4	13.3.3 Types of Tunnels 464
13.4	= ====================================
	13.4.1 Scribe Streets and Alignment Markers 466
	13.4.2 Bondpads, Trimpads, and Testpads 468
	13.4.3 ESD Structures 471
	Zener Clamp 473
	Two-stage Zener Clamps 475 Buffered Zener Clamp 476
	V_{CES} Clamp 478 V_{CES} Clamp 479
	Antiparallel Diode Clamps 480
	Additional ESD Structures for CMOS Processes 480
	13.4.4 Selecting ESD Structures 483
13.5	Exercises 485
10.0	AND PROPERTY.

13

14	Ass	embling the Die
		Die Planning 488
		14.1.1 Cell Area Estimation 489
		Resistors 489
		Capacitors 489
		Vertical Bipolar Transistors 489
		Lateral PNP Transistors 490
		MOS Transistors 490
		MOS Power Transistors 490
		Computing Cell Area 491
		14.1.2 Die Area Estimation 491
		14.1.3 Gross Profit Margin 494
	14.2	Floorplanning 495
		Top-level Interconnection 500
		14.3.1 Principles of Channel Routing 501
		14.3.2 Special Routing Techniques 503
		Kelvin Connections 503
		Noisy Signals and Sensitive Signals 504
		14.3.3 Electromigration 506
		14.3.4 Minimizing Stress Effects 508
	14.1	Conclusion 510
	14.5	Exercises 510

- Appendices
 A. Table of Acronyms Used in the Text 513
 B. The Miller Indices of a Cubic Crystal 516
 C. Sample Layout Rules 519

 - Mathematical Derivations 527 D.
 - Sources for Layout Editor Software 532

Index 533