14 *Assembling the Die*

The first step in laying out an integrated circuit is estimating the die area. Layout designers should not rely on preliminary area estimates, as these are seldom accurate. The area of each circuit block, or *cell,* should be computed separately. The total die area equals the sum of the areas of all the cells plus the area required for wiring, bondpads, scribe seals, and scribe streets. As area estimates tend toward optimism, the prudent designer always includes a generous safety margin.

Once the dimensions of the die and the areas of all of the cells have been determined, a floorplan should be constructed. A good floorplan includes an outline of the die, placements of all pads, and the sizes and locations of all the major cells. The initial floorplan often requires revision as the layout progresses.

The completed floorplan serves as a template for constructing the individual cells. Each cell requires a multitude of resistors, capacitors, transistors, and diodes. When these components have been laid out, the designer must arrange them to optimize matching, packing, and ease of interconnection. The components are then connected to form a cell, and the cells are connected to form the completed die. Previous chapters have examined the design of individual components and their placement relative to one another. This chapter examines the process of planning a die layout, constructing a die floorplan, and interconnecting the finished cells to form the complete die.

14.1 DIE PLANNING

The layout of an integrated circuit requires considerable planning and forethought. An experienced designer knows what tasks must be accomplished and in what order; the layout progresses smoothly and all of the components fit into their assigned places. A novice attempting the same feat soon discovers that it is not as easy as it seems. Days or weeks of effort often come to naught because of unforeseen complications. Most of these difficulties are usually due to incorrect die area estimates, misplaced components, and inadequate wiring channels. The cautious designer can avoid most of these problems by spending a few hours planning the layout.

Using the information gathered during the planning phase, one can estimate the total die area and the cost of manufacture. Assuming that the design appears profitable, a floorplan can be developed showing the size, shape, and location of each cell. This floorplan forms the basis for the top-level layout of the die. Floorplans become particularly valuable on larger designs where many people must simultaneously create portions of the layout.

14.1.1. Cell Area Estimation

The first phase of the planning effort consists of compiling a list of all the cells used in the design. If detailed schematics are available, then this task amounts to little more than listing the cells found in the top-level schematic. If no schematics exist, then the circuit designer must prepare a list based on a careful examination of the specifications. The list should only contain cells appearing in the top-level schematic, and should exclude cells occupying the lower levels of the schematic hierarchy. The top-level cells may number as few as three or four, or as many as thirty or forty, depending on the scale of the design. The list should also include any power devices that require specific locations due to routing or matching considerations.

The designer must now estimate the area required by each cell. Some cells may have already been laid out for previous designs, in which case accurate area estimates are easily obtained by measurement. If a previous design contains a similar cell, then its layout may provide a close approximation of the area required by the new cell. If no previous layout exists, then the area of the cell must be computed from the areas of the individual components. The following sections explain how to rapidly estimate the size of the areas required by various types of components. These estimates are, of necessity, somewhat imprecise, but planners are generally allowed a margin of error of at least ±20%. Area estimates are usually given in either square millimeters (mm^2) or in thousands of square mils ($kmil^2$), where $1kmil^2 = 0.645mm^2$ and $1mm^2 = 1.55kmil^2$.

Resistors

The area, A, required to construct one or more resistors can be estimated using the formula

$$A \cong \frac{1.2RW_r(W_r + S_r)}{R_s} \qquad [14.1]$$

where R equals the desired resistance, R_s is the applicable sheet resistance, W_r is the width of the resistor, and S_r is the spacing between adjacent resistor stripes. The factor of 1.2 helps account for the space consumed by dummy resistors, contact heads, and less-than-ideal layouts. For example, 122kΩ of 2kΩ/□ HSR with a width of 6μm and a spacing of 12μm will consume an estimated $7900\mu m^2$ of die area. Resistors of different widths or materials must be computed separately.

Capacitors

The area required by capacitors depends on the capacitance per unit area of the dielectric. For finger-style junction capacitors, an average capacitance per unit area can be computed using an existing capacitor as a guideline. For example, suppose that a 50pF finger-style junction capacitor has a measured area of $27{,}500\mu m^2$. This capacitor has an average capacitance per unit area of $1.8fF/\mu m^2$.

Vertical Bipolar Transistors

The area of vertical NPN and substrate PNP transistors must be computed separately, but the same principles apply to both types of devices. The area required for

a minimum-emitter device equals the area consumed by its tank; this is best measured from the layout of an existing device. The device area will not scale linearly with emitter area because the emitter forms only a small part of the transistor. It is usually not worth the effort to obtain exact area values for small transistors. One can safely assume that transistors with emitter areas of two to five times the minimum require 150% of the minimum device area. Larger transistors should be roughly sketched out, and their area estimated on this basis. Figure 14.1 shows a sketch of a wide-emitter, narrow-contact transistor. On the basis of the dimensions indicated, this device would consume an area of 38,800μm^2 and would contain 4,000μm^2 of emitter.

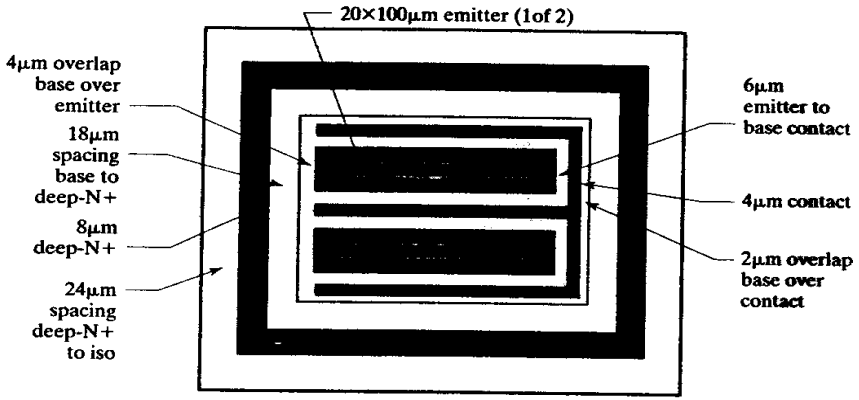

FIGURE 14.1 Sketch of a wide-emitter, narrow-contact transistor used for estimating its area.

Lateral PNP Transistors

The area required by a minimum lateral PNP transistor can be obtained by measuring the tank area of an existing device. Larger transistors are normally constructed either by placing multiple copies of a single device in a common tank or by stretching the transistor along one axis. In either case, the device area scales approximately linearly with collector size. Split-collector transistors require additional area, so count each such device as 150% of the minimum device area.

MOS Transistors

The area, A, required for a finger-style MOS transistor can be approximated by

$$A \cong 1.3W_g(L_g + S_{gg}) \qquad [14.2]$$

where W_g equals the width of the gate, L_g equals the length of the gate, and S_{gg} equals the spacing between adjacent gate stripes of a multiple-finger transistor. The factor of 1.3 helps account for the space consumed by the terminations on either end of the transistor array, well spacings, and less-than-ideal packing. This formula usually underestimates the area required by small transistors, particularly if they require guard rings or separate wells.

MOS Power Transistors

MOS power transistors are usually specified in terms of their on-resistance, $R_{ds(on)}$. Area estimations based on device models or SPICE simulations do not properly account for metallization resistance. Estimates based on measured specific on-

resistance R_{sp} give much better results. The area required to obtain a desired $R_{ds(on)}$ equals

$$A \cong \frac{R_{sp}}{R_{ds(on)} - R_p} \qquad [14.3]$$

The variable R_p accounts for the resistance of the package, including bondwires and leadframe. The bondwires contribute the largest component of the package resistance: A typical 1mil gold bondwire contributes about 25 to 50mΩ (Section 13.4.2). Larger-diameter bondwires or multiple bondwires placed in parallel can greatly reduce this resistance.

The accuracy of equation 14.3 depends on how closely the proposed transistors resemble the test devices. The proposed transistor should have the same gate length, and the R_{sp} and $R_{ds(on)}$ figures should be measured at the same gate-to-source voltage. Because R_{sp} varies with device area, the area of the proposed transistors should not differ from the area of the test devices by more than a factor of five. Further, the dimensions of the finger structure and the metallization pattern of the proposed transistor and the test device should closely resemble one another.

Computing Cell Area

The area of a cell A_{cell} can be estimated using the following formula

$$A_{cell} = P_f \Sigma A \qquad [14.4]$$

where ΣA equals the sum of the areas of all of the individual components. The packing factor, P_f, accounts for the area consumed by isolation and device interconnection as well as the area wasted by imperfect packing. Standard bipolar designs employing single-level metal typically have packing factors of 1.5 to 3.0. Values toward the lower end of this range represent well-packed designs using custom-crafted devices and extensive device mergers. The values toward the upper end of this range represent designs using standardized components and few or no device mergers. Standard bipolar designs using double-level metal require less area and will typically have packing factors of 1.5 to 2.0. Double-level-metal analog CMOS or BiCMOS designs using standardized components usually achieve packing factors of 1.5 to 2.0. Triple-level metal provides little improvement unless the cell contains an extraordinary amount of interconnection.

Suppose that the bandgap circuit in Figure 14.2 will be laid out in a standard bipolar process using single-level metallization. Three of the transistors require individual sketches: Q_1, Q_2, and Q_{10}. The first two form the ratioed pair of the Brokaw bandgap cell, while Q_{10} is a small power device. The area of the other devices can be estimated by the procedures discussed. Table 14.1 shows the results of this calculation.

14.1.2. Die Area Estimation

Three factors contribute to the overall die area: the circuitry it contains, the ring of pads around its periphery, and the scribe streets separating it from adjacent dice. The circuitry resides in the middle of the die, forming the *core*. The pads lie around the periphery of the die, forming the *padring*. Ideally, both the core and the padring should contain no wasted space. Practical designs almost never meet this goal. In a *core-limited* design, the core packs tightly into the space inside the padring, but there

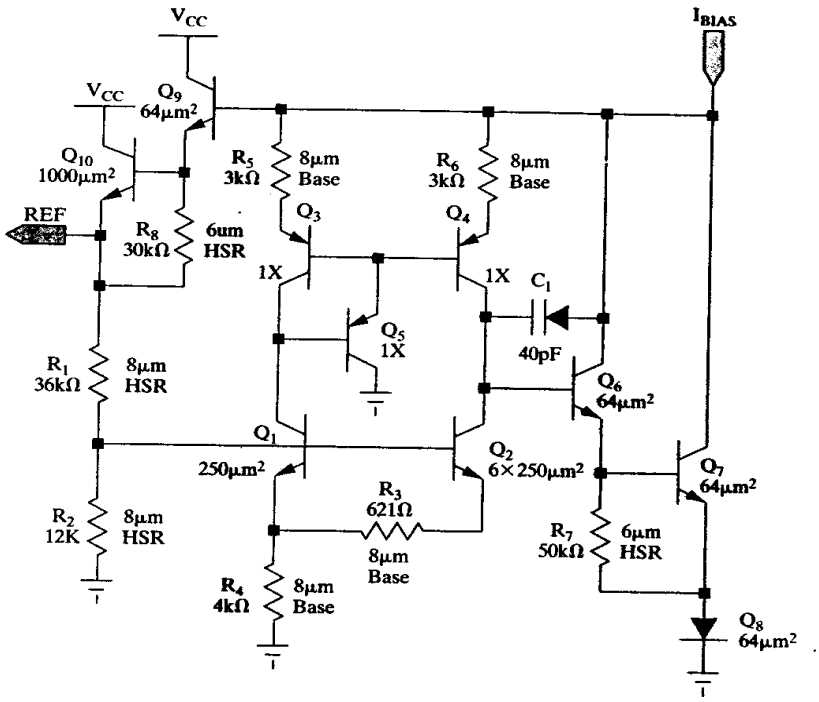

FIGURE 14.2 Schematic of the sample circuit block.

TABLE 14.1 Estimated area for the simple Brokaw bandgap.

Device	Amount	Area
8μm 160Ω/□ base resistance	10.621kΩ	14,200μm²
8μm 2kΩ/□ HSR resistance	48.0kΩ	4,600μm²
6μm 2kΩ/□ HSR resistance	80.0kΩ	5,200μm²
Junction capacitance, 1.8fF/μm²	40pF	22,200μm²
Minimum NPN transistors @ 2,200μm²	4	8,800μm²
Minimum PNP transistors @ 4,100μm²	3	12,300μm²
Bandgap NPN transistors @ 3,100μm²	7	21,700μm²
Output NPN transistors @ 6,600μm²	1	6,600μm²
Total area of components		95,400μm²
Estimated cell area ($P_f = 2$)		0.19mm²

are not enough pads to fill the ring (Figure 14.3A). The gaps between the pads are often used for ESD structures and trim circuitry. A *pad-limited* design has so many pads that the space remaining inside the padring exceeds the area required by the core (Figure 14.3B). The estimation procedure must determine whether the design is core-limited or pad-limited before a final area estimate is possible.

The first step in computing the estimated die area consists of computing the core area A_c

$$A_c \cong R_f P_f \Sigma A_{cell} + P_f \Sigma A_{pwr} \qquad [14.5]$$

where ΣA_{cell} represents the sum of the areas of all the individual cells, and ΣA_{pwr} represents the sum of the areas of all the power devices not contained in any cell. The core does not include bondpads, trimpads, ESD devices, scribe seals, and scribe

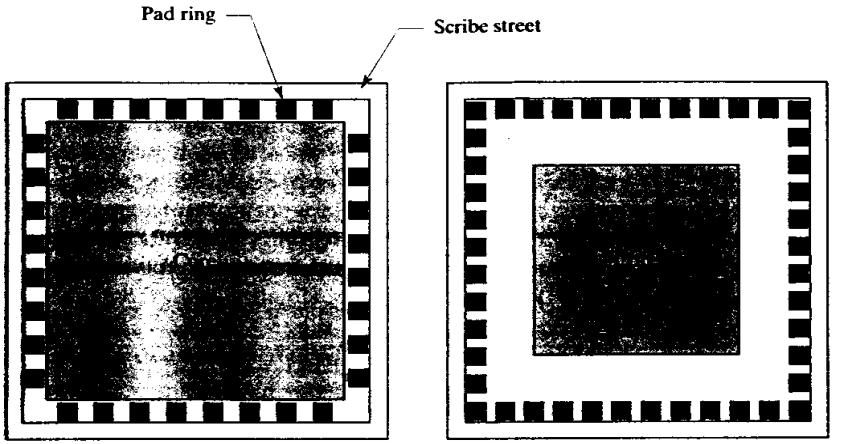

FIGURE 14.3 Comparison of core-limited and pad-limited dice.

streets. The *routing factor* R_f accounts for the area consumed by top-level wiring. Typical routing factors for a design with several hundred top-level signals are 1.3 to 1.5 for single-level metal, 1.2 to 1.3 for double-level metal, and 1.1 to 1.2 for triple-level metal. Designs making extensive use of poly routing fall somewhere between these values. For example, a design routed on metal-1 and poly-1 might achieve a routing factor of 1.3, as compared with a routing factor of 1.4 for metal-1 alone. The *packing factor* P_f represents the areas of wasted space between cells. A die containing twenty or thirty moderate-sized cells should achieve a packing factor of 1.1 to 1.2. Layouts incorporating very large or very odd-shaped cells often have much higher packing factors. Conversely, hand-optimized designs can achieve a packing factor close to one. However, hand optimization requires additional time and effort, particularly for larger designs.

The following formula computes the estimated area of the entire die A_{die} based upon a square aspect ratio:

$$A_{die} = (\sqrt{A_c} + 2W_{pr} + W_s)^2 \qquad [14.6]$$

The design rules should specify the scribe width W_s, typically 75 to 125μm. The width of the padring W_{pr} usually equals about 130% of the width of a bondpad. The design rules generally specify the minimum allowed dimensions of the bondpads. For ballbonded gold wires, the minimum bondpad width equals about three times the diameter of the wire. Following these guidelines, a 1mil (25μm) gold wire requires a 75μm bondpad and a 100μm padring. These approximations are adequate for preliminary area estimates, but the final area estimate should only be made after the padring has been constructed (Section 13.4).

The above computations assume that the padring contains enough space to contain all of the required pads. The minimum die perimeter P_{min} required to place the pads approximately equals

$$P_{min} \cong (N_p + 4)(W_p + S_p) + 4W_s \qquad [14.7]$$

where N_p equals the total number of pads, W_p equals the width of a pad, W_s equals the width of the scribe, and S_p equals the minimum spacing allowed between adjacent pads (measured between the facing edges of adjacent pads). This formula assumes that the pads can be placed relatively close to the corners of the die and that circuitry cannot reside underneath the bondpads. If the layout rules specify a

minimum allowed distance from the corner of the die to the edges of the nearest bondpads, then add eight times this distance to the estimate of P_{min} computed above.

The *perimeter utilization factor* P represents the fraction of available pad perimeter used by the pads. Assuming that the die has a square aspect ratio, P equals

$$P = \frac{P_{min}}{4\sqrt{A_{die}}} \qquad [14.8]$$

If P is less than one, then the design is core-limited and the estimated die area is probably correct. The following formula will determine the approximate number of ESD devices N_e that will fit between the pads

$$N_e \cong \frac{N_p(W_p + S_e)}{P(W_p + S_p)} \qquad [14.9]$$

where S_e equals the minimum spacing between pads required to fit one ESD structure. If N_e exceeds the number of ESD devices used by the design, then they should all fit into the padring. If there are too many ESD devices, then add the area of the devices that will not fit into the padring to the area of the core and repeat the calculations using equations 14.5 to 14.8.

If the perimeter utilization factor P exceeds one, then the design is pad-limited and the die area must increase. The total die area A_{die} for a pad-limited die with a square aspect ratio equals

$$A_{die} = \frac{P_{min}^2}{16} \qquad [14.10]$$

The pad-limited die will have wasted space equal to the difference between the area estimates of equations 14.6 and 14.10. It is possible to slightly increase the amount of usable die periphery by elongating the die, but reasonable aspect ratios rarely provide enough additional perimeter to transform a pad-limited die into a core-limited one.

14.1.3. Gross Profit Margin

Managers and marketers use die-area estimates to determine the profitability of a design. The figure of merit most often used for this purpose is the *gross profit margin* (GPM), defined as the percentage of the sales price remaining after manufacturing costs have been subtracted. The procedure used to determine GPM is worth examining, as it provides some insight into the economics of integrated circuit manufacture.

The first step consists of computing the number of dice obtainable from one wafer N_d

$$N_d = \frac{\eta \pi d^2}{4A_d} \qquad [14.11]$$

where d represents the diameter of the wafer in millimeters (or mils) and A_d represents the area of the die in square millimeters (or square mils). The *wafer utilization factor* η represents the fraction of the wafer's surface covered by potentially usable dice. Some of the dice around the edges will be incomplete, either because they extend beyond the edge of the wafer or because they fall outside the field of exposure. Wafer utilization factors range from 0.7 to 0.9, depending on die size and photolithography techniques. As an example of the use of this equation, consider a $10mm^2$ die constructed on a 6″ (150mm) wafer with a wafer utilization factor of 0.8. This wafer will yield 1414 dice.

The cost of a functional die C_d can be determined using the following formula

$$C_d = \frac{C_w}{N_d Y_p} \qquad [14.12]$$

where C_w represents the cost of one wafer, including probing and sawing, and Y_p represents the *probe yield*, defined as the fraction of the potentially usable dice that pass wafer probe. Probe yields depend on the area of the die, the complexity of the process, and the robustness of the design. Probe yields of analog integrated circuits usually range from 0.7 to 0.9, although both lower and higher figures are possible. Continuing the previous example, suppose that each 6″ wafer costs $600 and the probe yield equals 85%. Assuming 1414 potential dice per wafer, each good die costs 50¢.

The total cost C_t of an integrated circuit equals

$$C_t = \frac{C_d + C_a}{Y_a} \qquad [14.13]$$

where C_d represents the die cost and C_a the assembly cost (including packaging, symbolization, final testing, storage, and shipping). The *assembly yield* Y_a usually exceeds 0.95 because the vast majority of the defective dice have already been rejected during wafer probe. Continuing the previous example, if each good die costs 50¢, assembly costs 20¢, and the assembly yield equals 0.95, the cost of the finished integrated circuit equals 74¢.

The *gross profit margin* (GPM) is computed from the total cost C_t and the sales price S:

$$GPM = \frac{S - C_t}{S} \cdot 100\% \qquad [14.14]$$

If an integrated circuit costs 74¢ to produce and sells for $1.50, then it will have a GPM of 50.7%. The gross profit margin must cover all the costs associated with running a large company, including sales and distribution, engineering, research and development, fixed overhead, and administrative costs. A GPM of at least 50% is desirable.

14.2 FLOORPLANNING

The final phase of the planning process consists of creating a sketch of the layout, called a *floorplan*, showing the placement of the bondpads and the locations and shapes of all the cells. During the layout, the floorplan serves as a guide for constructing the padring. If any cell requires significantly more or less space than allocated, the floorplan should be revised accordingly. Once most or all of the cells have been completed, the floorplan can be used as a template for assembling the top level layout.

The information required to construct a floorplan includes area estimates for each cell as well as an area estimate for the whole die. The designer must also obtain a complete listing of all pads and the order of their placement. Table 14.2 shows a sample worksheet containing the information needed to produce a floorplan of a small analog integrated circuit.

Having obtained the necessary information, the next step consists of sketching out the padring. Assuming a square die aspect ratio, a 1.33mm^2 die will have dimensions of 1153 × 1153μm. This distance must be rounded off to the nearest increment allowed by the stepper, as determined by the photomask vendor. Many older steppers require the die size to equal an integer number of mils. A die that is 1153μm on a side would become 46mils (1168.4μm) on a side.

TABLE 14.2 Sample floorplanning worksheet.

Device:	Dual operational amplifier
Process:	Standard bipolar, double-level metal
Dimensions in:	Mils
Package type:	8-pin DIP
Die area estimate:	1.33 mm^2 (P_f = 1, R_f = 1.2)
Bondpad width:	3mil (75μm)
Padring width:	100μm estimated
Scribe width:	3mil (75μm)

Circuit Block	Area	Dedicated Pins	Shared Pins
AMP1	0.32mm^2	IN1+, IN1–, OUT1	V+, V–
AMP2	0.32mm^2	IN2+, IN2–, OUT2	V+, V–
BIAS	0.13mm^2	None	V+, V–

Note: AMP1 and AMP2 are identical to each other.

Pin #	Pin Name	Function of Pin
1	OUT1	Output of first amplifier
2	IN1–	Inverting input of first amplifier
3	IN1+	Noninverting input of first amplifier
4	VEE	Negative supply (connect to substrate)
5	IN2+	Noninverting input of second amplifier
6	IN2–	Inverting input of second amplifier
7	OUT2	Output of second amplifier
8	VCC	Power supply

Once the dimensions of the die have been determined, a leadframe must be chosen. Figure 14.4 shows a drawing of a typical 8-pin DIP leadframe. The large square tab in the middle of the drawing is called the *mount pad.* The die must be slightly smaller than the mount pad to allow for misalignment. Given an allowance of 5mils (125μm) per side, an 80 × 100mil mount pad can accommodate a die with maximum dimensions of 70 × 90mil. This leadframe can easily accommodate a 46mil-square die. Given a choice of several leadframes, choose the smallest one that will accommodate the die. Excessively large leadframes may reduce the assembly yield because of wiresweep and sag.

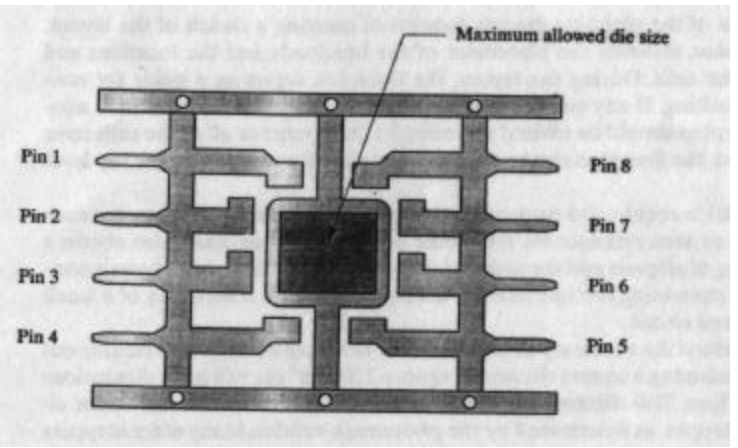

FIGURE 14.4 Sample leadframe drawing for an 8-pin DIP package.

The leadframe in Figure 14.4 illustrates a common arrangement in which the lead fingers actually encircle the mount pad. Thus, while pin one emerges from the top left of the package, the bondwire attaches to its lead finger directly above the mount pad. The bondpads should be placed to obtain the shortest and most direct bondwire routings. This precaution not only minimizes the chance of wires shorting to one another but also reduces the amount of gold wire required to bond the die.

The floorplan should also show the location of the scribe streets. Some processes require the scribe street on the bottom and left sides, others on the top and right sides, and still others place half-width scribe streets on all four sides of the die. All of these arrangements result in the same pattern of scribe streets on the wafer, but each requires a slightly different layout. For the purposes of this example, we will assume that the scribe occupies the top and right sides of the die and that the origin of the layout resides at the lower left corner.

The floorplan sketch includes a rectangle marking the extents of the die and a second smaller rectangle delimiting the area reserved for the core (Figure 14.5). A strip along the top and right-hand sides of the die shows where the scribe fits. The individual cells are represented by rectangles having the appropriate areas. Since this design contains two identical amplifiers, it makes sense to use mirror-image placements of a single amplifier cell. This not only saves layout effort but also ensures that the two amplifiers will have similar electrical characteristics. The placement of the amplifiers must allow wires to route to the appropriate pins. AMP1 connects to pins 2, 3, and 4, while AMP2 connects to pins 6, 7, and 8. AMP1 should therefore reside on the left side of the die and AMP2 on the right. The BIAS block fits into the middle between the two amplifiers. This arrangement produces rather elongated circuit blocks, but there is no reason why this should cause problems. The die's aspect ratio remains square, and the elongation of the amplifier blocks actually helps improve matching by allowing the sensitive input circuitry to be placed

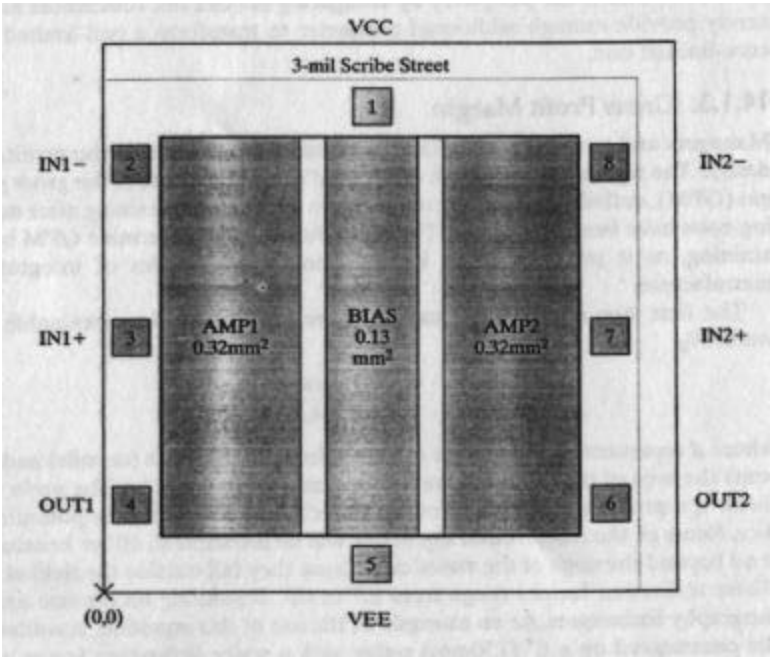

FIGURE 14.5 Floorplan of the eight-pin dual op-amp die.

far away from the power devices. The shape of the bias circuit is somewhat awkward, but not unworkable.

The die area estimate reserved 20% of the core area for routing. This space has been incorporated into the floorplan in the form of two narrow strips running vertically across the entire die. The actual placement of the leads will be determined later; these strips merely reserve room for them.

The next step consists of placing the bondpads. This requires that the floorplan be superimposed on a copy of the leadframe drawing. The bondpads should initially sit adjacent to their respective leadframe fingers (Figure 14.6A). This arrangement results in the shortest bondwires and the largest separation between the wires, but it does not necessarily provide the best interconnection between pads and circuit blocks. The pads can move slightly to accommodate layout, but if they are moved too far the design becomes unmanufacturable. In order to allow automated bonding, the bondwires must not intersect, nor should they even closely approach one another. Figure 14.6B shows an acceptable bonding arrangement, while Figure 14.6C shows an unacceptable one. This arrangement causes the wire for pin #2 to pass too close to the ball bond for pin #1. Similarly, the wire for pin #3 comes too close to the ball bond for pin #2. These faults make it almost impossible to bond the die without damaging some of the wires. Once the bondpad arrangement has been tentatively decided, the designer should forward a bonding diagram to the assembly site to allow them to check for potential bonding problems.

The floorplan in Figure 14.5 uses the pad arrangement shown in Figure 14.6B, and places the three input/output pads of AMP2 directly opposite the three corresponding input/output pads of AMP1. This symmetric placement helps simplify the connection of these pads to their respective amplifiers. The two power pads move to the top and bottom of the die. These locations not only help minimize interference between adjacent bondwires but also help to ensure that the power leads can run to all three blocks.

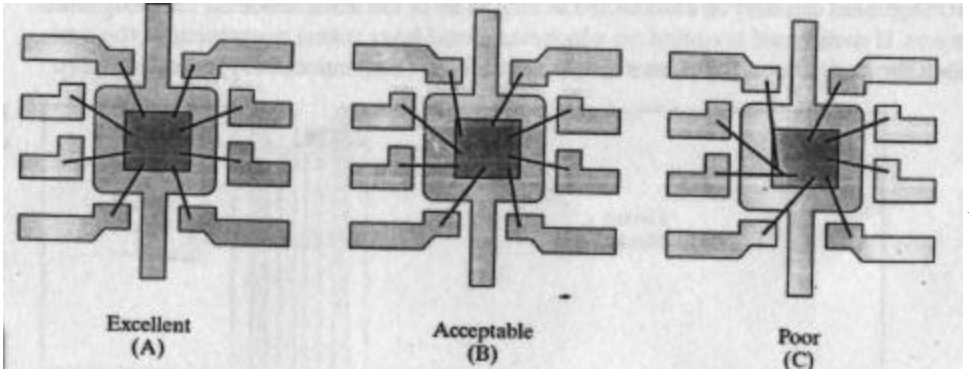

FIGURE 14.6 Three possible placements of bondpads for an 8-pin leadframe.

If the design incorporates high-current circuitry, then the designer should check the routing of high-current leads. Electromigration sets a lower limit on the width of a high-current lead, but metal resistance often forces the use of much wider leads. All high-current leads should be kept as short as possible to minimize unnecessary metal resistance. The anticipated locations of each high-current lead should be marked on the floorplan, along with the equivalent DC current that they must conduct. The resulting diagram will show whether any awkward or unnecessarily long leads exist.

Figure 14.7 shows a diagram of the dual op-amp highlighting the locations of the high-current leads. The VCC lead routes directly across the top of the bias cell. This is an acceptable arrangement for a double-level-metal layout because the lead can be routed in metal-2 and the circuitry in metal-1. The lead routing does place a limi-

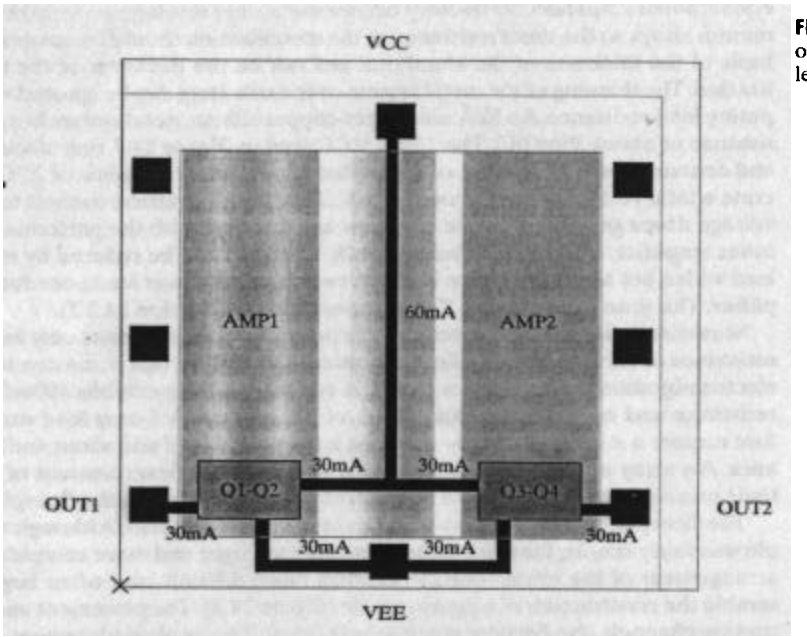

FIGURE 14.7 Floorplan of dual op-amp showing the routing of leads to transistors Q1 to Q4.

tation on the layout of the BIAS block, which might not have otherwise been apparent. If the BIAS block must use metal-2, then the power lead can slide laterally into either of the two routing channels.

Although the floorplan in Figure 14.7 explicitly shows the VEE leads connecting to each amplifier, in practice these leads form part of the scribe seal metallization. Most dice arrange their power and ground return signals to take advantage of the scribe seal metallization as much as possible, and this design is no exception. An additional width of metal placed around the periphery of the die abutting the scribe seal allows the metal to carry additional current. Substrate contacts placed under this metallization augment those in the scribe seal and form a significant portion of the substrate contact system of the die.

As previously mentioned, electromigration determines the minimum width of high-current leads. The minimum allowed lead width W_{min} (in microns) equals

$$W_{min} = \frac{10^{12} I_{DC}}{J_{max} t} \qquad [14.15]$$

where I_{DC} is the equivalent DC current in amps, J_{max} equals the maximum allowed current density in A/cm^2, and t is the thickness of the metal in Angstroms (Å). The values for J_{max} and t depend on the process and operating conditions (Section 14.3.3). If the lead passes over oxide steps, then the minimum thickness of the lead at the crossing point should be used for electromigration calculations.

For example, suppose $J_{max} = 5{\cdot}10^5$ A/cm^2 and t = 8kÅ. Given these values, Equation 12.14 indicates that a lead carrying 60mA requires a width of 15μm. The sheet resistance R_s for a metal lead can be computed using the following formula

$$R_s = \frac{10^8 \rho}{t} \qquad [14.16]$$

where ρ is the resistivity of the metal in Ω·cm and t is the thickness of the metal in Angstroms (Å). The resistivity of aluminum containing 0.5% copper and 2% silicon

equals about 2.8μΩ·cm. Refractory barrier metals are much more resistive than aluminum alloys, so the sheet resistance of the metallization should be computed on the basis of the thickness of the aluminum and not on the thickness of the full metallization. The thinning of the metal system over oxide steps can be ignored when computing lead resistance. An 8kÅ aluminum-copper-silicon metal system has a sheet resistance of about 35mΩ/□. The 15μm VCC lead in Figure 14.7 runs about 1000μm and contains about 67 squares of metal that have a total resistance of 2.3Ω and generate a total voltage drop of about 140mV. Since both amplifiers connect to this lead, voltage drops generated by one amplifier can interfere with the performance of the other amplifier, a problem called *crosstalk*. Crosstalk can be reduced by making the lead wider, but a better solution is to run two separate power leads, one for each amplifier. This is an example of a *Kelvin connection* (see Section 14.3.2).

Sometimes vias must be placed in large power leads. The vias not only increase the resistance of the lead but also limit the amount of current that it can conduct before electromigration causes the vias to fail. A typical $1\mu m^2$ via exhibits 100mΩ of series resistance and can safely conduct 25mA of DC current. A 1-amp lead would therefore require a minimum of forty vias, which together would add about 4mΩ of resistance. An array of vias that large would consume a significant amount of area, and their presence would have to be considered while constructing the floorplan.

The floorplan for the dual op-amp has now been completed. Although this example was fairly simple, the same principles apply to larger and more complex dice. The arrangement of the circuit blocks becomes more difficult, and often begins to resemble the construction of a jigsaw puzzle (Figure 14.8). The placement and width of routing channels also become much more critical. The careless placement of a block can easily constrict a routing channel. The resulting *choke points* can needlessly complicate routing, especially if they are not found until the routing has begun. The layout of Figure 14.8 contains two obvious choke points.

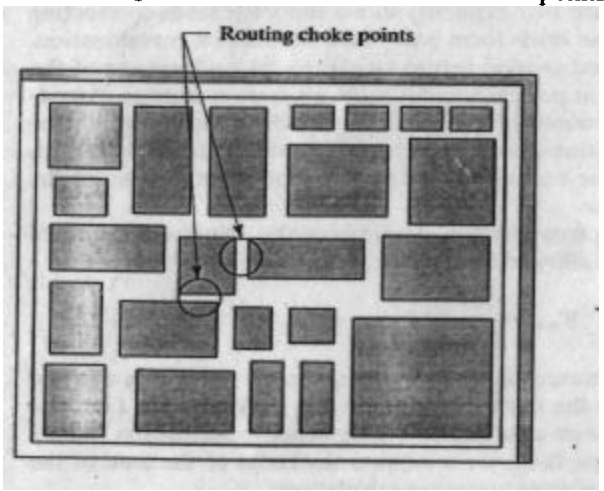

FIGURE 14.8 Floorplan of a complex die showing two potential choke points in the routing.

14.3 TOP-LEVEL INTERCONNECTION

Most analog and mixed-signal layouts actually benefit from manual interconnection. Autorouting software can interconnect blocks very quickly, but a human designer better understands such factors as wiring resistance, electromigration, noise coupling, and heat distribution. A skilled layout designer also takes advantage of every

opportunity to insert substrate contacts, bypass capacitors, probe points, and test pads. Even if an autorouter is used, the layout designer must still verify that each analog signal has been properly routed. This process of verification (and the inevitable corrections) may require as much time as manual interconnection.

Some designers advocate running most of the wires across or through the circuit blocks themselves, a technique called *maze routing*. Others advocate running the wires alongside the individual blocks, a technique known as *channel routing*. Maze routing can save 5 to 10% of the initial die area, but it often requires two or three times as long to complete. Most modern designs use channel routing because it is quicker to implement and easier to modify.

14.3.1. Principles of Channel Routing

Channel routing requires at least two levels of interconnection. These consist, at a minimum, of one level of metal and one level of polysilicon. Unsilicided gate poly usually has a sheet resistance of 20 to 50Ω/□, while silicided poly can routinely achieve sheet resistances of less than 5Ω/□. Many signals can tolerate the insertion of short poly jumpers, especially if these are silicided. On the other hand, most signals cannot tolerate the resistance of long poly runs. This consideration makes it difficult to produce a compact wiring arrangement using only one level of metal, so most modern designs use at least two. Multiple metal layers reduce the need for poly routing, but the use of limited amounts of poly can still help clear congested wiring channels. As long as the designer carefully chooses which signals to route in poly, the presence of long polysilicon traces has little or no impact on circuit performance.

In a double-level-metal design, channel routing allocates one layer of metallization for vertical routing and a second for horizontal routing. It matters little which layer runs horizontally and which vertically. Figure 14.9 shows portions of two routing channels and an intersection between them. As this example shows, leads can exit from either routing channel at any point by jumping from one metal layer to the other. This orderly arrangement can only be maintained as long as all of the leads reside on the designated layers. If each signal is routed on whichever metal layer seems convenient at the time, then the design soon becomes a tangle of unwieldy (and unnecessary) metal jumpers.

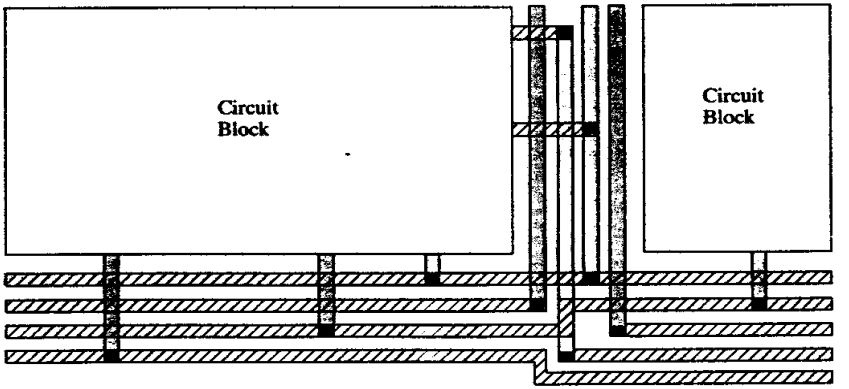

FIGURE 14.9 A portion of a channel-routed layout.

The leads on successive layers should run at right angles to one another. For example, metal-3 leads should run at right angles to metal-2 leads. Similarly, poly should run at right angles to metal-1. Thus, if poly runs horizontally, metal-1 should run vertically, metal-2 horizontally, and metal-3 vertically. This arrangement minimizes the need for jumpers and results in the best utilization of channel space.

Metal systems are often specified in terms of their *metal pitch*. The metal pitch P_m equals the sum of the minimum drawn metal width W_m and the minimum drawn metal spacing S_m:

$$P_m = W_m + S_m \quad [14.17]$$

For example, a process that can fabricate 2μm leads spaced 1.5μm apart has a metal pitch of 3.5μm. The width of a wiring channel can be determined using the formula

$$W_c = NP_m + S_m \quad [14.18]$$

where W_c equals the width of a wiring channel that can just accommodate N minimum-width leads. Continuing the previous example, a six-lead wiring channel would require a width of 22.5μm. The width W_c includes the space on either side of the channel between the leads and adjacent metallization.

In order to ensure optimal packing, the vias should not require enlarged metal heads. This requirement will be satisfied if the following inequality holds

$$W_m \geq W_v + 2O_{mv} \quad [14.19]$$

where W_v equals the minimum width of a via and O_{mv} equals the minimum overlap of metal over via. If this inequality does not hold, then W_m should be increased. For example, suppose a process is capable of fabricating a 2μm metal lead, but it requires 1.5μm vias and a metal overlap of via of 0.5μm. The width of the metal head required to contain the via is 2.5μm, which is 0.5μm larger than the specified metal width. In order to maintain proper packing in the wiring channels, the designer should increase the width of the metal leads in the channel to 2.5μm. The increased lead width wastes a little area, but it greatly simplifies wiring. Figure 14.10A shows a layout employing enlarged via heads, while Figure 14.10B shows the same layout reworked using wider leads. Despite the presence of a little wasted space, the layout of Figure 14.10B is obviously preferable to that of Figure 14.10A.

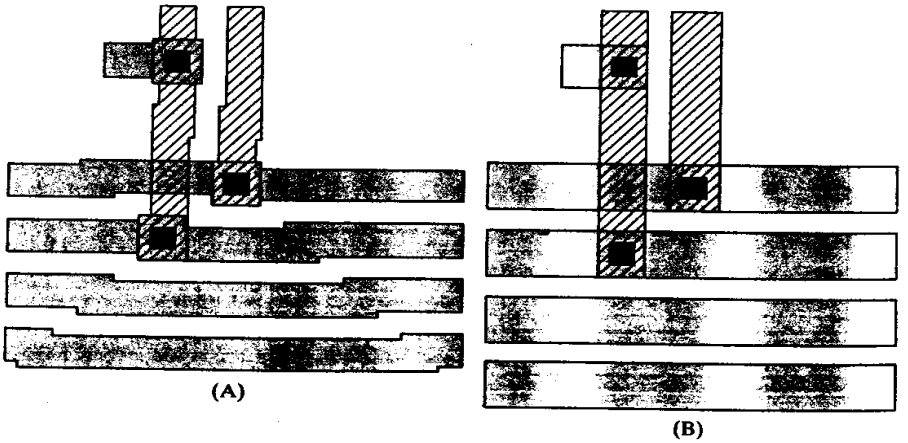

FIGURE 14.10 (A) A layout that requires enlarged via heads (B) becomes much simpler when the lead width is slightly increased.

In most designs, two or three routing channels carry a large percentage of the signals. These *primary routing channels* usually intersect somewhere near the center of the die. These intersections may easily become choke points unless the channels are made quite wide. As a conservative rule, each primary routing channel should contain space for about 20% of the top-level signals. A design containing 100 top-level signals requires room for about 20 leads in each of its primary routing channels. The

width of the primary wiring channels can decrease as they approach the edges of the die. Similarly, the feeder channels branching off the primary channels can be made proportionately narrower. The resulting pattern of routing channels resembles the path of watercourses across a plain. Even the narrowest channels should always allow capacity for 3 to 5 signals, as it is very difficult to guess exactly where leads need to route, and it is very difficult to increase channel widths once the top-level interconnection has commenced.

Poly routing can reduce the width of the primary routing channels by perhaps 30%. This reduction in width assumes that about a third of the leads are routable in poly. The use of poly routing under both horizontal and vertical routing channels can lead to gridlock in the vicinity of major intersections. This type of gridlock is best avoided by running poly leads in only one direction, preferably in the same direction as metal-2. If possible, one should align the largest (or longest) primary routing channel so that it contains poly.

14.3.2. Special Routing Techniques

Certain leads require special consideration during routing. Some leads are particularly sensitive to voltage drops or noise coupling, while others require wider metal to minimize voltage drops and to prevent electromigration. This section discusses some of the techniques used to handle these concerns.

Kelvin Connections

The metallization resistance, although small, is not always negligible. Consider an amplifier circuit containing a pair of matched bipolar transistors whose emitters connect to a ground return line carrying 100μA (Figure 14.11A). The two emitter leads do not tap into the ground return at the same point, so the ground current generates a small voltage differential between them. Suppose the ground return lead between points A and B contains ten squares of 30mΩ/□ metal. A 100μA current flowing through 0.3Ω develops a voltage of 30μV. Any variation in ground current produces a corresponding variation in this voltage drop, which the circuit amplifies. If the ground current fluctuates by ±10% and the amplifier has 80dB of voltage gain, then the output will fluctuate by 0.3V! This is clearly an unacceptable situation.

The magnitude of the voltage drop in the ground lead depends on the distance between points A and B. Figure 14.11B shows the same circuit with one modification: both emitter leads now return to a common point C. Since the leads return to the same point, the ground current cannot generate any differential between them. Ground drops elsewhere along the lead cause the voltage on both emitters to vary in unison, but most circuits exhibit a high degree of immunity to such *common-mode variations.*

The common point C is called a *star node* or a *Kelvin connection.* These points are often represented on schematics by leads entering a solder dot at 45° angles, as

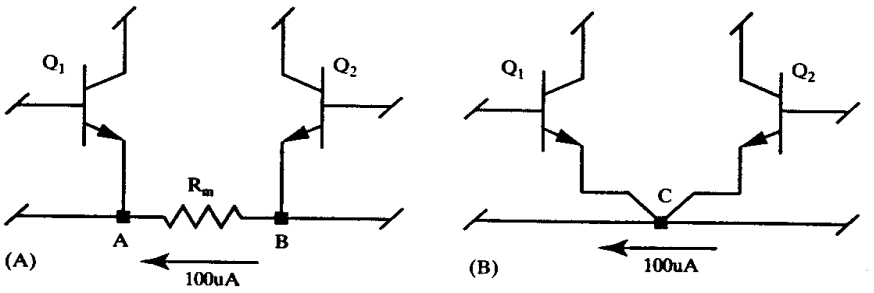

FIGURE 14.11 (A) The effects of voltage drops in a ground return line (B) can be eliminated through the use of a Kelvin connection.

in Figures 4.11 and 4.12. Kelvin connections have many other applications. Figure 14.12A shows a pair of Kelvin connections that allow accurate sensing of the voltage developed across a metal resistor. Leads F_1 and F_2 carry a large current through resistor R_1, while leads S_1 and S_2 connect the resistor to a sensing circuit. F_1 and F_2 are called *force leads*, while S_1 and S_2 are called *sense leads*. Figure 5.16 shows sample layouts of metal resistors with force and sense leads. The sense leads carry very little current to minimize the voltage drops occurring in them. In high-precision applications, the currents flowing through the sense leads are carefully balanced, and the layouts of the leads are adjusted so that each contains the same number of squares. This precaution ensures that any voltage drops that do occur in the sense leads are common-mode variations.

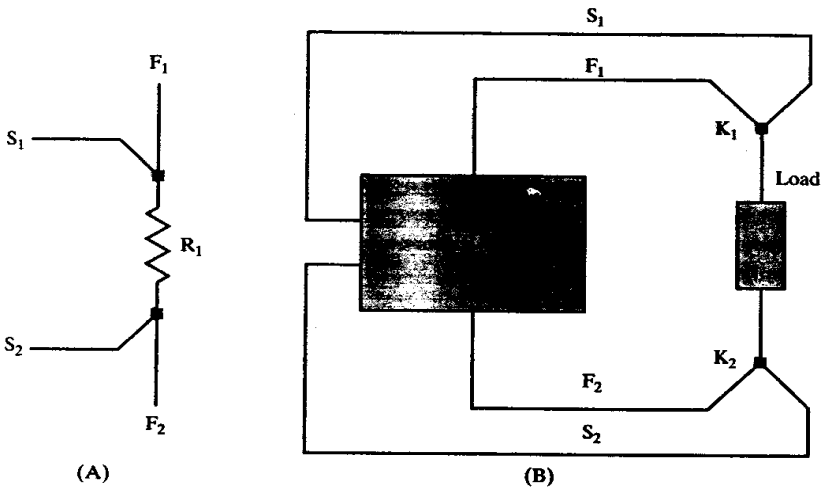

FIGURE 14.12 Additional applications of Kelvin connections: (A) metal sense resistor and (B) remote sensing.

Figure 14.12B shows another application for Kelvin connections. A voltage regulator, VR_1, must provide a large amount of current to an external circuit. Voltage drops inevitably occur in power lead F_1 and in ground lead F_2. A separate set of sense leads, S_1 and S_2, is employed to sense the voltage across the load at Kelvin connections K_1 and K_2. This arrangement ensures that voltage drops in the force leads do not degrade the regulation of the circuit. The manufacturers of commercial power supplies call this arrangement *remote sensing*. Integrated voltage regulators sometimes support remote sensing by providing separate force and sense pins. If the package does not provide enough pins to accommodate separate force and sense connections, two bondwires can be connected to the same pin to eliminate voltage drops in the IC metallization and the bondwires. Even if the package cannot accommodate double bonding, the designer can still run separate force and sense leads to the output and ground bondpads.

Noisy Signals and Sensitive Signals

Broadly speaking, electrical noise consists of any unintended or undesired signal. All electrical devices generate some noise, but the level of this ***device noise*** is so low that it only affects very sensitive circuits. Most of the noise problems encountered in integrated circuits are caused by capacitive coupling of signals from one circuit node to another. A capacitor appears whenever leads cross or run alongside one another. Although these capacitors are very small, the amount of energy coupled through

them increases with frequency. At sufficiently high frequencies, even intersections between minimum-width leads can couple objectionable amounts of noise energy from one circuit to another.

In practice, capacitively coupled noise becomes a concern only if one or more signals contain appreciable energy at frequencies in excess of 1MHz. Most analog signals have relatively little high-frequency content, but digital signals are quite another matter. The crisp transitions so prized by digital designers generate high-frequency harmonics extending well beyond 1GHz. Each digital signal generates a burst of noise every time it switches states. All digital signals that experience state transitions during normal circuit operation should be considered potential noise sources. All power switching transistors should be considered noise sources, as should signals connecting to pins seeing rapid transients during normal operation.

The mere existence of any number of noisy signals is harmless. Problems only arise if the integrated circuit also contains one or more signals that are unusually sensitive to capacitively coupled noise. Analog signals are far more noise-sensitive than digital signals, but not all analog signals are equally sensitive. The most sensitive nodes are those that carry very low-level signals at high impedance levels. For example, the input of an amplifier is far more noise sensitive than its output because any signal present at the input is amplified by the gain of the amplifier. Furthermore, the output of an amplifier is usually low-impedance, while its inputs are often very high-impedance. The following types of signals are among the most noise sensitive:

- Inputs to high-gain amplifiers and precision comparators
- Inputs to analog-to-digital converters (DACs)
- Outputs of precision voltage references
- Analog ground lines to high-precision circuitry
- Precision high-value resistor networks
- Very low-level signals, regardless of impedance
- Very low-current circuitry of any sort

Most layout designers do not possess the knowledge and experience required to correctly identify all of the noisy and sensitive nodes in a complicated analog circuit. Instead, the circuit designer must identify these signals, preferably by marking them on the schematic in some distinctive manner. Once the layout designer understands which signals are noisy and which are sensitive, the signals can be routed appropriately.

Noisy signals should not run on top of sensitive signals, or *vice versa.* If a crossing must occur, the area of intersection should be minimized. The circuit designer should examine each crossing to determine if it requires electrostatic shielding (Section 7.1.7). The usual method of constructing such shielding in double-level-metal designs is to run one signal in poly and the other in metal-2. A plate of metal-1 interposed between the two signals acts as an electrostatic shield. The shield should connect to a quiet low-impedance node such as an analog ground line. The shielding plate should extend beyond the area of intersection by 2 to 3μm to block fringing fields.

Noisy signals should not run adjacent to sensitive signals. If such an arrangement seems unavoidable, then the layout designer should run another signal between the two. The shield lead may consist of some other relatively low-noise, low-impedance signal, such as the output of a digital logic gate that seldom changes states. Alternatively, it may consist of an extra ground line or supply line added to the layout specifically to shield the noisy signal from the sensitive one. In order for the shield lead to perform its function, it must connect to a fairly low-impedance node in the

circuit. Supply and ground lines satisfy this requirement, as will the output of digital logic gates.

Whenever possible, the designer should place noisy circuitry as far away from sensitive circuitry as possible. This usually requires that noisy circuitry occupy one portion of the die and sensitive circuitry another. This type of arrangement often proves beneficial from other standpoints because it separates sensitive circuitry from large power devices.

Sensitive signals should never run farther than necessary. The shorter these signals, the fewer opportunities they provide for noise coupling. A layout designer should always try to place analog circuits so that the sensitive signals running between them do not pass through other circuit blocks. Although this is not always possible, the fewer long sensitive leads a design contains, the easier it is to prevent capacitive coupling problems.

14.3.3. Electromigration

As discussed in Section 4.1.2, electromigration limits the current density that can safely flow through metallization. If the current density becomes too large, the pressure of carrier collisions on the aluminum metal atoms causes a slow displacement of the metal. This eventually results in voiding or lateral extrusions (*whiskers*) that can short adjacent signals.[1]

Electromigration obeys a modified Arrhenius relationship that was first discovered by J. R. Black, and is therefore called ***Black's Law***:[2]

$$MTF = \frac{1}{AJ^2} e^{\frac{E_a}{kT_j}} \qquad [14.20]$$

where MTF is the mean time to metallization failure, in hours, A is a rate constant having units of $cm^4/A^2/hr$, J is the current density passing through the lead in A/cm^2, E_a is the activation energy in electron volts (eV), k is Boltzmann's constant ($8.6 \cdot 10^{-5}$eV/K), and T_j is the absolute junction temperature in Kelvin.

Since the rate of electromigration varies exponentially with temperature, high-temperature testing can accelerate the failure process to allow experimental determination of constants A and E_a. On the basis of such testing, one can derive a maximum current density, J_{max}, corresponding to any desired operating life. As one might expect, J_{max} is a strong function of temperature. A typical value for copper-doped aluminum is $5 \cdot 10^5 A/cm^2$ at 85°C. This value is widely accepted throughout the industry for computing the required width of metallization in devices operating at junction temperatures of 85°C or less. The current that an arbitrary lead can carry equals

$$I_{max} = 10^{-9} J_{max} W t \qquad [14.21]$$

where I_{max} is the maximum current (in mA) that the lead can safely carry, J_{max} is the maximum allowed current density in A/cm^2, W is the width of the lead in microns, and t is the thickness of the metallization in Angstroms (Å). A factor of 10^{-9} is inserted in equation 14.21 to balance the units. As an example of the use of this equation, suppose a 10kÅ lead is constructed of copper-doped aluminum having $J_{max} = 5 \cdot 10^5 A/cm^2$. If this lead is 10μm wide, then it can conduct no more than 50mA.

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[1] J. R. Black, "Electromigration—A Brief Survey and Some Recent Results," *IEEE Trans. Electron Devices*, Vol. ED-16, #4, 1969, pp. 338–348.

[2] J. R. Black, "Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons," *Proc. 1967 Ann. Symp. on Reliability Physics*, IEEE Cat 7-15C58, 1967.

Metal leads passing over oxide steps often experience less-than-perfect step coverage. Most processes state a minimum guaranteed step coverage in terms of a percentage of normal metal thickness. The carrying capacity of any lead crossing an oxide step must be derated by the percentage step coverage. Standard bipolar processes typically quote a 50% step coverage figure. Thus, if the 10μm lead discussed above crosses an oxide step, then its current carrying capacity would drop to 25mA.

Most parts are assumed to experience junction temperatures of 85°C or less for the majority of their operating life, even if the parts are rated for higher junction temperatures. Certain types of devices, particularly those that experience substantial differences between junction and ambient temperatures, may actually operate at high temperatures for long periods of time. If such conditions are anticipated, then the current carrying capacity of the leads must be multiplied by a derating factor, D, equal to

$$D = e^{\frac{E_a}{2k}\left(\frac{1}{T_j} - \frac{1}{T_o}\right)} \qquad [14.22]$$

where T_o is the junction temperature at which I_{max} was computed in degrees Kelvin, T_j is the anticipated maximum operating temperature in Kelvin, E_a is the activation energy in electron volts, and k is Boltzmann's constant. A typical activation energy for electromigration-induced voiding in pure aluminum is 0.5eV, while values for copper-doped aluminum[3] are closer to 0.7eV. Suppose we wish to compute the derating factor for 125°C (398K), given an original current density calculation performed at 85°C. Assuming $E_a = 0.7$eV, the derating factor D equals 0.32. Therefore a lead that can safely carry 25mA at 85°C can safely carry only 32% of this current, or 8mA, at 125°C.

If a lead does not carry a constant current, but rather a time-varying current, then its current-handling capability is increased. One type of time-varying current, consisting of short pulses repeated at frequent intervals, often occurs in digital logic and MOS gate drivers. The derating factor D for pulsed-current operation equals[4]

$$D \cong \frac{1}{d^2} \qquad [14.23]$$

where d is the duty cycle of the signal and D is the derating factor. For example, a lead conducting current only 50% of the time has a duty cycle of 0.5 and a derating factor of 4. If the lead can safely carry 25mA DC, then it can handle 50mA pulses at a duty cycle of 0.5. The derating factor computed in equation 14.23 assumes that the pulsed current flows only in one direction. The rate of AC electromigration is somewhat slower than the rate of DC electromigration because some of the displacement occurring during one phase reverses during the other phase. The magnitude of the derating factor for AC operation is difficult to determine because it varies with the exact waveforms involved, but a conservative estimate is $D = 1.5$. Thus, if a lead could handle 50mA unipolar pulses, then it could handle 75mA bipolar pulses.

Another common type of time-varying signal consists of a sinusoid, or sine wave. A lead can handle a sinusoidal current with a peak value equal to about three times its DC rating. Thus, if a lead can handle 25mA DC, then it can handle a sinusoidal current with a peak value of 75mA (which equals 150mA peak-to-peak or 106mA root-mean-square).

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[3] H. V. Schreiber, "Activation Energies for the Different Electromigration Mechanisms in Aluminum," *Solid-State Elect.*, Vol. 24, 1981, pp. 583–589.

[4] J. S. Suehle and H. A. Schafft, "Current Density Dependence of Electromigration t_{50} Enhancement Due to Pulsed Operation," *Proc. International Reliability Physics Symposium*, 1990, pp. 106–110.

Bondwires also have limited current-carrying capability. If too much current flows through a wire, its internal temperature may rise to the point where it fails, either gradually through electromigration, or suddenly through fusing or burning. Military specification Mil-M-38510 sets a maximum allowed current, I_{max}, (in mA) equal to[5]

$$I_{max} = kd^{3/2} \qquad [14.24]$$

where d is the bondwire diameter in mils and k is a constant equal to approximately 480mA·mil$^{2/3}$ for aluminum and 650mA·mil$^{2/3}$ for gold. This law is derived from the classical three-halves power law of radiative processes.[6] While it applies to long bondwires suspended in air, it does not apply to bondwires embedded in plastic or other encapsulating materials. These substances act as thermal insulators and prevent radiative heat transfer. The temperature of the wire is therefore determined solely by conduction of heat through the wire to its endpoints and through the encapsulation. Assuming that the wire is relatively long and that the encapsulation is a good thermal insulator, then the temperature of the wire depends only on the amount of power dissipated and not on its surface area or volume. Under these conditions, the current-handling capability of a bondwire scales linearly with its diameter. Large-diameter bondwires are placed under a disadvantage when they are encapsulated because they do not gain the benefit of their larger surface area.

In practice, bondwires that are less than about 100mil long conduct enough heat to their ends to produce a noticeable increase in their current-carrying capacity.[7] For this reason, most designers use slightly larger current values than Mil-M-38510 suggests. Gold wires encapsulated in plastic are often scaled using the rule of "one amp per mil of diameter," and aluminum wires are usually rated to carry about half the current of an equivalent gold wire. Aluminum wires are not allowed to carry as much current as gold wires because they are more vulnerable to electromigration and high-temperature corrosion. Conservative designers may wish to apply the Mil-M-38510 values of 650mA/mil for gold and 480mA/mil for aluminum, and to allow these to scale linearly with diameter if the wires are encapsulated, and to scale with the three-halves power of diameter if they are not.

14.3.4. Minimizing Stress Effects

The coefficients of thermal expansion of packaging materials rarely match that of silicon, and encapsulation usually takes place at an elevated temperature (Section 7.1.5). The stresses that accumulate as the die cools become permanently frozen into the finished part. On larger dice, or on those mounted using solder or gold eutectic, the stress levels at the corners of the die may become severe enough to damage the die.[8] Common forms of damage include sheared bondwires, broken metal traces, and delamination of the protective overcoat from the underlying metallization.

Some assembly sites prohibit the placement of circuitry in the stress-prone regions around the corners of the die. The prohibited regions usually take the form of *stress triangles* extending some 5 to 10 mils (125 to 250μm) from each corner of the die (Figure 14.13). The designer should not place circuit components, leads, or bond-

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[5] "Maximum Current in Wires," *Semiconductor Reliability News*, Vol. I, #10, 1989, p. 9.

[6] W. H. Preece, "On the Heating Effects of Electric Currents," *Proc. Roy. Soc. (London)*, April 1884, December 1887, April 1888.

[7] From bondwire fusing data given in "Fusing Currents of Bond Wires," *Semiconductor Reliability News*, Vol. VIII. #12, 1996, p. 8. See also B. Krabbenborg, "High Current Bond Design Rules Based on Bond Pad Degradation and Fusing of the Wire," *Microelectronics Reliability*, Vol. 39, 1999, pp. 77–88.

[8] J. R. Dale and R. C. Oldfield, "Mechanical Stresses Likely to be Encountered in the Manufacture and Use of Plastically Encapsulated Devices," *Microelectronics and Reliability*, Vol. 16, 1977, pp. 255–258.

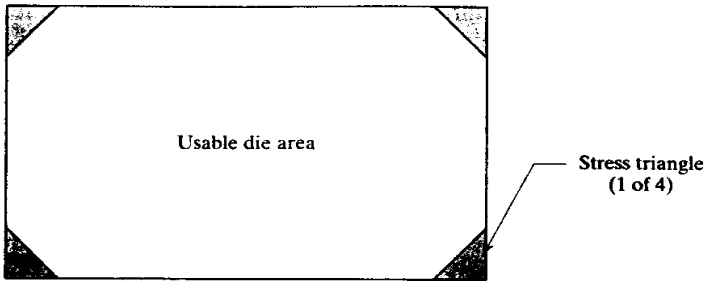

FIGURE 14.13 Layout of a die showing the placement of stress triangles.

pads in these triangles. Test structures can still reside in the stress triangles, as can identification markings and alignment structures.

Stress triangles are usually added to large dice, but not to small ones. The benefits of adding stress triangles to a large die outweigh the relatively small percentage of die area they consume. The stress levels on a small die are lower, yet the stress triangles consume a larger fraction of the available area. At some point, the triangles become more burdensome than they are worth. Most dice under 10kmil^2 (6.5mm^2) do not incorporate stress triangles, and those under 20kmil^2 (13mm^2) often leave them off unless the die experiences unusually stressful conditions, such as solder mounting or gold eutectic bonding.

Certain precautions should always be taken when placing components in the corners of a die. Matched components should never occupy the corners of a die (Section 7.2.6). If possible, one should also avoid placing bondpads in the corners of a die to minimize the possibility of sheared bonds. This prohibition does not apply to trimpads and testpads since neither of these receives bondwires.

Leads should not make right angles near a corner of the die. Stresses concentrate on the outside vertex of such a lead, and this can, in turn, lead to delamination and cracking of the protective overcoat. The designer should insert a short 45° segment into each such lead to help distribute the stresses more evenly (Figure 14.14A). This precaution helps prevent delamination and subsequent damage to the metal system.

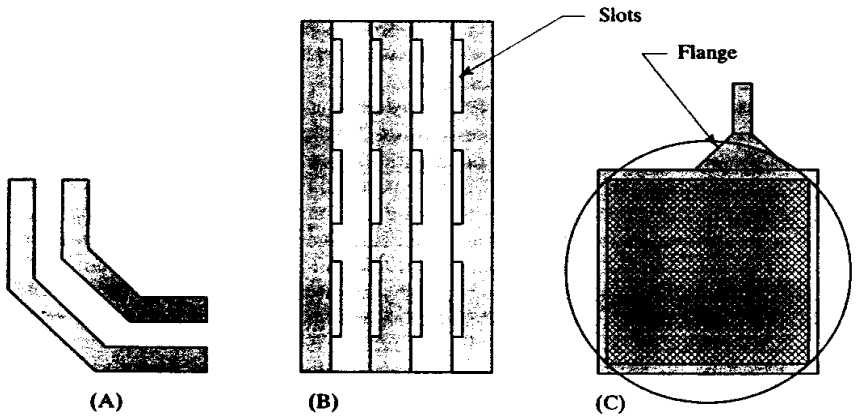

FIGURE 14.14 Various stress-reduction techniques: (A) 45° bends in leads, (B) slots in a wide metal-2 lead, and (C) flanged bondpad.

The presence of large areas of top-level metal near the corners of a die can also cause delamination. The planarization techniques that improve the step coverage of upper-level metal also eliminate the irregularities that help lock the protective overcoat to the die. The addition of an array of narrow slots in the metal helps restore these irregularities and consequently discourages delamination. The slots should be

oriented in the same direction that the current flows through the lead so that they do not greatly reduce its effective cross-sectional area (Figure 14.14B). Leads less than 1mil (25μm) wide generally do not require slots. An array of vias placed between two levels of metal also produces surface irregularities that will lock the protective overcoat in much the same way that the addition of slots will. Thus arrays of vias do not require the addition of slots.

The bonding process also produces high levels of stress. Although this stress only lasts for an instant, it can still damage adjacent metal traces or components. Most processes therefore define a circular exclusion zone around each ball bond and a rectangular or trapezoidal exclusion zone around each wedge bond (Section 13.4.2). Leads that do not connect to the bondpad should not enter this zone, and active circuitry should also reside outside it. Many designers also add a triangular or rectangular *flange* of metal to each lead entering a bondpad (Figure 14.14C). This helps ensure that the stresses associated with bonding do not sever the lead from the bondpad. Modern bonding equipment has minimized the need for these flanges by more accurately controlling the forces applied during bonding, but the flanges consume so little area that it seems unreasonable to eliminate them.

14.4 CONCLUSION

A layout designer must understand not only how to design individual components but also how to interconnect these components to form a complete die. This chapter has touched upon the skills required to predict the size and structure of the die, and those required to actually assemble it. These are perhaps the most difficult of all of the skills the layout designer must learn. They partake of the essential character of all analog layout, in that they are largely arts and not sciences. As such, they require a certain degree of intuition and sound judgment that can only be learned through experience. The information presented here represents only a foundation, and the designer must continue to learn through actually practicing the art of layout.

14.5 EXERCISES

Refer to Appendix C for layout rules and process specifications.

14.1. Estimate the area of the following components in a standard bipolar process. Show all computations and state all assumptions used in the estimations.
- a. 250kΩ of 8μm-wide HSR resistance.
- b. A minimum-area lateral PNP transistor.
- c. 100pF of junction capacitance (assume 1.8fF/μm^2).
- d. A power NPN transistor with an emitter area of 1200μm^2.
- e. A bondpad for 1.2mil ballbonded gold wire.

14.2. Estimate the total area of a circuit laid out in standard bipolar using single-level metallization containing 410kΩ of 6μm HSR resistance, 55kΩ of 8μm base resistance, 50pF of junction capacitance (at 1.8fF/μm^2), eleven minimum NPN transistors, seven minimum lateral PNP transistors, two split-collector lateral PNP transistors, one 4X lateral PNP, and one power NPN transistor requiring an emitter area of 660μm^2. Justify your choice of packing factor.

14.3. Compute the core area of a design containing six cells having the following areas: 0.35, 0.27, 0.21, 0.18, 0.10, and 0.08mm^2. The design also includes two power transistors that each consume 0.77mm^2. The design will be laid out in double-level metal and contains about fifty top-level signals. Justify your choices of routing and packing factors.

14.4. Compute the estimated die area for each of the following designs. Assume that all designs require a bondpad width of 75μm, a spacing between adjacent bondpads of 65μm, and a scribe width of 75μm. State whether each design is core-limited or pad-limited.

a. Core area of 10.1mm^2 using 23 pads.
b. Core area of 1.49mm^2 using 42 pads.
c. Core area of 8.8mm^2 using 11 pads.

14.5. Using the parameters specified in Exercise 14.4, estimate the number of bondpads that can be packed around the periphery of a square die having a total area of 3.9mm^2. How many additional pads could be obtained if the die had an aspect ratio of 1.5:1?

14.6. A device with a die area of 7.6mm^2 is fabricated on 150mm^2 wafers. Assume a wafer utilization factor of 0.85. (A) Approximately how many dice will each wafer yield? (B) If each wafer costs $650 and yields 77% functional dice, what is the cost of a single functional die? (C) If packaging and final testing costs 11.5¢ per device and 97% of devices pass the final test, what is the cost of a completed integrated circuit? (D) If the device is sold for 83¢, what is the GPM? (E) What would be a more reasonable sale price, and why?

14.7. Suppose an improved testing technique increases the probe yield of the device in Exercise 14.6 to 92%. This technique adds 4¢ to the cost of each die probed. Is it worthwhile to implement the new technique?

14.8. A certain integrated circuit contains four operational amplifiers, each with a cell area of 0.41mm^2. The circuit also contains a bias circuit that consumes 0.15mm^2. This circuit requires fourteen bondpads: VCC, VEE, IN1+, IN1–, OUT1, IN2+, IN2–, OUT2, IN3+, IN3–, OUT3, IN4+, IN4–, and OUT4. VCC and VEE are the power and ground pins, respectively. The remaining pins are the inputs and outputs of each of the four amplifiers. The package has fourteen pins, with pin #1 bonded to the top center of the die and the remaining pins arranged in counterclockwise order. (A) Suggest a reasonable pinout for this device. (B) Draw a die floorplan showing the placement of each of the five cells of this design. (C) Each amplifier requires high-current leads to VCC, VEE and its output pin. Assuming that the design uses only a single level of metallization, draw a diagram illustrating a suitable routing pattern.

14.9. A voltage reference circuit contains a reference cell occupying 0.13mm^2 and a small power transistor requiring 0.16mm^2. (A) Assuming the die uses single-level metallization and a hand-packed layout, estimate the core area of the die. (B) Estimate the complete die area assuming a 110μm-wide scribe and a total of three bondpads, each requiring a total area of 9000μm (pad plus ESD protection). (C) Draw a die floorplan for this device. The power transistor must connect to the VIN and VOUT pads, which are at the top right and bottom right of the die, respectively. The reference cell must connect to the GND pin, which must lie somewhere along the left side of the die. (D) Indicate the preferred location for critical matched devices.

14.10. An octal buffer circuit contains eight buffers, each of which require an area of 0.09mm^2. Each buffer has an input and an output, and all require connections to VCC and GND. (A) Assuming that the die uses single-level metallization and must be assembled quickly, estimate the core area of the die. (B) Estimate the total die area assuming a 110μm-wide scribe and a total of eighteen pads, each requiring 9000μm of area. (C) Draw a die floorplan for this device. Pin #9 must be GND and pin #18 must be PWR; suggest a reasonable arrangement for the eight inputs and eight outputs. Assume pad #1 must occupy the top left corner of the die and the remaining pads are arranged in counterclockwise order. (D) Each buffer requires high-current connections to VCC, GND, and its output pin. Draw a diagram of a routing pattern that will connect all eight cells without requiring any tunnels in power leads.

14.11. Calculate the width required to construct a wiring channel capable of holding twelve leads using the CMOS layout rules of Appendix C.

14.12. Suppose the output lead of a buffer carries a digital signal with a duty cycle of 50%. When the output is on, it sources 360mA of current, and when it is off it sinks negligible current. (A) If the metallization consists of 10kÅ of copper-doped aluminum capable of carrying a constant current of $5 \cdot 10^5$ A/cm^2 at 85°C, how wide

must the output lead be made in order for it to withstand electromigration? (B) How wide must the lead be made to safely cross an oxide step that may induce 30% metallization thinning? (C) How wide must the lead be made if the device will operate continuously at a junction temperature of 125°C? Assume an activation energy of 0.7eV.

14.13. The power output of an amplifier circuit conducts an average current of 3.1A under worst-case conditions. (A) Assuming the part is packaged in plastic, how many 1.2mil gold bondwires are required to safely conduct this current? (B) How many 2mil aluminum wires would be required to conduct the same current?