CHAPTER 3

METHODS OF ANALYSIS

Scientists study the world as it is, engineers create the world that never has been.

—Theodore von Karman

Enhancing Your Career

Career in Electronics One area of application for electric circuit analysis is electronics. The term *electronics* was originally used to distinguish circuits of very low current levels. This distinction no longer holds, as power semiconductor devices operate at high levels of current. Today, electronics is regarded as the science of the motion of charges in a gas, vacuum, or semiconductor. Modern electronics involves transistors and transistor circuits. The earlier electronic circuits were assembled from components. Many electronic circuits are now produced as integrated circuits, fabricated in a semiconductor substrate or chip.

Electronic circuits find applications in many areas, such as automation, broadcasting, computers, and instrumentation. The range of devices that use electronic circuits is enormous and is limited only by our imagination. Radio, television, computers, and stereo systems are but a few.

An electrical engineer usually performs diverse functions and is likely to use, design, or construct systems that incorporate some form of electronic circuits. Therefore, an understanding of the operation and analysis of electronics is essential to the electrical engineer. Electronics has become a specialty distinct from other disciplines within electrical engineering. Because the field of electronics is ever advancing, an electronics engineer must update his/her knowledge from time to time. The best way to do this is by being a member of a professional organization such as the Institute of Electrical and Electronics Engineers (IEEE). With a membership of over 300,000, the IEEE is the largest professional organization in the world. Members benefit immensely from the numerous magazines, journals, transactions, and conference/symposium proceedings published yearly by IEEE. You should consider becoming an IEEE member.

Troubleshooting an electronic circuit board. Source: T. J. Maloney, Modern Industrial Electronics, 3rd ed. Englewood Cliffs, NJ: Prentice Hall, 1996, p. 408.

3.1 INTRODUCTION

Having understood the fundamental laws of circuit theory (Ohm's law and Kirchhoff's laws), we are now prepared to apply these laws to develop two powerful techniques for circuit analysis: nodal analysis, which is based on a systematic application of Kirchhoff's current law (KCL), and mesh analysis, which is based on a systematic application of Kirchhoff's voltage law (KVL). The two techniques are so important that this chapter should be regarded as the most important in the book. Students are therefore encouraged to pay careful attention.

With the two techniques to be developed in this chapter, we can analyze almost any circuit by obtaining a set of simultaneous equations that are then solved to obtain the required values of current or voltage. One method of solving simultaneous equations involves Cramer's rule, which allows us to calculate circuit variables as a quotient of determinants. The examples in the chapter will illustrate this method; Appendix A also briefly summarizes the essentials the reader needs to know for applying Cramer's rule.

Also in this chapter, we introduce the use of *PSpice for Windows*, a circuit simulation computer software program that we will use throughout the text. Finally, we apply the techniques learned in this chapter to analyze transistor circuits.

3.2 NODAL ANALYSIS

Nodal analysis is also known as the *node-voltage method.*

Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Choosing node voltages instead of element voltages as circuit variables is convenient and reduces the number of equations one must solve simultaneously.

To simplify matters, we shall assume in this section that circuits do not contain voltage sources. Circuits that contain voltage sources will be analyzed in the next section.

In *nodal analysis*, we are interested in finding the node voltages. Given a circuit with n nodes without voltage sources, the nodal analysis of the circuit involves taking the following three steps.

Steps to Determine Node Voltages:

1. Select a node as the reference node. Assign voltages $v_1, v_2, \ldots, v_{n-1}$ to the remaining $n - 1$ nodes. The voltages are referenced with respect to the reference node.
2. Apply KCL to each of the $n - 1$ nonreference nodes. Use Ohm's law to express the branch currents in terms of node voltages.
3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

We shall now explain and apply these three steps.

The first step in nodal analysis is selecting a node as the *reference* or *datum node*. The reference node is commonly called the *ground* since it is assumed to have zero potential. A reference node is indicated by

any of the three symbols in Fig. 3.1. The type of ground in Fig. 3.1(b) is called a *chassis ground* and is used in devices where the case, enclosure, or chassis acts as a reference point for all circuits. When the potential of the earth is used as reference, we use the *earth ground* in Fig. 3.1(a) or (c). We shall always use the symbol in Fig. 3.1(b).

Once we have selected a reference node, we assign voltage designations to nonreference nodes. Consider, for example, the circuit in Fig. 3.2(a). Node 0 is the reference node ($v = 0$), while nodes 1 and 2 are assigned voltages v_1 and v_2, respectively. Keep in mind that the node voltages are defined with respect to the reference node. As illustrated in Fig. 3.2(a), each node voltage is the voltage rise from the reference node to the corresponding nonreference node or simply the voltage of that node with respect to the reference node.

As the second step, we apply KCL to each nonreference node in the circuit. To avoid putting too much information on the same circuit, the circuit in Fig. 3.2(a) is redrawn in Fig. 3.2(b), where we now add i_1, i_2, and i_3 as the currents through resistors R_1, R_2, and R_3, respectively. At node 1, applying KCL gives

$$I_1 = I_2 + i_1 + i_2 \tag{3.1}$$

At node 2,

$$I_2 + i_2 = i_3 \tag{3.2}$$

We now apply Ohm's law to express the unknown currents i_1, i_2, and i_3 in terms of node voltages. The key idea to bear in mind is that, since resistance is a passive element, by the passive sign convention, current must always flow from a higher potential to a lower potential.

Current flows from a higher potential to a lower potential in a resistor.

We can express this principle as

$$i = \frac{v_{\text{higher}} - v_{\text{lower}}}{R} \tag{3.3}$$

Note that this principle is in agreement with the way we defined resistance in Chapter 2 (see Fig. 2.1). With this in mind, we obtain from Fig. 3.2(b),

$$\begin{aligned} i_1 &= \frac{v_1 - 0}{R_1} \quad \text{or} \quad i_1 = G_1 v_1 \\ i_2 &= \frac{v_1 - v_2}{R_2} \quad \text{or} \quad i_2 = G_2(v_1 - v_2) \\ i_3 &= \frac{v_2 - 0}{R_3} \quad \text{or} \quad i_3 = G_3 v_2 \end{aligned} \tag{3.4}$$

Substituting Eq. (3.4) in Eqs. (3.1) and (3.2) results, respectively, in

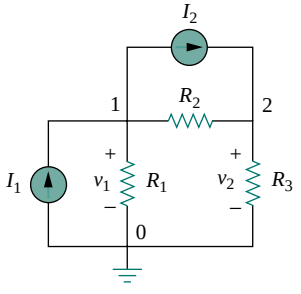
$$I_1 = I_2 + \frac{v_1}{R_1} + \frac{v_1 - v_2}{R_2} \tag{3.5}$$

$$I_2 + \frac{v_1 - v_2}{R_2} = \frac{v_2}{R_3} \tag{3.6}$$

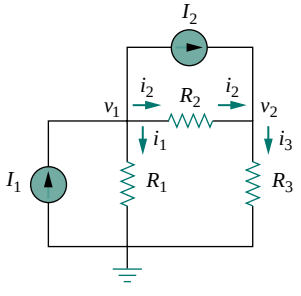
The number of nonreference nodes is equal to the number of independent equations that we will derive.

(a) (b) (c)

Figure 3.1 Common symbols for indicating a reference node.



(a)



(b)

Figure 3.2 Typical circuit for nodal analysis.

In terms of the conductances, Eqs. (3.5) and (3.6) become

$$I_1 = I_2 + G_1 v_1 + G_2(v_1 - v_2) \tag{3.7}$$

$$I_2 + G_2(v_1 - v_2) = G_3 v_2 \tag{3.8}$$

The third step in nodal analysis is to solve for the node voltages. If we apply KCL to $n-1$ nonreference nodes, we obtain $n-1$ simultaneous equations such as Eqs. (3.5) and (3.6) or (3.7) and (3.8). For the circuit of Fig. 3.2, we solve Eqs. (3.5) and (3.6) or (3.7) and (3.8) to obtain the node voltages v_1 and v_2 using any standard method, such as the substitution method, the elimination method, Cramer's rule, or matrix inversion. To use either of the last two methods, one must cast the simultaneous equations in matrix form. For example, Eqs. (3.7) and (3.8) can be cast in matrix form as

Appendix A discusses how to use Cramer's rule.

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix} \tag{3.9}$$

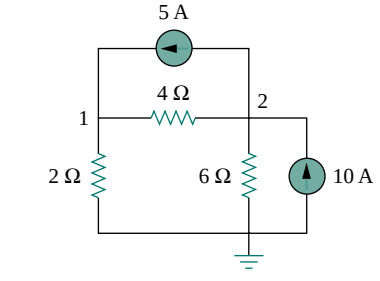
which can be solved to get v_1 and v_2. Equation 3.9 will be generalized in Section 3.6. The simultaneous equations may also be solved using calculators such as HP48 or with software packages such as *Matlab*, *Mathcad*, *Maple*, and *Quattro Pro*.

EXAMPLE 3.1

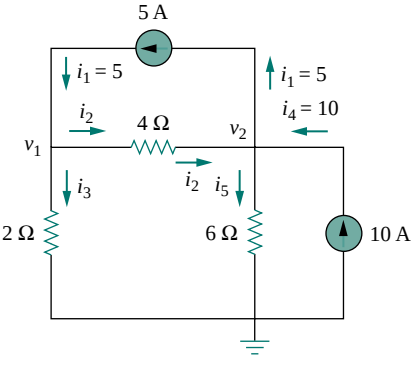
Calculate the node voltages in the circuit shown in Fig. 3.3(a).

Solution:

Consider Fig. 3.3(b), where the circuit in Fig. 3.3(a) has been prepared for nodal analysis. Notice how the currents are selected for the application of KCL. Except for the branches with current sources, the labeling of the currents is arbitrary but consistent. (By consistent, we mean that if, for example, we assume that i_2 enters the 4 Ω resistor from the left-hand side, i_2 must leave the resistor from the right-hand side.) The reference node is selected, and the node voltages v_1 and v_2 are now to be determined.



(a)



(b)

Figure 3.3 For Example 3.1: (a) original circuit, (b) circuit for analysis.

At node 1, applying KCL and Ohm's law gives

$$i_1 = i_2 + i_3 \quad \Longrightarrow \quad 5 = \frac{v_1 - v_2}{4} + \frac{v_1 - 0}{2}$$

Multiplying each term in the last equation by 4, we obtain

$$20 = v_1 - v_2 + 2v_1$$

or

$$3v_1 - v_2 = 20 \tag{3.1.1}$$

At node 2, we do the same thing and get

$$i_2 + i_4 = i_1 + i_5 \quad \Longrightarrow \quad \frac{v_1 - v_2}{4} + 10 = 5 + \frac{v_2 - 0}{6}$$

Multiplying each term by 12 results in

$$3v_1 - 3v_2 + 120 = 60 + 2v_2$$

or

$$-3v_1 + 5v_2 = 60 \tag{3.1.2}$$

Now we have two simultaneous Eqs. (3.1.1) and (3.1.2). We can solve the equations using any method and obtain the values of v_1 and v_2.

METHOD 1 Using the elimination technique, we add Eqs. (3.1.1) and (3.1.2).

$$4v_2 = 80 \quad \Longrightarrow \quad v_2 = 20 \text{ V}$$

Substituting $v_2 = 20$ in Eq. (3.1.1) gives

$$3v_1 - 20 = 20 \quad \Longrightarrow \quad v_1 = \frac{40}{3} = 13.33 \text{ V}$$

METHOD 2 To use Cramer's rule, we need to put Eqs. (3.1.1) and (3.1.2) in matrix form as

$$\begin{bmatrix} 3 & -1 \\ -3 & 5 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 20 \\ 60 \end{bmatrix} \tag{3.1.3}$$

The determinant of the matrix is

$$\Delta = \begin{vmatrix} 3 & -1 \\ -3 & 5 \end{vmatrix} = 15 - 3 = 12$$

We now obtain v_1 and v_2 as

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{\begin{vmatrix} 20 & -1 \\ 60 & 5 \end{vmatrix}}{\Delta} = \frac{100 + 60}{12} = 13.33 \text{ V}$$

$$v_2 = \frac{\Delta_2}{\Delta} = \frac{\begin{vmatrix} 3 & 20 \\ -3 & 60 \end{vmatrix}}{\Delta} = \frac{180 + 60}{12} = 20 \text{ V}$$

giving us the same result as did the elimination method.

If we need the currents, we can easily calculate them from the values of the nodal voltages.

$$i_1 = 5 \text{ A}, \qquad i_2 = \frac{v_1 - v_2}{4} = -1.6667 \text{ A}, \qquad i_3 = \frac{v_1}{2} = 6.666$$

$$i_4 = 10 \text{ A}, \qquad i_5 = \frac{v_2}{6} = 3.333 \text{ A}$$

The fact that i_2 is negative shows that the current flows in the direction opposite to the one assumed.

PRACTICE PROBLEM 3.1

Obtain the node voltages in the circuit in Fig. 3.4.

Answer: $v_1 = -2$ V, $v_2 = -14$ V.

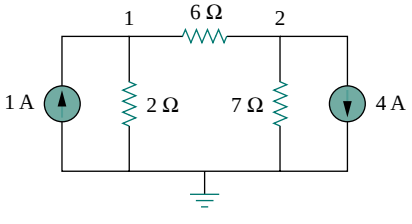


Figure 3.4 For Practice Prob. 3.1.

EXAMPLE 3.2

Determine the voltages at the nodes in Fig. 3.5(a).

Solution:

The circuit in this example has three nonreference nodes, unlike the previous example which has two nonreference nodes. We assign voltages to the three nodes as shown in Fig. 3.5(b) and label the currents.

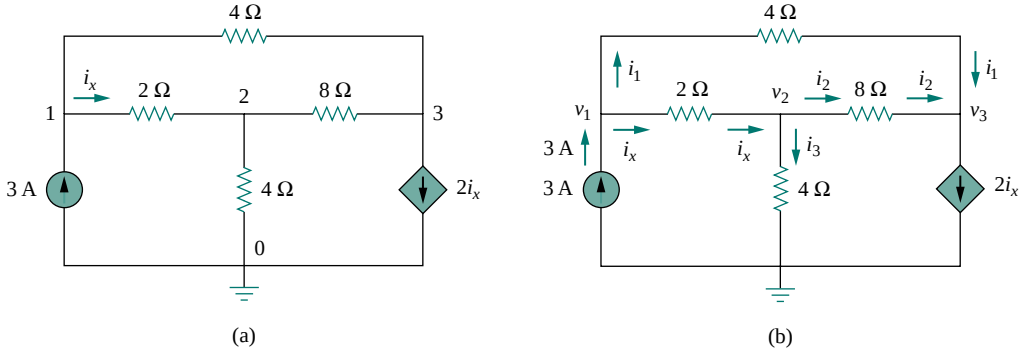


Figure 3.5 For Example 3.2: (a) original circuit, (b) circuit for analysis.

At node 1,

$$3 = i_1 + i_x \quad \Longrightarrow \quad 3 = \frac{v_1 - v_3}{4} + \frac{v_1 - v_2}{2}$$

Multiplying by 4 and rearranging terms, we get

$$3v_1 - 2v_2 - v_3 = 12 \tag{3.2.1}$$

At node 2,

$$i_x = i_2 + i_3 \quad \Longrightarrow \quad \frac{v_1 - v_2}{2} = \frac{v_2 - v_3}{8} + \frac{v_2 - 0}{4}$$

Multiplying by 8 and rearranging terms, we get

$$-4v_1 + 7v_2 - v_3 = 0 \tag{3.2.2}$$

At node 3,

$$i_1 + i_2 = 2i_x \quad \Longrightarrow \quad \frac{v_1 - v_3}{4} + \frac{v_2 - v_3}{8} = \frac{2(v_1 - v_2)}{2}$$

Multiplying by 8, rearranging terms, and dividing by 3, we get

$$2v_1 - 3v_2 + v_3 = 0 \tag{3.2.3}$$

We have three simultaneous equations to solve to get the node voltages v_1, v_2, and v_3. We shall solve the equations in two ways.

METHOD 1 Using the elimination technique, we add Eqs. (3.2.1) and (3.2.3).

$$5v_1 - 5v_2 = 12$$

or

$$v_1 - v_2 = \frac{12}{5} = 2.4 \tag{3.2.4}$$

Adding Eqs. (3.2.2) and (3.2.3) gives

$$-2v_1 + 4v_2 = 0 \quad \Longrightarrow \quad v_1 = 2v_2 \tag{3.2.5}$$

Substituting Eq. (3.2.5) into Eq. (3.2.4) yields

$$2v_2 - v_2 = 2.4 \quad \Longrightarrow \quad v_2 = 2.4, \quad v_1 = 2v_2 = 4.8 \text{ V}$$

From Eq. (3.2.3), we get

$$v_3 = 3v_2 - 2v_1 = 3v_2 - 4v_2 = -v_2 = -2.4 \text{ V}$$

Thus,

$$v_1 = 4.8 \text{ V}, \quad v_2 = 2.4 \text{ V}, \quad v_3 = -2.4 \text{ V}$$

METHOD 2 To use Cramer's rule, we put Eqs. (3.2.1) to (3.2.3) in matrix form.

$$\begin{bmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix}$$

From this, we obtain

$$v_1 = \frac{\Delta_1}{\Delta}, \quad v_2 = \frac{\Delta_2}{\Delta}, \quad v_3 = \frac{\Delta_3}{\Delta}$$

where Δ, Δ_1, Δ_2, and Δ_3 are the determinants to be calculated as follows. As explained in Appendix A, to calculate the determinant of a 3 by 3 matrix, we repeat the first two rows and cross multiply.

$$\Delta = \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{vmatrix} = \begin{array}{ccc} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \\ 3 & -2 & -1 \\ -4 & 7 & -1 \end{array} \quad \begin{array}{l} + \\ + \\ + \\ - \\ - \\ - \end{array}$$

$$= 21 - 12 + 4 + 14 - 9 - 8 = 10$$

Similarly, we obtain

$$\Delta_1 = \begin{array}{ccc} 12 & -2 & -1 \\ 0 & 7 & -1 \\ 0 & -3 & 1 \\ 12 & -2 & -1 \\ 0 & 7 & -1 \end{array} \quad \begin{array}{l} + \\ + \\ + \\ - \\ - \\ - \end{array} \quad = 84 + 0 + 0 - 0 - 36 - 0 = 48$$

$$\Delta_2 = \begin{vmatrix} 3 & 12 & -1 \\ -4 & 0 & -1 \\ 2 & 0 & 1 \end{vmatrix} = 0 + 0 - 24 - 0 - 0 + 48 = 24$$

$$\Delta_3 = \begin{vmatrix} 3 & -2 & 12 \\ -4 & 7 & 0 \\ 2 & -3 & 0 \end{vmatrix} = 0 + 144 + 0 - 168 - 0 - 0 = -24$$

Thus, we find

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{48}{10} = 4.8 \text{ V}, \qquad v_2 = \frac{\Delta_2}{\Delta} = \frac{24}{10} = 2.4 \text{ V}$$

$$v_3 = \frac{\Delta_3}{\Delta} = \frac{-24}{10} = -2.4 \text{ V}$$

as we obtained with Method 1.

PRACTICE PROBLEM 3.2

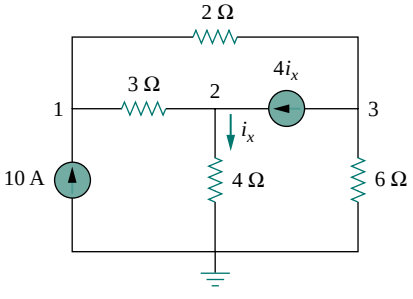


Figure 3.6 For Practice Prob. 3.2.

Find the voltages at the three nonreference nodes in the circuit of Fig. 3.6.

Answer: $v_1 = 80$ V, $v_2 = -64$ V, $v_3 = 156$ V.

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3.3 NODAL ANALYSIS WITH VOLTAGE SOURCES

We now consider how voltage sources affect nodal analysis. We use the circuit in Fig. 3.7 for illustration. Consider the following two possibilities.

CASE 1 If a voltage source is connected between the reference node and a nonreference node, we simply set the voltage at the nonreference node equal to the voltage of the voltage source. In Fig. 3.7, for example,

$$v_1 = 10 \text{ V} \tag{3.10}$$

Thus our analysis is somewhat simplified by this knowledge of the voltage at this node.

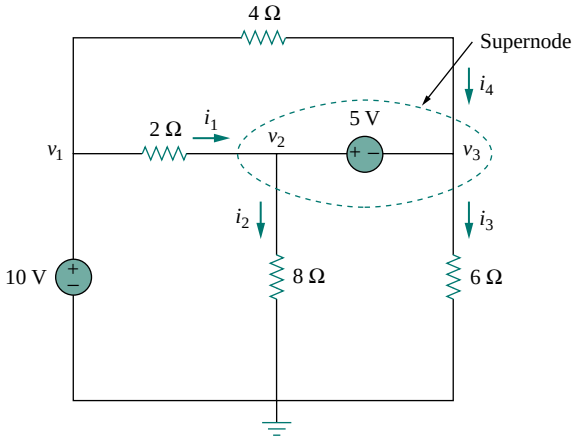


Figure 3.7 A circuit with a supernode.

CASE 2 If the voltage source (dependent or independent) is connected between two nonreference nodes, the two nonreference nodes form a *generalized node* or *supernode*; we apply both KCL and KVL to determine the node voltages.

A supernode may be regarded as a closed surface enclosing the voltage source and its two nodes.

> A supernode is formed by enclosing a (dependent or independent) voltage source connected between two nonreference nodes and any elements connected in parallel with it.

In Fig. 3.7, nodes 2 and 3 form a supernode. (We could have more than two nodes forming a single supernode. For example, see the circuit in Fig. 3.14.) We analyze a circuit with supernodes using the same three steps mentioned in the previous section except that the supernodes are treated differently. Why? Because an essential component of nodal analysis is applying KCL, which requires knowing the current through each element. There is no way of knowing the current through a voltage source in advance. However, KCL must be satisfied at a supernode like any other node. Hence, at the supernode in Fig. 3.7,

$$i_1 + i_4 = i_2 + i_3 \tag{3.11a}$$

or

$$\frac{v_1 - v_2}{2} + \frac{v_1 - v_3}{4} = \frac{v_2 - 0}{8} + \frac{v_3 - 0}{6} \tag{3.11b}$$

To apply Kirchhoff's voltage law to the supernode in Fig. 3.7, we redraw the circuit as shown in Fig. 3.8. Going around the loop in the clockwise direction gives

$$-v_2 + 5 + v_3 = 0 \quad \Longrightarrow \quad v_2 - v_3 = 5 \tag{3.12}$$

From Eqs. (3.10), (3.11b), and (3.12), we obtain the node voltages.

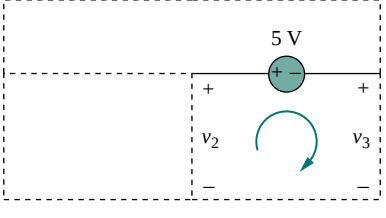


Figure 3.8 Applying KVL to a supernode.

Note the following properties of a supernode:

1. The voltage source inside the supernode provides a constraint equation needed to solve for the node voltages.
2. A supernode has no voltage of its own.
3. A supernode requires the application of both KCL and KVL.

EXAMPLE 3.3

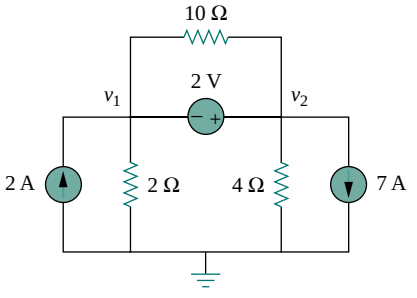


Figure 3.9 For Example 3.3.

For the circuit shown in Fig. 3.9, find the node voltages.

Solution:

The supernode contains the 2-V source, nodes 1 and 2, and the 10-Ω resistor. Applying KCL to the supernode as shown in Fig. 3.10(a) gives

$$2 = i_1 + i_2 + 7$$

Expressing i_1 and i_2 in terms of the node voltages

$$2 = \frac{v_1 - 0}{2} + \frac{v_2 - 0}{4} + 7 \qquad \Longrightarrow \qquad 8 = 2v_1 + v_2 + 28$$

or

$$v_2 = -20 - 2v_1 \tag{3.3.1}$$

To get the relationship between v_1 and v_2, we apply KVL to the circuit in Fig. 3.10(b). Going around the loop, we obtain

$$-v_1 - 2 + v_2 = 0 \qquad \Longrightarrow \qquad v_2 = v_1 + 2 \tag{3.3.2}$$

From Eqs. (3.3.1) and (3.3.2), we write

$$v_2 = v_1 + 2 = -20 - 2v_1$$

or

$$3v_1 = -22 \qquad \Longrightarrow \qquad v_1 = -7.333 \text{ V}$$

and $v_2 = v_1 + 2 = -5.333$ V. Note that the 10-Ω resistor does not make any difference because it is connected across the supernode.

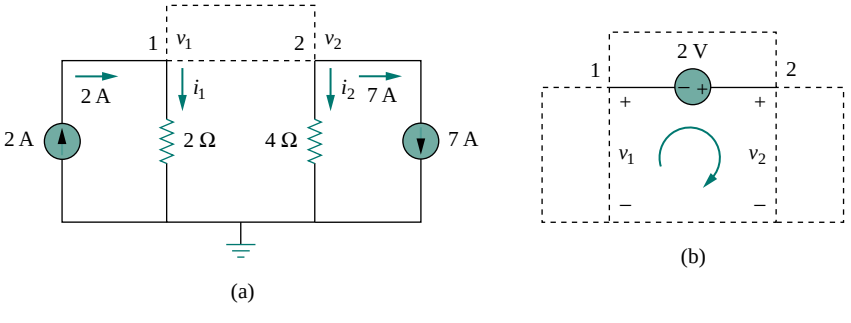


Figure 3.10 Applying: (a) KCL to the supernode, (b) KVL to the loop.

PRACTICE PROBLEM 3.3

Find v and i in the circuit in Fig. 3.11.

Answer: −0.2 V, 1.4 A.

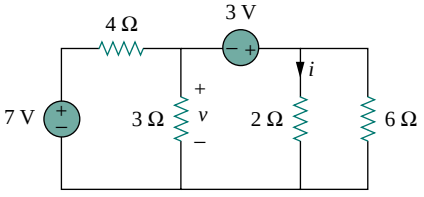


Figure 3.11 For Practice Prob. 3.3.

EXAMPLE 3.4

Find the node voltages in the circuit of Fig. 3.12.

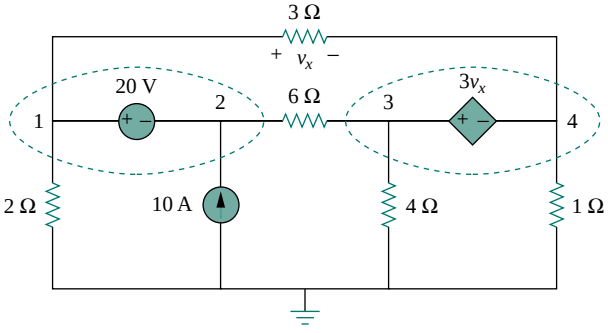


Figure 3.12 For Example 3.4.

Solution:

Nodes 1 and 2 form a supernode; so do nodes 3 and 4. We apply KCL to the two supernodes as in Fig. 3.13(a). At supernode 1-2,

$$i_3 + 10 = i_1 + i_2$$

Expressing this in terms of the node voltages,

$$\frac{v_3 - v_2}{6} + 10 = \frac{v_1 - v_4}{3} + \frac{v_1}{2}$$

or

$$5v_1 + v_2 - v_3 - 2v_4 = 60 \tag{3.4.1}$$

At supernode 3-4,

$$i_1 = i_3 + i_4 + i_5 \quad \Longrightarrow \quad \frac{v_1 - v_4}{3} = \frac{v_3 - v_2}{6} + \frac{v_4}{1} + \frac{v_3}{4}$$

or

$$4v_1 + 2v_2 - 5v_3 - 16v_4 = 0 \tag{3.4.2}$$

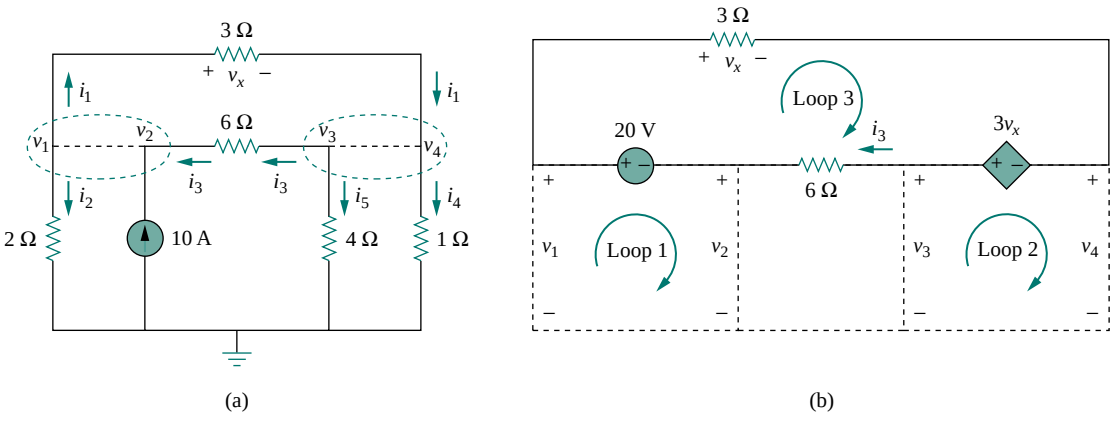


Figure 3.13 Applying: (a) KCL to the two supernodes, (b) KVL to the loops.

We now apply KVL to the branches involving the voltage sources as shown in Fig. 3.13(b). For loop 1,

$$-v_1 + 20 + v_2 = 0 \quad \Longrightarrow \quad v_1 - v_2 = 20 \tag{3.4.3}$$

For loop 2,

$$-v_3 + 3v_x + v_4 = 0$$

But $v_x = v_1 - v_4$ so that

$$3v_1 - v_3 - 2v_4 = 0 \tag{3.4.4}$$

For loop 3,

$$v_x - 3v_x + 6i_3 - 20 = 0$$

But $6i_3 = v_3 - v_2$ and $v_x = v_1 - v_4$. Hence

$$-2v_1 - v_2 + v_3 + 2v_4 = 20 \tag{3.4.5}$$

We need four node voltages, v_1, v_2, v_3, and v_4, and it requires only four out of the five Eqs. (3.4.1) to (3.4.5) to find them. Although the fifth equation is redundant, it can be used to check results. We can eliminate one node voltage so that we solve three simultaneous equations instead of four. From Eq. (3.4.3), $v_2 = v_1 - 20$. Substituting this into Eqs. (3.4.1) and (3.4.2), respectively, gives

$$6v_1 - v_3 - 2v_4 = 80 \tag{3.4.6}$$

and

$$6v_1 - 5v_3 - 16v_4 = 40 \tag{3.4.7}$$

Equations (3.4.4), (3.4.6), and (3.4.7) can be cast in matrix form as

$$\begin{bmatrix} 3 & -1 & -2 \\ 6 & -1 & -2 \\ 6 & -5 & -16 \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 80 \\ 40 \end{bmatrix}$$

Using Cramer's rule,

$$\Delta = \begin{vmatrix} 3 & -1 & -2 \\ 6 & -1 & -2 \\ 6 & -5 & -16 \end{vmatrix} = -18, \qquad \Delta_1 = \begin{vmatrix} 0 & -1 & -2 \\ 80 & -1 & -2 \\ 40 & -5 & -16 \end{vmatrix} = -480$$

$$\Delta_3 = \begin{vmatrix} 3 & 0 & -2 \\ 6 & 80 & -2 \\ 6 & 40 & -16 \end{vmatrix} = -3120, \qquad \Delta_4 = \begin{vmatrix} 3 & -1 & 0 \\ 6 & -1 & 80 \\ 6 & -5 & 40 \end{vmatrix} = 840$$

Thus, we arrive at the node voltages as

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{-480}{-18} = 26.667 \text{ V}, \qquad v_3 = \frac{\Delta_3}{\Delta} = \frac{-3120}{-18} = 173.333 \text{ V}$$

$$v_4 = \frac{\Delta_4}{\Delta} = \frac{840}{-18} = -46.667 \text{ V}$$

and $v_2 = v_1 - 20 = 6.667$ V. We have not used Eq. (3.4.5); it can be used to cross check results.

PRACTICE PROBLEM 3.4

Find v_1, v_2, and v_3 in the circuit in Fig. 3.14 using nodal analysis.

Answer: $v_1 = 3.043$ V, $v_2 = -6.956$ V, $v_3 = 0.6522$ V.

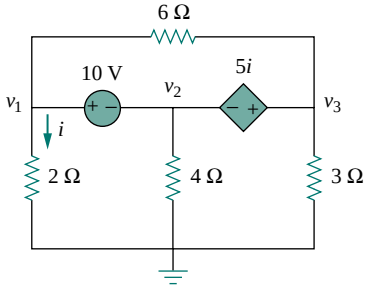


Figure 3.14 For Practice Prob. 3.4.

3.4 MESH ANALYSIS

Mesh analysis provides another general procedure for analyzing circuits, using mesh currents as the circuit variables. Using mesh currents instead of element currents as circuit variables is convenient and reduces the number of equations that must be solved simultaneously. Recall that a loop is a closed path with no node passed more than once. A mesh is a loop that does not contain any other loop within it.

Nodal analysis applies KCL to find unknown voltages in a given circuit, while mesh analysis applies KVL to find unknown currents. Mesh analysis is not quite as general as nodal analysis because it is only applicable to a circuit that is *planar*. A planar circuit is one that can be drawn in a plane with no branches crossing one another; otherwise it is *nonplanar*. A circuit may have crossing branches and still be planar if it can be redrawn such that it has no crossing branches. For example, the

Mesh analysis is also known as *loop analysis* or the *mesh-current method.*

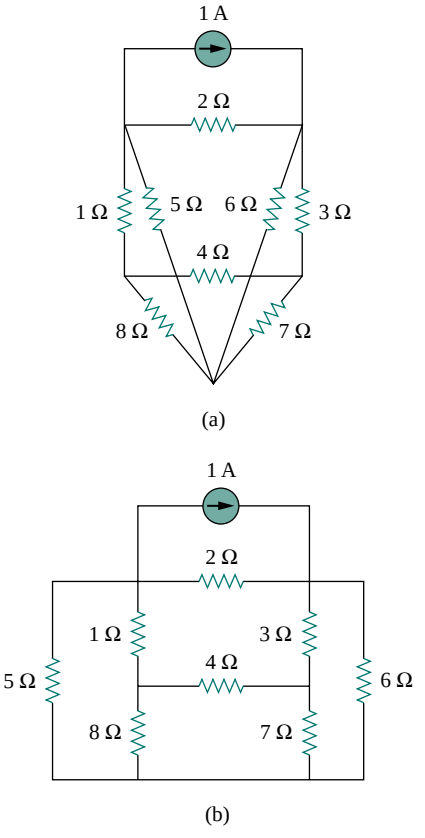


Figure 3.15 (a) A planar circuit with crossing branches, (b) the same circuit redrawn with no crossing branches.

circuit in Fig. 3.15(a) has two crossing branches, but it can be redrawn as in Fig. 3.15(b). Hence, the circuit in Fig. 3.15(a) is planar. However, the circuit in Fig. 3.16 is nonplanar, because there is no way to redraw it and avoid the branches crossing. Nonplanar circuits can be handled using nodal analysis, but they will not be considered in this text.

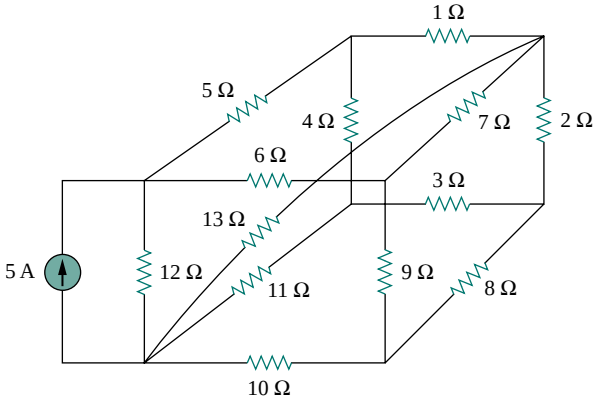


Figure 3.16 A nonplanar circuit.

To understand mesh analysis, we should first explain more about what we mean by a mesh.

A mesh is a loop which does not contain any other loops within it.

In Fig. 3.17, for example, paths *abefa* and *bcdeb* are meshes, but path *abcdefa* is not a mesh. The current through a mesh is known as *mesh current*. In mesh analysis, we are interested in applying KVL to find the mesh currents in a given circuit.

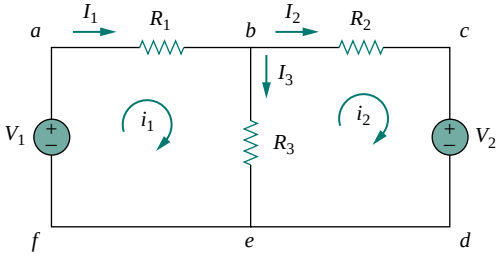


Figure 3.17 A circuit with two meshes.

In this section, we will apply mesh analysis to planar circuits that do not contain current sources. In the next sections, we will consider circuits with current sources. In the mesh analysis of a circuit with n meshes, we take the following three steps.

Although path *abcdefa* is a loop and not a mesh, KVL still holds. This is the reason for loosely using the terms *loop analysis* and *mesh analysis* to mean the same thing.

Steps to Determine Mesh Currents:

1. Assign mesh currents $i_1, i_2, \ldots, i_n$ to the n meshes.
2. Apply KVL to each of the n meshes. Use Ohm's law to express the voltages in terms of the mesh currents.
3. Solve the resulting n simultaneous equations to get the mesh currents.

To illustrate the steps, consider the circuit in Fig. 3.17. The first step requires that mesh currents i_1 and i_2 are assigned to meshes 1 and 2. Although a mesh current may be assigned to each mesh in an arbitrary direction, it is conventional to assume that each mesh current flows clockwise.

The direction of the mesh current is arbitrary—(clockwise or counterclockwise)—and does not affect the validity of the solution.

As the second step, we apply KVL to each mesh. Applying KVL to mesh 1, we obtain

$$-V_1 + R_1 i_1 + R_3(i_1 - i_2) = 0$$

or

$$(R_1 + R_3)i_1 - R_3 i_2 = V_1 \tag{3.13}$$

For mesh 2, applying KVL gives

$$R_2 i_2 + V_2 + R_3(i_2 - i_1) = 0$$

or

$$-R_3 i_1 + (R_2 + R_3)i_2 = -V_2 \tag{3.14}$$

Note in Eq. (3.13) that the coefficient of i_1 is the sum of the resistances in the first mesh, while the coefficient of i_2 is the negative of the resistance common to meshes 1 and 2. Now observe that the same is true in Eq. (3.14). This can serve as a shortcut way of writing the mesh equations. We will exploit this idea in Section 3.6.

The shortcut way will not apply if one mesh current is assumed clockwise and the other assumed anticlockwise, although this is permissible.

The third step is to solve for the mesh currents. Putting Eqs. (3.13) and (3.14) in matrix form yields

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \end{bmatrix} \tag{3.15}$$

which can be solved to obtain the mesh currents i_1 and i_2. We are at liberty to use any technique for solving the simultaneous equations. According to Eq. (2.12), if a circuit has n nodes, b branches, and l independent loops or meshes, then $l = b - n + 1$. Hence, l independent simultaneous equations are required to solve the circuit using mesh analysis.

Notice that the branch currents are different from the mesh currents unless the mesh is isolated. To distinguish between the two types of currents, we use i for a mesh current and I for a branch current. The current elements I_1, I_2, and I_3 are algebraic sums of the mesh currents. It is evident from Fig. 3.17 that

$$I_1 = i_1, \qquad I_2 = i_2, \qquad I_3 = i_1 - i_2 \tag{3.16}$$

EXAMPLE 3.5

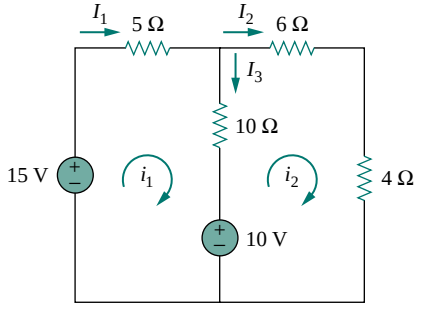


Figure 3.18 For Example 3.5.

For the circuit in Fig. 3.18, find the branch currents I_1, I_2, and I_3 using mesh analysis.

Solution:

We first obtain the mesh currents using KVL. For mesh 1,

$$-15 + 5i_1 + 10(i_1 - i_2) + 10 = 0$$

or

$$3i_1 - 2i_2 = 1 \tag{3.5.1}$$

For mesh 2,

$$6i_2 + 4i_2 + 10(i_2 - i_1) - 10 = 0$$

or

$$i_1 = 2i_2 - 1 \tag{3.5.2}$$

METHOD 1 Using the substitution method, we substitute Eq. (3.5.2) into Eq. (3.5.1), and write

$$6i_2 - 3 - 2i_2 = 1 \qquad \Longrightarrow \qquad i_2 = 1 \text{ A}$$

From Eq. (3.5.2), $i_1 = 2i_2 - 1 = 2 - 1 = 1$ A. Thus,

$$I_1 = i_1 = 1 \text{ A}, \qquad I_2 = i_2 = 1 \text{ A}, \qquad I_3 = i_1 - i_2 = 0$$

METHOD 2 To use Cramer's rule, we cast Eqs. (3.5.1) and (3.5.2) in matrix form as

$$\begin{bmatrix} 3 & -2 \\ -1 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}$$

We obtain the determinants

$$\Delta = \begin{vmatrix} 3 & -2 \\ -1 & 2 \end{vmatrix} = 6 - 2 = 4$$

$$\Delta_1 = \begin{vmatrix} 1 & -2 \\ 1 & 2 \end{vmatrix} = 2 + 2 = 4, \qquad \Delta_2 = \begin{vmatrix} 3 & 1 \\ -1 & 1 \end{vmatrix} = 3 + 1 = 4$$

Thus,

$$i_1 = \frac{\Delta_1}{\Delta} = 1 \text{ A}, \qquad i_2 = \frac{\Delta_2}{\Delta} = 1 \text{ A}$$

as before.

PRACTICE PROBLEM 3.5

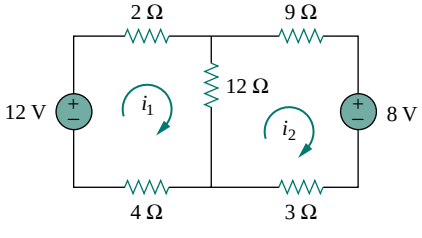


Figure 3.19 For Practice Prob. 3.5.

Calculate the mesh currents i_1 and i_2 in the circuit of Fig. 3.19.

Answer: $i_1 = \frac{2}{3}$ A, $i_2 = 0$ A.

EXAMPLE 3.6

Use mesh analysis to find the current i_o in the circuit in Fig. 3.20.

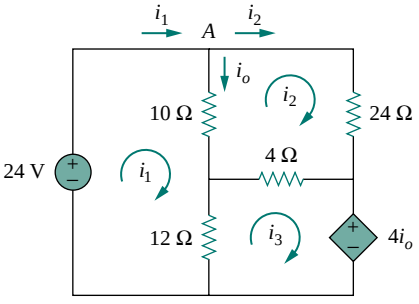


Figure 3.20 For Example 3.6.

Solution:

We apply KVL to the three meshes in turn. For mesh 1,

$$-24 + 10(i_1 - i_2) + 12(i_1 - i_3) = 0$$

or

$$11i_1 - 5i_2 - 6i_3 = 12 \tag{3.6.1}$$

For mesh 2,

$$24i_2 + 4(i_2 - i_3) + 10(i_2 - i_1) = 0$$

or

$$-5i_1 + 19i_2 - 2i_3 = 0 \tag{3.6.2}$$

For mesh 3,

$$4i_o + 12(i_3 - i_1) + 4(i_3 - i_2) = 0$$

But at node A, $i_o = i_1 - i_2$, so that

$$4(i_1 - i_2) + 12(i_3 - i_1) + 4(i_3 - i_2) = 0$$

or

$$-i_1 - i_2 + 2i_3 = 0 \tag{3.6.3}$$

In matrix form, Eqs. (3.6.1) to (3.6.3) become

$$\begin{bmatrix} 11 & -5 & -6 \\ -5 & 19 & -2 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix}$$

We obtain the determinants as

$$\Delta = \begin{vmatrix} 11 & -5 & -6 \\ -5 & 19 & -2 \\ -1 & -1 & 2 \end{vmatrix} \begin{matrix} 11 & -5 \\ -5 & 19 \\ -1 & -1 \end{matrix}$$

$$= 418 - 30 - 10 - 114 - 22 - 50 = 192$$

$$\Delta_1 = \begin{vmatrix} 12 & -5 & -6 \\ 0 & 19 & -2 \\ 0 & -1 & 2 \end{vmatrix} \begin{matrix} 12 & -5 \\ 0 & 19 \\ 0 & -1 \end{matrix} = 456 - 24 = 432$$

$$\Delta_2 = \begin{vmatrix} 11 & 12 & -6 \\ -5 & 0 & -2 \\ -1 & 0 & 2 \end{vmatrix} \begin{matrix} 11 & 12 \\ -5 & 0 \\ -1 & 0 \end{matrix} = 24 + 120 = 144$$

$$\Delta_3 = \begin{vmatrix} 11 & -5 & 12 \\ -5 & 19 & 0 \\ -1 & -1 & 0 \end{vmatrix} \begin{matrix} \\ - \\ - \\ - \end{matrix} \begin{matrix} \\ \\ + \\ + \\ + \end{matrix} = 60 + 228 = 288$$

We calculate the mesh currents using Cramer's rule as

$$i_1 = \frac{\Delta_1}{\Delta} = \frac{432}{192} = 2.25 \text{ A}, \qquad i_2 = \frac{\Delta_2}{\Delta} = \frac{144}{192} = 0.75 \text{ A}$$

$$i_3 = \frac{\Delta_3}{\Delta} = \frac{288}{192} = 1.5 \text{ A}$$

Thus, $i_o = i_1 - i_2 = 1.5$ A.

PRACTICE PROBLEM 3.6

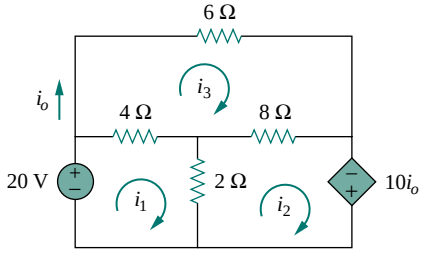


Figure 3.21 For Practice Prob. 3.6.

Using mesh analysis, find i_o in the circuit in Fig. 3.21.

Answer: -5 A.

Electronic Testing Tutorials

3.5 MESH ANALYSIS WITH CURRENT SOURCES

Applying mesh analysis to circuits containing current sources (dependent or independent) may appear complicated. But it is actually much easier than what we encountered in the previous section, because the presence of the current sources reduces the number of equations. Consider the following two possible cases.

CASE 1 When a current source exists only in one mesh: Consider the circuit in Fig. 3.22, for example. We set $i_2 = -5$ A and write a mesh equation for the other mesh in the usual way, that is,

$$-10 + 4i_1 + 6(i_1 - i_2) = 0 \quad \Longrightarrow \quad i_1 = -2 \text{ A} \tag{3.17}$$

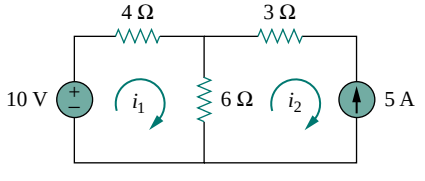


Figure 3.22 A circuit with a current source.

CASE 2 When a current source exists between two meshes: Consider the circuit in Fig. 3.23(a), for example. We create a *supermesh* by excluding the current source and any elements connected in series with it, as shown in Fig. 3.23(b). Thus,

A supermesh results when two meshes have a (dependent or independent) current source in common.

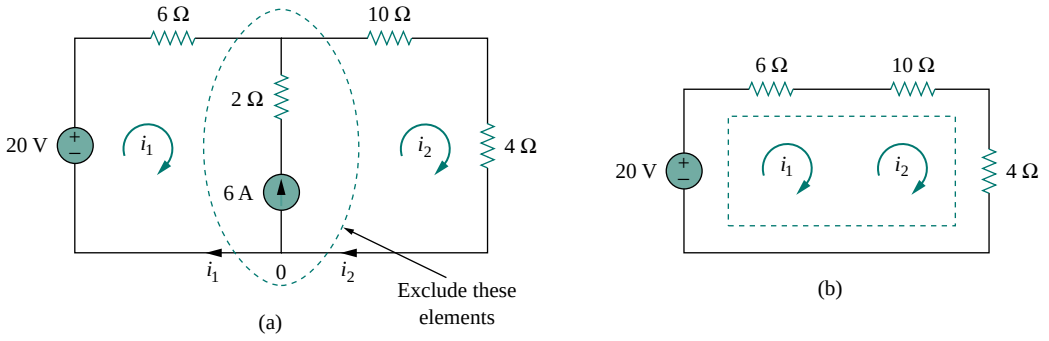


Figure 3.23 (a) Two meshes having a current source in common, (b) a supermesh, created by excluding the current source.

As shown in Fig. 3.23(b), we create a supermesh as the periphery of the two meshes and treat it differently. (If a circuit has two or more supermeshes that intersect, they should be combined to form a larger supermesh.) Why treat the supermesh differently? Because mesh analysis applies KVL—which requires that we know the voltage across each branch—and we do not know the voltage across a current source in advance. However, a supermesh must satisfy KVL like any other mesh. Therefore, applying KVL to the supermesh in Fig. 3.23(b) gives

$$-20 + 6i_1 + 10i_2 + 4i_2 = 0$$

or

$$6i_1 + 14i_2 = 20 \tag{3.18}$$

We apply KCL to a node in the branch where the two meshes intersect. Applying KCL to node 0 in Fig. 3.23(a) gives

$$i_2 = i_1 + 6 \tag{3.19}$$

Solving Eqs. (3.18) and (3.19), we get

$$i_1 = -3.2 \text{ A}, \qquad i_2 = 2.8 \text{ A} \tag{3.20}$$

Note the following properties of a supermesh:

1. The current source in the supermesh is not completely ignored; it provides the constraint equation necessary to solve for the mesh currents.
2. A supermesh has no current of its own.
3. A supermesh requires the application of both KVL and KCL.

EXAMPLE 3.7

For the circuit in Fig. 3.24, find i_1 to i_4 using mesh analysis.

Solution:

Note that meshes 1 and 2 form a supermesh since they have an independent current source in common. Also, meshes 2 and 3 form another supermesh

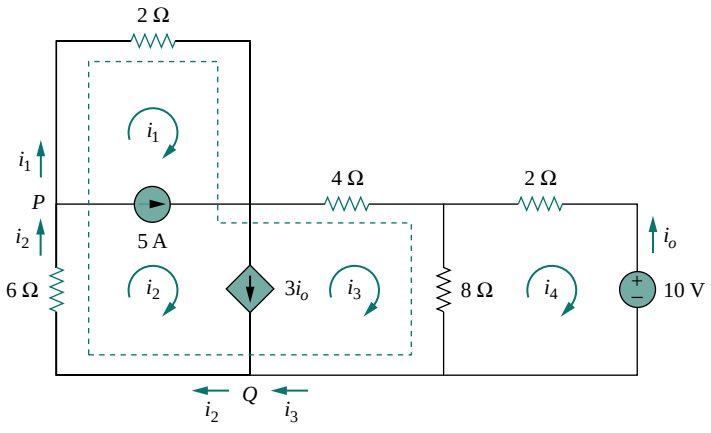


Figure 3.24 For Example 3.7.

because they have a dependent current source in common. The two supermeshes intersect and form a larger supermesh as shown. Applying KVL to the larger supermesh,

$$2i_1 + 4i_3 + 8(i_3 - i_4) + 6i_2 = 0$$

or

$$i_1 + 3i_2 + 6i_3 - 4i_4 = 0 \tag{3.7.1}$$

For the independent current source, we apply KCL to node P:

$$i_2 = i_1 + 5 \tag{3.7.2}$$

For the dependent current source, we apply KCL to node Q:

$$i_2 = i_3 + 3i_o$$

But $i_o = -i_4$, hence,

$$i_2 = i_3 - 3i_4 \tag{3.7.3}$$

Applying KVL in mesh 4,

$$2i_4 + 8(i_4 - i_3) + 10 = 0$$

or

$$5i_4 - 4i_3 = -5 \tag{3.7.4}$$

From Eqs. (3.7.1) to (3.7.4),

$$i_1 = -7.5 \text{ A}, \quad i_2 = -2.5 \text{ A}, \quad i_3 = 3.93 \text{ A}, \quad i_4 = 2.143 \text{ A}$$

PRACTICE PROBLEM 3.7

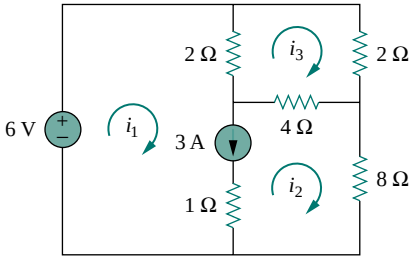


Figure 3.25 For Practice Prob. 3.7.

Use mesh analysis to determine i_1, i_2, and i_3 in Fig. 3.25.

Answer: $i_1 = 3.474$ A, $i_2 = 0.4737$ A, $i_3 = 1.1052$ A.

†3.6 NODAL AND MESH ANALYSES BY INSPECTION

This section presents a generalized procedure for nodal or mesh analysis. It is a shortcut approach based on mere inspection of a circuit.

When all sources in a circuit are independent current sources, we do not need to apply KCL to each node to obtain the node-voltage equations as we did in Section 3.2. We can obtain the equations by mere inspection of the circuit. As an example, let us reexamine the circuit in Fig. 3.2, shown again in Fig. 3.26(a) for convenience. The circuit has two nonreference nodes and the node equations were derived in Section 3.2 as

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix} \tag{3.21}$$

Observe that each of the diagonal terms is the sum of the conductances connected directly to node 1 or 2, while the off-diagonal terms are the negatives of the conductances connected between the nodes. Also, each term on the right-hand side of Eq. (3.21) is the algebraic sum of the currents entering the node.

In general, if a circuit with independent current sources has N nonreference nodes, the node-voltage equations can be written in terms of the conductances as

$$\begin{bmatrix} G_{11} & G_{12} & \cdots & G_{1N} \\ G_{21} & G_{22} & \cdots & G_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ G_{N1} & G_{N2} & \cdots & G_{NN} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} \tag{3.22}$$

or simply

$$\mathbf{Gv} = \mathbf{i} \tag{3.23}$$

where

G_{kk} = Sum of the conductances connected to node k

$G_{kj} = G_{jk}$ = Negative of the sum of the conductances directly connecting nodes k and j, $k \neq j$

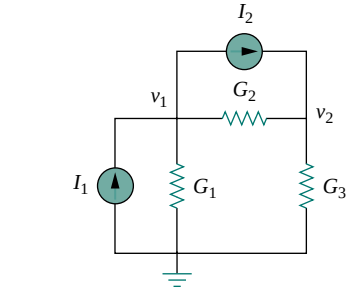
v_k = Unknown voltage at node k

i_k = Sum of all independent current sources directly connected to node k, with currents entering the node treated as positive

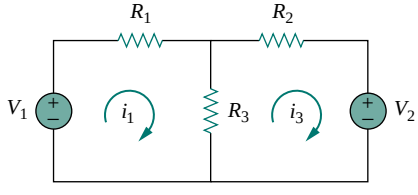
G is called the *conductance matrix*, **v** is the output vector; and **i** is the input vector. Equation (3.22) can be solved to obtain the unknown node voltages. Keep in mind that this is valid for circuits with only independent current sources and linear resistors.

Similarly, we can obtain mesh-current equations by inspection when a linear resistive circuit has only independent voltage sources. Consider the circuit in Fig. 3.17, shown again in Fig. 3.26(b) for convenience. The circuit has two nonreference nodes and the node equations were derived in Section 3.4 as

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} v_1 \\ -v_2 \end{bmatrix} \tag{3.24}$$



(a)



(b)

Figure 3.26 (a) The circuit in Fig. 3.2, (b) the circuit in Fig. 3.17.

We notice that each of the diagonal terms is the sum of the resistances in the related mesh, while each of the off-diagonal terms is the negative of the resistance common to meshes 1 and 2. Each term on the right-hand side of Eq. (3.24) is the algebraic sum taken clockwise of all independent voltage sources in the related mesh.

In general, if the circuit has N meshes, the mesh-current equations can be expressed in terms of the resistances as

$$\begin{bmatrix} R_{11} & R_{12} & \dots & R_{1N} \\ R_{21} & R_{22} & \dots & R_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ R_{N1} & R_{N2} & \dots & R_{NN} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} \tag{3.25}$$

or simply

$$\mathbf{Ri} = \mathbf{v} \tag{3.26}$$

where

R_{kk} = Sum of the resistances in mesh k

$R_{kj} = R_{jk}$ = Negative of the sum of the resistances in common with meshes k and j, $k \neq j$

i_k = Unknown mesh current for mesh k in the clockwise direction

v_k = Sum taken clockwise of all independent voltage sources in mesh k, with voltage rise treated as positive

R is called the *resistance matrix*, **i** is the output vector; and **v** is the input vector. We can solve Eq. (3.25) to obtain the unknown mesh currents.

EXAMPLE 3.8

Write the node-voltage matrix equations for the circuit in Fig. 3.27 by inspection.

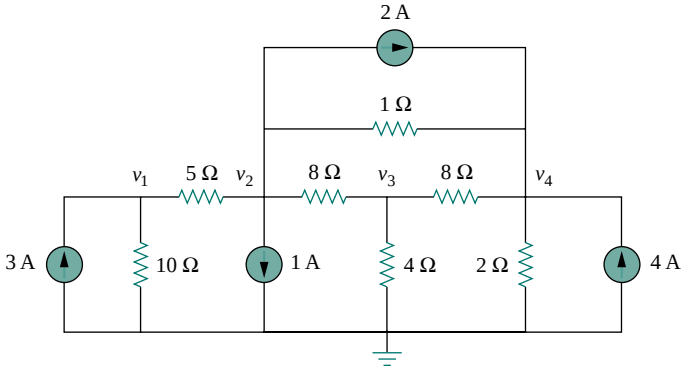


Figure 3.27 For Example 3.8.

Solution:

The circuit in Fig. 3.27 has four nonreference nodes, so we need four node equations. This implies that the size of the conductance matrix **G**, is 4 by 4. The diagonal terms of **G**, in siemens, are

$$G_{11} = \frac{1}{5} + \frac{1}{10} = 0.3, \qquad G_{22} = \frac{1}{5} + \frac{1}{8} + \frac{1}{1} = 1.325$$

$$G_{33} = \frac{1}{8} + \frac{1}{8} + \frac{1}{4} = 0.5, \qquad G_{44} = \frac{1}{8} + \frac{1}{2} + \frac{1}{1} = 1.625$$

The off-diagonal terms are

$$G_{12} = -\frac{1}{5} = -0.2, \qquad G_{13} = G_{14} = 0$$

$$G_{21} = -0.2, \qquad G_{23} = -\frac{1}{8} = -0.125, \qquad G_{24} = -\frac{1}{1} = -1$$

$$G_{31} = 0, \qquad G_{32} = -0.125, \qquad G_{34} = -\frac{1}{8} = -0.125$$

$$G_{41} = 0, \qquad G_{42} = -1, \qquad G_{43} = -0.125$$

The input current vector **i** has the following terms, in amperes:

$$i_1 = 3, \qquad i_2 = -1 - 2 = -3, \qquad i_3 = 0, \qquad i_4 = 2 + 4 = 6$$

Thus the node-voltage equations are

$$\begin{bmatrix} 0.3 & -0.2 & 0 & 0 \\ -0.2 & 1.325 & -0.125 & -1 \\ 0 & -0.125 & 0.5 & -0.125 \\ 0 & -1 & -0.125 & 1.625 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 3 \\ -3 \\ 0 \\ 6 \end{bmatrix}$$

which can be solved to obtain the node voltages v_1, v_2, v_3, and v_4.

PRACTICE PROBLEM 3.8

By inspection, obtain the node-voltage equations for the circuit in Fig. 3.28.

Answer:

$$\begin{bmatrix} 1.3 & -0.2 & -1 & 0 \\ -0.2 & 0.2 & 0 & 0 \\ -1 & 0 & 1.25 & -0.25 \\ 0 & 0 & -0.25 & 0.75 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 3 \\ -1 \\ 3 \end{bmatrix}$$

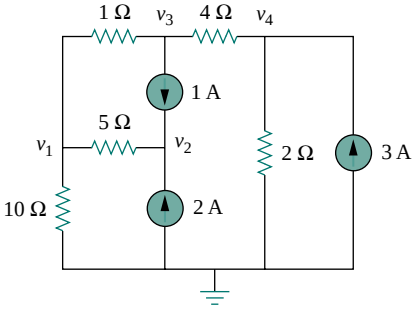


Figure 3.28 For Practice Prob. 3.8.

EXAMPLE 3.9

By inspection, write the mesh-current equations for the circuit in Fig. 3.29.

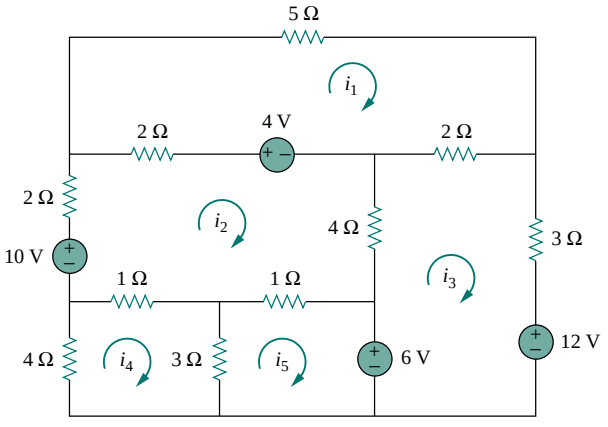


Figure 3.29 For Example 3.9.

Solution:

We have five meshes, so the resistance matrix is 5 by 5. The diagonal terms, in ohms, are:

$$R_{11} = 5 + 2 + 2 = 9, \qquad R_{22} = 2 + 4 + 1 + 1 + 2 = 10$$
$$R_{33} = 2 + 3 + 4 = 9, \qquad R_{44} = 1 + 3 + 4 = 8, \qquad R_{55} = 1 + 3 = 4$$

The off-diagonal terms are:

$$R_{12} = -2, \qquad R_{13} = -2, \qquad R_{14} = 0 = R_{15}$$
$$R_{21} = -2, \qquad R_{23} = -4, \qquad R_{24} = -1, \qquad R_{25} = -1$$
$$R_{31} = -2, \qquad R_{32} = -4, \qquad R_{34} = 0 = R_{35}$$
$$R_{41} = 0, \qquad R_{42} = -1, \qquad R_{43} = 0, \qquad R_{45} = -3$$
$$R_{51} = 0, \qquad R_{52} = -1, \qquad R_{53} = 0, \qquad R_{54} = -3$$

The input voltage vector **v** has the following terms in volts:

$$v_1 = 4, \qquad v_2 = 10 - 4 = 6$$
$$v_3 = -12 + 6 = -6, \qquad v_4 = 0, \qquad v_5 = -6$$

Thus the mesh-current equations are:

$$\begin{bmatrix} 9 & -2 & -2 & 0 & 0 \\ -2 & 10 & -4 & -1 & -1 \\ -2 & -4 & 9 & 0 & 0 \\ 0 & -1 & 0 & 8 & -3 \\ 0 & -1 & 0 & -3 & 4 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 4 \\ 6 \\ -6 \\ 0 \\ -6 \end{bmatrix}$$

From this, we can obtain mesh currents i_1, i_2, i_3, i_4, and i_5.

PRACTICE PROBLEM 3.9

By inspection, obtain the mesh-current equations for the circuit in Fig. 3.30.

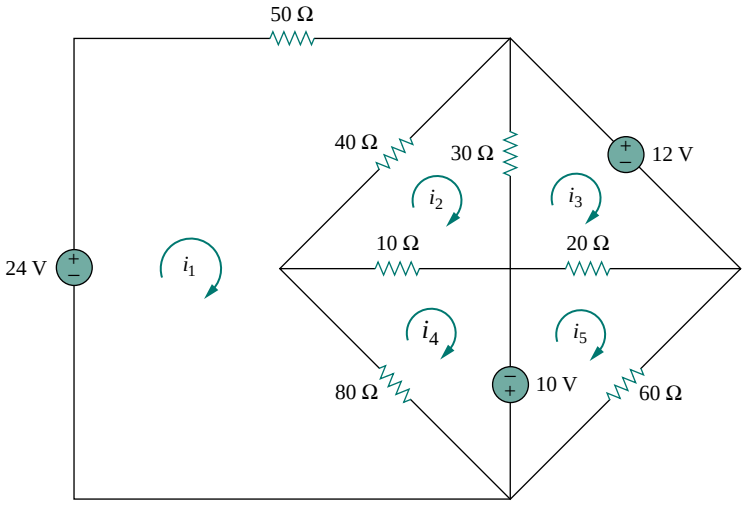


Figure 3.30 For Practice Prob. 3.9.

Answer:

$$\begin{bmatrix} 170 & -40 & 0 & -80 & 0 \\ -40 & 80 & -30 & -10 & 0 \\ 0 & -30 & 50 & 0 & -20 \\ -80 & -10 & 0 & 90 & 0 \\ 0 & 0 & -20 & 0 & 80 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 24 \\ 0 \\ -12 \\ 10 \\ -10 \end{bmatrix}$$

3.7 NODAL VERSUS MESH ANALYSIS

Both nodal and mesh analyses provide a systematic way of analyzing a complex network. Someone may ask: Given a network to be analyzed, how do we know which method is better or more efficient? The choice of the better method is dictated by two factors.

The first factor is the nature the particular network. Networks that contain many series-connected elements, voltage sources, or supermeshes are more suitable for mesh analysis, whereas networks with parallel-connected elements, current sources, or supernodes are more suitable for nodal analysis. Also, a circuit with fewer nodes than meshes is better analyzed using nodal analysis, while a circuit with fewer meshes than nodes is better analyzed using mesh analysis. The key is to select the method that results in the smaller number of equations.

The second factor is the information required. If node voltages are required, it may be expedient to apply nodal analysis. If branch or mesh currents are required, it may be better to use mesh analysis.

It is helpful to be familiar with both methods of analysis, for at least two reasons. First, one method can be used to check the results from the other method, if possible. Second, since each method has its limitations, only one method may be suitable for a particular problem. For example,

mesh analysis is the only method to use in analyzing transistor circuits, as we shall see in Section 3.9. But mesh analysis cannot easily be used to solve an op amp circuit, as we shall see in Chapter 5, because there is no direct way to obtain the voltage across the op amp itself. For nonplanar networks, nodal analysis is the only option, because mesh analysis only applies to planar networks. Also, nodal analysis is more amenable to solution by computer, as it is easy to program. This allows one to analyze complicated circuits that defy hand calculation. A computer software package based on nodal analysis is introduced next.

3.8 CIRCUIT ANALYSIS WITH *PSPICE*

Appendix D provides a tutorial on using PSpice for Windows.

PSpice is a computer software circuit analysis program that we will gradually learn to use throught the course of this text. This section illustrates how to use *PSpice for Windows* to analyze the dc circuits we have studied so far.

The reader is expected to review Sections D.1 through D.3 of Appendix D before proceeding in this section. It should be noted that *PSpice* is only helpful in determining branch voltages and currents when the numerical values of all the circuit components are known.

EXAMPLE 3.10

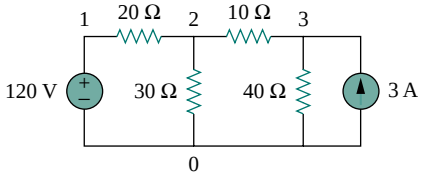


Figure 3.31 For Example 3.10.

Use *PSpice* to find the node voltages in the circuit of Fig. 3.31.

Solution:

The first step is to draw the given circuit using Schematics. If one follows the instructions given in Appendix sections D.2 and D.3, the schematic in Fig. 3.32 is produced. Since this is a dc analysis, we use voltage source VDC and current source IDC. The pseudocomponent VIEWPOINTS are added to display the required node voltages. Once the circuit is drawn and saved as exam310.sch, we run *PSpice* by selecting **Analysis/Simulate**. The circuit is simulated and the results are displayed on VIEWPOINTS and also saved in output file exam310.out. The output file includes the following:

```
NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE
(1)    120.0000   (2)    81.2900    (3)    89.0320
```

indicating that $V_1 = 120$ V, $V_2 = 81.29$ V, $V_3 = 89.032$ V.

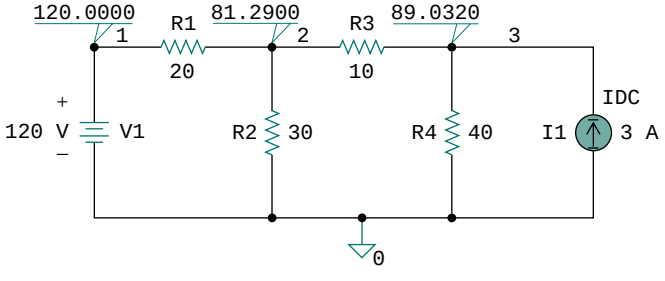


Figure 3.32 For Example 3.10; the schematic of the circuit in Fig. 3.31.

PRACTICE PROBLEM 3.10

For the circuit in Fig. 3.33, use *PSpice* to find the node voltages.

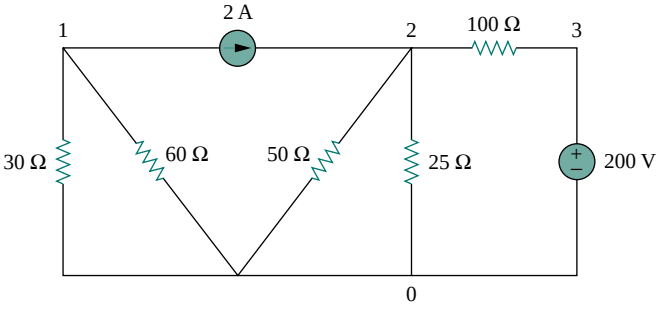


Figure 3.33 For Practice Prob. 3.10.

Answer: $V_1 = -40$ V, $V_2 = 57.14$ V, $V_3 = 200$ V.

EXAMPLE 3.11

In the circuit in Fig. 3.34, determine the currents i_1, i_2, and i_3.

Solution:

The schematic is shown in Fig. 3.35. (The schematic in Fig. 3.35 includes the output results, implying that it is the schematic displayed on the screen *after* the simulation.) Notice that the voltage-controlled voltage source E1 in Fig. 3.35 is connected so that its input is the voltage across the 4-Ω resistor; its gain is set equal to 3. In order to display the required currents, we insert pseudocomponent IPROBES in the appropriate branches. The schematic is saved as exam311.sch and simulated by selecting **Analysis/Simulate**. The results are displayed on IPROBES as shown in Fig. 3.35 and saved in output file exam311.out. From the output file or the IPROBES, we obtain $i_1 = i_2 = 1.333$ A and $i_3 = 2.667$ A.

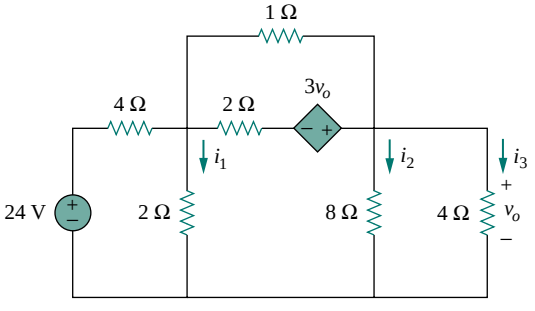


Figure 3.34 For Example 3.11.

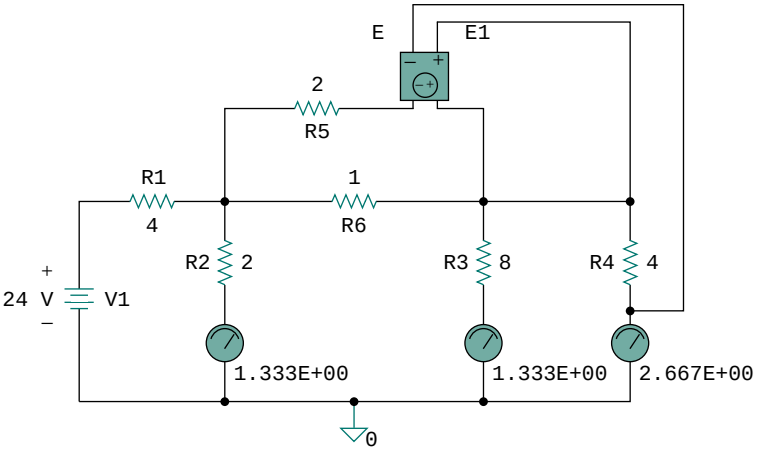


Figure 3.35 The schematic of the circuit in Fig. 3.34.

PRACTICE PROBLEM 3.11

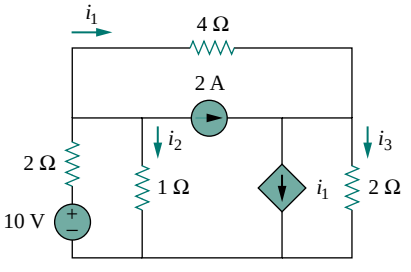


Figure 3.36 For Practice Prob. 3.11.

Use *PSpice* to determine currents i_1, i_2, and i_3 in the circuit of Fig. 3.36.

Answer: $i_1 = -0.4286$ A, $i_2 = 2.286$ A, $i_3 = 2$ A.

†3.9 APPLICATIONS: DC TRANSISTOR CIRCUITS

Most of us deal with electronic products on a routine basis and have some experience with personal computers. A basic component for the integrated circuits found in these electronics and computers is the active, three-terminal device known as the *transistor.* Understanding the transistor is essential before an engineer can start an electronic circuit design.

Figure 3.37 depicts various kinds of transistors commercially available. There are two basic types of transistors: *bipolar junction transistors* (BJTs) and *field-effect transistors* (FETs). Here, we consider only the BJTs, which were the first of the two and are still used today. Our objective is to present enough detail about the BJT to enable us to apply the techniques developed in this chapter to analyze dc transistor circuits.

There are two types of BJTs: *npn* and *pnp*, with their circuit symbols as shown in Fig. 3.38. Each type has three terminals, designated as emitter (E), base (B), and collector (C). For the *npn* transistor, the currents and

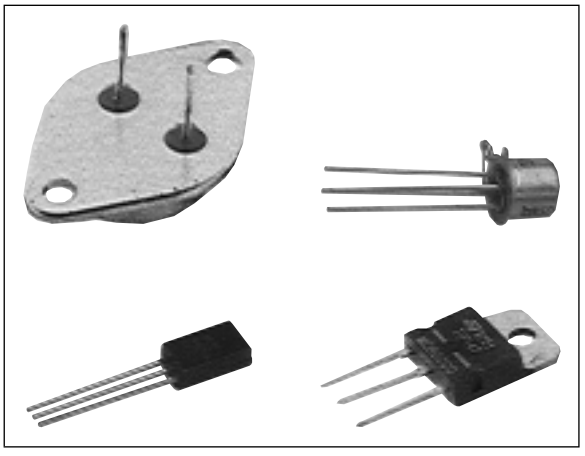


Figure 3.37 Various types of transistors. *(Courtesy of Tech America.)*

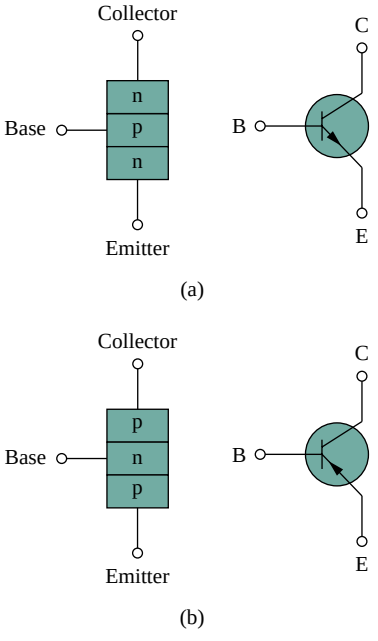


Figure 3.38 Two types of BJTs and their circuit symbols: (a) *npn*, (b) *pnp*.

voltages of the transistor are specified as in Fig. 3.39. Applying KCL to Fig. 3.39(a) gives

$$I_E = I_B + I_C \tag{3.27}$$

where I_E, I_C, and I_B are emitter, collector, and base currents, respectively. Similarly, applying KVL to Fig. 3.39(b) gives

$$V_{CE} + V_{EB} + V_{BC} = 0 \tag{3.28}$$

where V_{CE}, V_{EB}, and V_{BC} are collector-emitter, emitter-base, and base-collector voltages. The BJT can operate in one of three modes: active, cutoff, and saturation. When transistors operate in the active mode, typically $V_{BE} \simeq 0.7$ V,

$$I_C = \alpha I_E \tag{3.29}$$

where α is called the *common-base current gain.* In Eq. (3.29), α denotes the fraction of electrons injected by the emitter that are collected by the collector. Also,

$$I_C = \beta I_B \tag{3.30}$$

where β is known as the *common-emitter current gain.* The α and β are characteristic properties of a given transistor and assume constant values for that transistor. Typically, α takes values in the range of 0.98 to 0.999, while β takes values in the range 50 to 1000. From Eqs. (3.27) to (3.30), it is evident that

$$I_E = (1 + \beta) I_B \tag{3.31}$$

and

$$\beta = \frac{\alpha}{1 - \alpha} \tag{3.32}$$

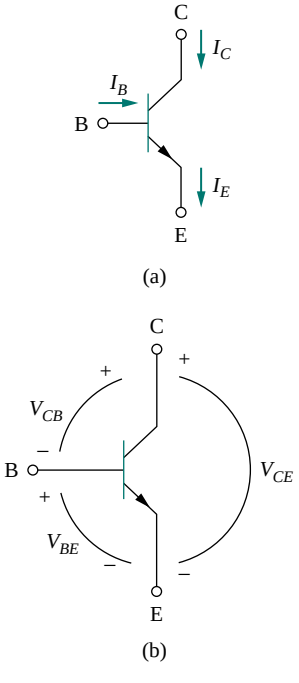


Figure 3.39 The terminal variables of an *npn* transistor: (a) currents, (b) voltages.

In fact, transistor circuits provide motivation to study dependent sources.

These equations show that, in the active mode, the BJT can be modeled as a dependent current-controlled current source. Thus, in circuit analysis, the dc equivalent model in Fig. 3.40(b) may be used to replace the *npn* transistor in Fig. 3.40(a). Since β in Eq. (3.32) is large, a small base current controls large currents in the output circuit. Consequently, the bipolar transistor can serve as an amplifier, producing both current gain and voltage gain. Such amplifiers can be used to furnish a considerable amount of power to transducers such as loudspeakers or control motors.

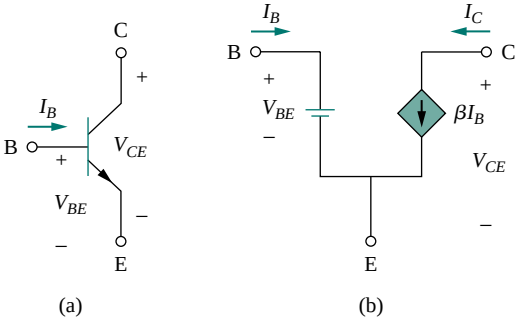


Figure 3.40 (a) An *npn* transistor, (b) its dc equivalent model.

It should be observed in the following examples that one cannot directly analyze transistor circuits using nodal analysis because of the potential difference between the terminals of the transistor. Only when the transistor is replaced by its equivalent model can we apply nodal analysis.

EXAMPLE 3.12

Find I_B, I_C, and v_o in the transistor circuit of Fig. 3.41. Assume that the transistor operates in the active mode and that $\beta = 50$.

Solution:

For the input loop, KVL gives

$$-4 + I_B(20 \times 10^3) + V_{BE} = 0$$

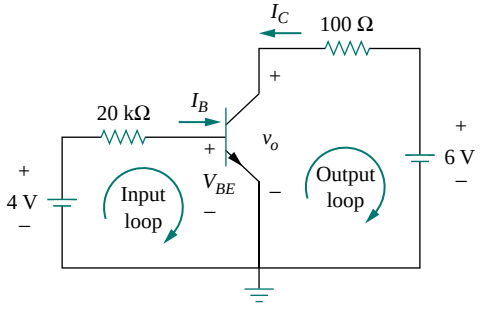


Figure 3.41 For Example 3.12.

Since $V_{BE} = 0.7$ V in the active mode,

$$I_B = \frac{4 - 0.7}{20 \times 10^3} = 165\ \mu\text{A}$$

But

$$I_C = \beta I_B = 50 \times 165\ \mu\text{A} = 8.25\ \text{mA}$$

For the output loop, KVL gives

$$-v_o - 100 I_C + 6 = 0$$

or

$$v_o = 6 - 100 I_C = 6 - 0.825 = 5.175\ \text{V}$$

Note that $v_o = V_{CE}$ in this case.

PRACTICE PROBLEM 3.12

For the transistor circuit in Fig. 3.42, let $\beta = 100$ and $V_{BE} = 0.7$ V. Determine v_o and V_{CE}.

Answer: 2.876 V, 1.984 V.

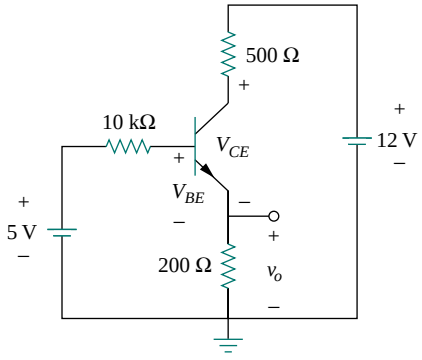


Figure 3.42 For Practice Prob. 3.12.

EXAMPLE 3.13

For the BJT circuit in Fig. 3.43, $\beta = 150$ and $V_{BE} = 0.7$ V. Find v_o.

Solution:

We can solve this problem in two ways. One way is by direct analysis of the circuit in Fig. 3.43. Another way is by replacing the transistor with its equivalent circuit.

METHOD 1 We can solve the problem as we solved the problem in the previous example. We apply KVL to the input and output loops as shown in Fig. 3.44(a). For loop 1,

$$2 = 100 \times 10^3 I_1 + 200 \times 10^3 I_2 \tag{3.13.1}$$

For loop 2,

$$V_{BE} = 0.7 = 200 \times 10^3 I_2 \quad \Longrightarrow \quad I_2 = 3.5\ \mu\text{A} \tag{3.13.2}$$

For loop 3,

$$-v_o - 1000 I_C + 16 = 0$$

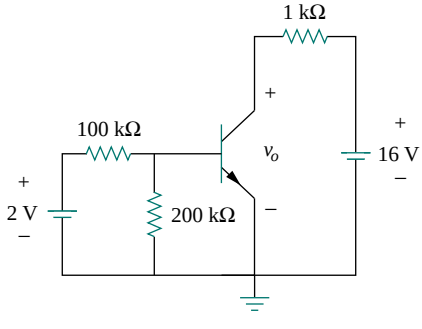


Figure 3.43 For Example 3.13.

or

$$v_o = 16 - 1000I_C \tag{3.13.3}$$

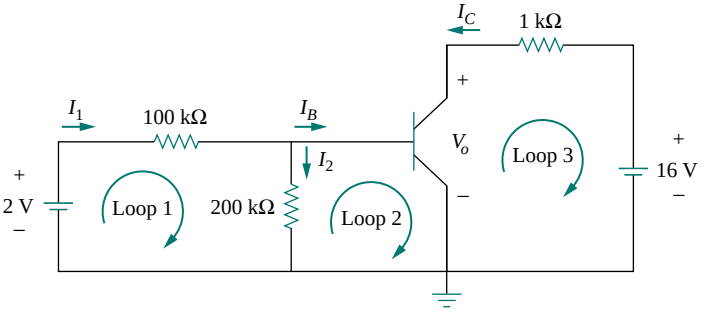
From Eqs. (3.13.1) and (3.13.2),

$$I_1 = \frac{2 - 0.7}{100 \times 10^3} = 13\ \mu\text{A}, \qquad I_B = I_1 - I_2 = 9.5\ \mu\text{A}$$

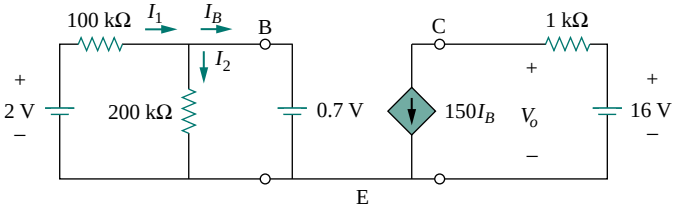
$$I_C = \beta I_B = 150 \times 9.5\ \mu\text{A} = 1.425\ \text{mA}$$

Substituting for I_C in Eq. (3.13.3),

$$v_o = 16 - 1.425 = 14.575\ \text{V}$$



(a)



(b)

Figure 3.44 Solution of the problem in Example 3.13: (a) method 1, (b) method 2.

METHOD 2 We can modify the circuit in Fig. 3.43 by replacing the transistor by its equivalent model in Fig. 3.40(b). The result is the circuit shown in Fig. 3.44(b). Notice that the locations of the base (B), emitter (E), and collector (C) remain the same in both the original circuit in Fig. 3.43 and its equivalent circuit in Fig. 3.44(b). From the output loop,

$$v_o = 16 - 1000(150I_B)$$

But

$$I_B = I_1 - I_2 = \frac{2 - 0.7}{100 \times 10^3} - \frac{0.7}{200 \times 10^3} = (13 - 3.5)\ \mu\text{A} = 9.5\ \mu\text{A}$$

and so

$$v_o = 16 - 1000(150 \times 9.5 \times 10^{-6}) = 14.575\ \text{V}$$

PRACTICE PROBLEM 3.13

The transistor circuit in Fig. 3.45 has $\beta = 80$ and $V_{BE} = 0.7$ V. Find v_o and i_o.

Answer: -3 V, -150 μA.

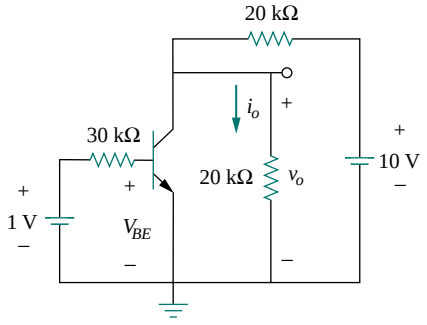


Figure 3.45 For Practice Prob. 3.13.

3.10 SUMMARY

1. Nodal analysis is the application of Kirchhoff's current law at the nonreference nodes. (It is applicable to both planar and nonplanar circuits.) We express the result in terms of the node voltages. Solving the simultaneous equations yields the node voltages.
2. A supernode consists of two nonreference nodes connected by a (dependent or independent) voltage source.
3. Mesh analysis is the application of Kirchhoff's voltage law around meshes in a planar circuit. We express the result in terms of mesh currents. Solving the simultaneous equations yields the mesh currents.
4. A supermesh consists of two meshes that have a (dependent or independent) current source in common.
5. Nodal analysis is normally used when a circuit has fewer node equations than mesh equations. Mesh analysis is normally used when a circuit has fewer mesh equations than node equations.
6. Circuit analysis can be carried out using *PSpice*.
7. DC transistor circuits can be analyzed using the techniques covered in this chapter.

REVIEW QUESTIONS

3.1 At node 1 in the circuit in Fig. 3.46, applying KCL gives:

(a) $2 + \dfrac{12 - v_1}{3} = \dfrac{v_1}{6} + \dfrac{v_1 - v_2}{4}$

(b) $2 + \dfrac{v_1 - 12}{3} = \dfrac{v_1}{6} + \dfrac{v_2 - v_1}{4}$

(c) $2 + \dfrac{12 - v_1}{3} = \dfrac{0 - v_1}{6} + \dfrac{v_1 - v_2}{4}$

(d) $2 + \dfrac{v_1 - 12}{3} = \dfrac{0 - v_1}{6} + \dfrac{v_2 - v_1}{4}$

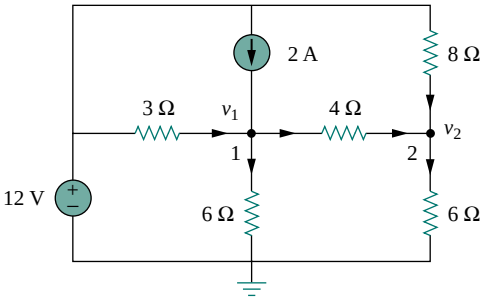


Figure 3.46 For Review Questions 3.1 and 3.2.

3.2 In the circuit in Fig. 3.46, applying KCL at node 2 gives:

(a) $\dfrac{v_2 - v_1}{4} + \dfrac{v_2}{8} = \dfrac{v_2}{6}$

(b) $\dfrac{v_1 - v_2}{4} + \dfrac{v_2}{8} = \dfrac{v_2}{6}$

(c) $\dfrac{v_1 - v_2}{4} + \dfrac{12 - v_2}{8} = \dfrac{v_2}{6}$

(d) $\dfrac{v_2 - v_1}{4} + \dfrac{v_2 - 12}{8} = \dfrac{v_2}{6}$

3.3 For the circuit in Fig. 3.47, v_1 and v_2 are related as:

(a) $v_1 = 6i + 8 + v_2$ (b) $v_1 = 6i - 8 + v_2$

(c) $v_1 = -6i + 8 + v_2$ (d) $v_1 = -6i - 8 + v_2$

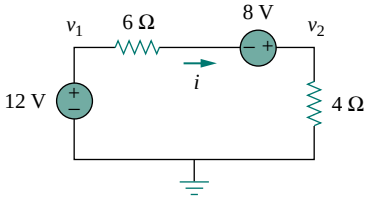


Figure 3.47 For Review Questions 3.3 and 3.4.

3.4 In the circuit in Fig. 3.47, the voltage v_2 is:

(a) −8 V (b) −1.6 V

(c) 1.6 V (d) 8 V

3.5 The current i in the circuit in Fig. 3.48 is:

(a) −2.667 A (b) −0.667 A

(c) 0.667 A (d) 2.667 A

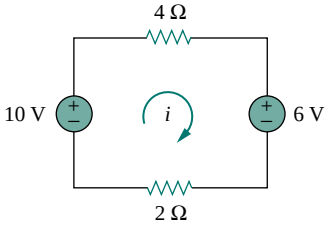


Figure 3.48 For Review Questions 3.5 and 3.6.

3.6 The loop equation for the circuit in Fig. 3.48 is:

(a) $-10 + 4i + 6 + 2i = 0$

(b) $10 + 4i + 6 + 2i = 0$

(c) $10 + 4i - 6 + 2i = 0$

(d) $-10 + 4i - 6 + 2i = 0$

3.7 In the circuit in Fig. 3.49, current i_1 is:

(a) 4 A (b) 3 A (c) 2 A (d) 1 A

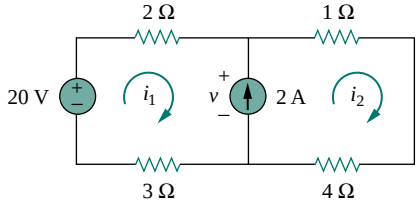


Figure 3.49 For Review Questions 3.7 and 3.8.

3.8 The voltage v across the current source in the circuit of Fig. 3.49 is:

(a) 20 V (b) 15 V (c) 10 V (d) 5 V

3.9 The *PSpice* part name for a current-controlled voltage source is:

(a) EX (b) FX (c) HX (d) GX

3.10 Which of the following statements are not true of the pseudocomponent IPROBE:

(a) It must be connected in series.

(b) It plots the branch current.

(c) It displays the current through the branch in which it is connected.

(d) It can be used to display voltage by connecting it in parallel.

(e) It is used only for dc analysis.

(f) It does not correspond to a particular circuit element.

Answers: 3.1a, 3.2c, 3.3b, 3.4d, 3.5c, 3.6a, 3.7d, 3.8b, 3.9c, 3.10b,d.

PROBLEMS

Sections 3.2 and 3.3 Nodal Analysis

3.1 Determine v_1, v_2, and the power dissipated in all the resistors in the circuit of Fig. 3.50.

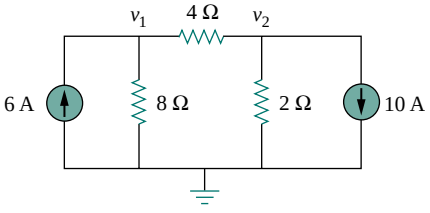


Figure 3.50 For Prob. 3.1.

3.2 For the circuit in Fig. 3.51, obtain v_1 and v_2.

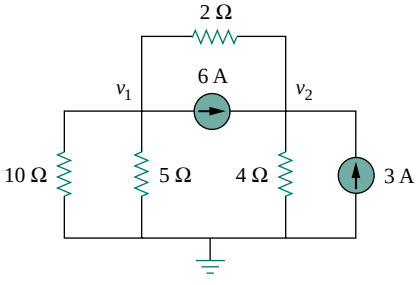


Figure 3.51 For Prob. 3.2.

3.3 Find the currents i_1 through i_4 and the voltage v_o in the circuit in Fig. 3.52.

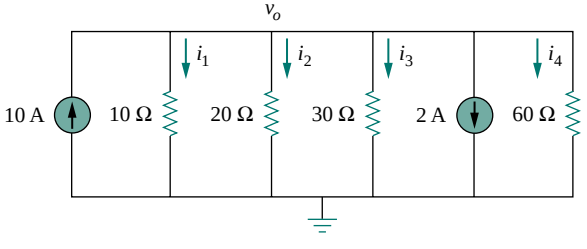


Figure 3.52 For Prob. 3.3.

3.4 Given the circuit in Fig. 3.53, calculate the currents i_1 through i_4.

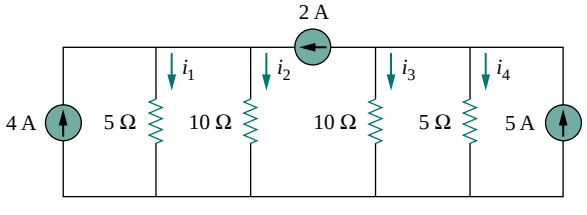


Figure 3.53 For Prob. 3.4.

3.5 Obtain v_o in the circuit of Fig. 3.54.

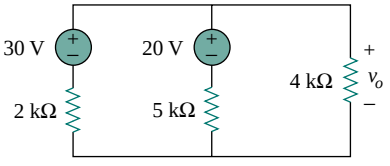


Figure 3.54 For Prob. 3.5.

3.6 Use nodal analysis to obtain v_o in the circuit in Fig. 3.55.

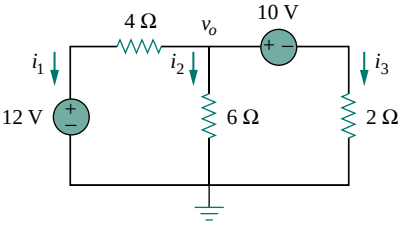


Figure 3.55 For Prob. 3.6.

3.7 Using nodal analysis, find v_o in the circuit of Fig. 3.56.

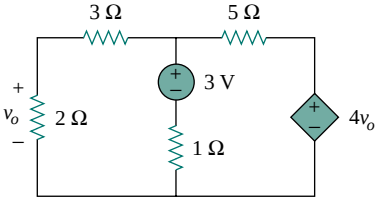


Figure 3.56 For Prob. 3.7.

3.8 Calculate v_o in the circuit in Fig. 3.57.

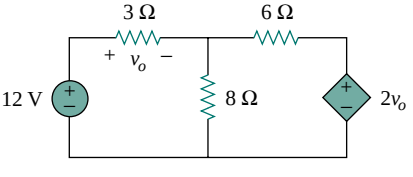


Figure 3.57 For Prob. 3.8.

3.9 Find i_o in the circuit in Fig. 3.58.

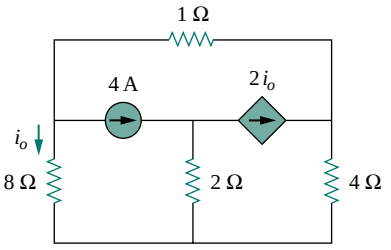


Figure 3.58 For Prob. 3.9.

3.10 Solve for i_1 and i_2 in the circuit in Fig. 3.22 (Section 3.5) using nodal analysis.

3.11 Use nodal analysis to find currents i_1 and i_2 in the circuit of Fig. 3.59.

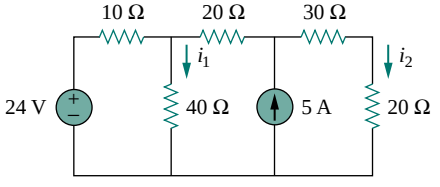


Figure 3.59 For Prob. 3.11.

3.12 Calculate v_1 and v_2 in the circuit in Fig. 3.60 using nodal analysis.

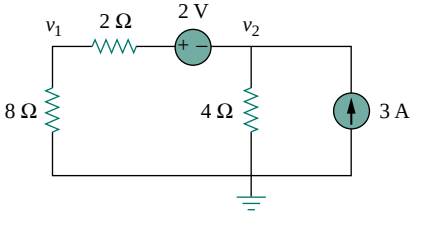


Figure 3.60 For Prob. 3.12.

3.13 Using nodal analysis, find v_o in the circuit of Fig. 3.61.

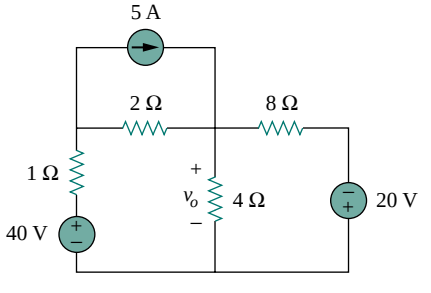


Figure 3.61 For Prob. 3.13.

3.14 Apply nodal analysis to find i_o and the power dissipated in each resistor in the circuit of Fig. 3.62.

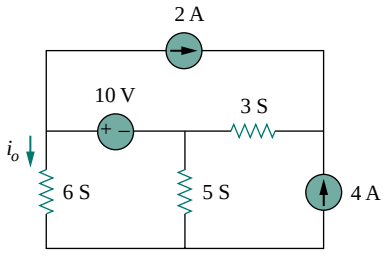


Figure 3.62 For Prob. 3.14.

3.15 Determine voltages v_1 through v_3 in the circuit of Fig. 3.63 using nodal analysis.

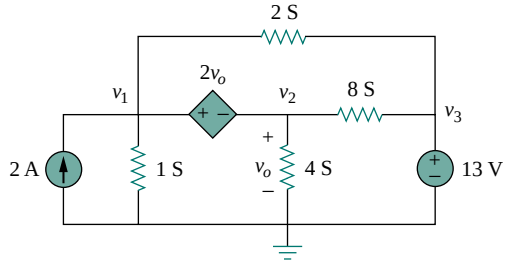


Figure 3.63 For Prob. 3.15.

3.16 Using nodal analysis, find current i_o in the circuit of Fig. 3.64.

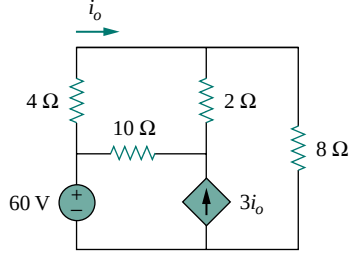


Figure 3.64 For Prob. 3.16.

3.17 Determine the node voltages in the circuit in Fig. 3.65 using nodal analysis.

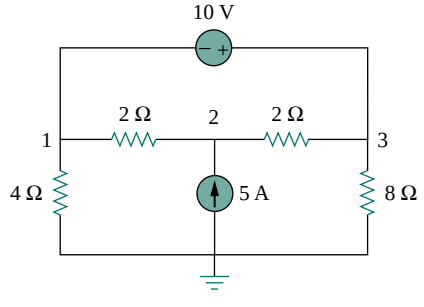


Figure 3.65 For Prob. 3.17.

3.18 For the circuit in Fig. 3.66, find v_1 and v_2 using nodal analysis.

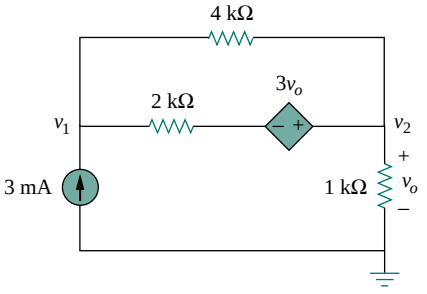


Figure 3.66 For Prob. 3.18.

3.19 Determine v_1 and v_2 in the circuit in Fig. 3.67.

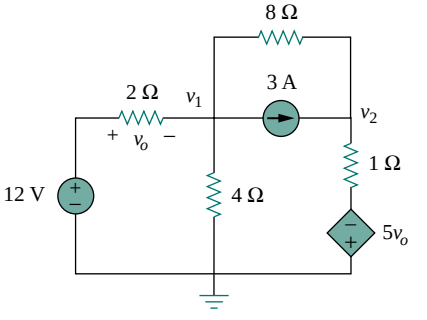


Figure 3.67 For Prob. 3.19.

3.20 Obtain v_1 and v_2 in the circuit of Fig. 3.68.

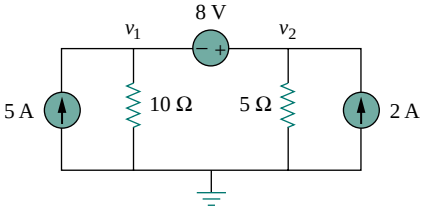


Figure 3.68 For Prob. 3.20.

3.21 Find v_o and i_o in the circuit in Fig. 3.69.

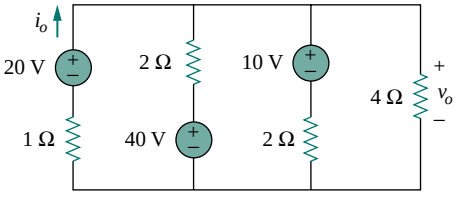


Figure 3.69 For Prob. 3.21.

*An asterisk indicates a challenging problem.

***3.22** Use nodal analysis to determine voltages v_1, v_2, and v_3 in the circuit in Fig. 3.70.

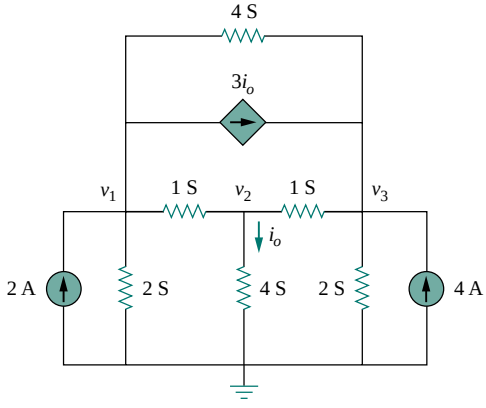


Figure 3.70 For Prob. 3.22.

3.23 Using nodal analysis, find v_o and i_o in the circuit of Fig. 3.71.

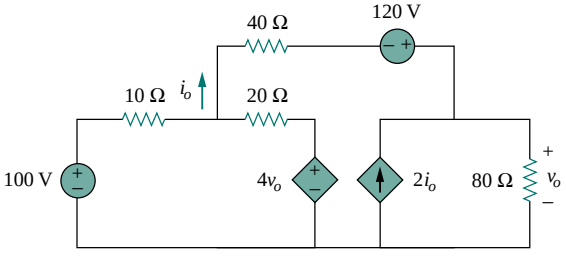


Figure 3.71 For Prob. 3.23.

3.24 Find the node voltages for the circuit in Fig. 3.72.

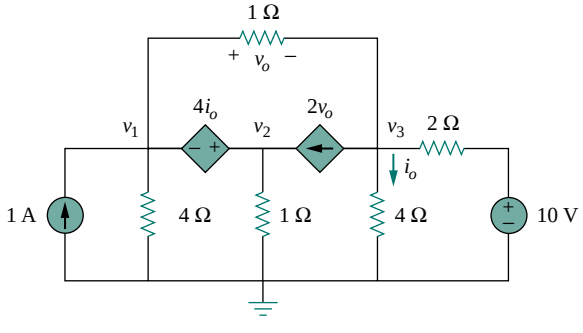


Figure 3.72 For Prob. 3.24.

*3.25 Obtain the node voltages v_1, v_2, and v_3 in the circuit of Fig. 3.73.

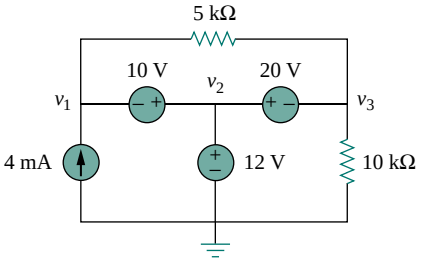
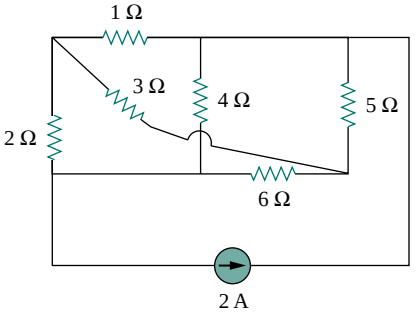


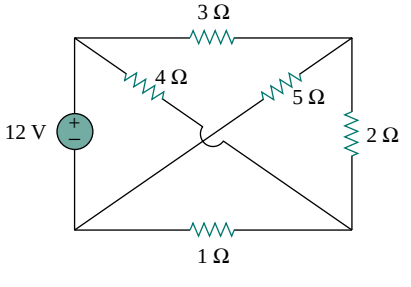
Figure 3.73 For Prob. 3.25.

Sections 3.4 and 3.5 Mesh Analysis

3.26 Which of the circuits in Fig. 3.74 is planar? For the planar circuit, redraw the circuits with no crossing branches.



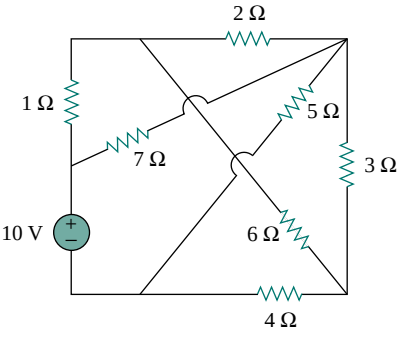
(a)



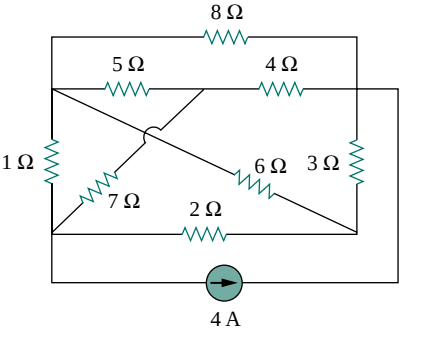
(b)

Figure 3.74 For Prob. 3.26.

3.27 Determine which of the circuits in Fig. 3.75 is planar and redraw it with no crossing branches.



(a)



(b)

Figure 3.75 For Prob. 3.27.

3.28 Rework Prob. 3.5 using mesh analysis.

3.29 Rework Prob. 3.6 using mesh analysis.

3.30 Solve Prob. 3.7 using mesh analysis.

3.31 Solve Prob. 3.8 using mesh analysis.

3.32 For the bridge network in Fig. 3.76, find i_o using mesh analysis.

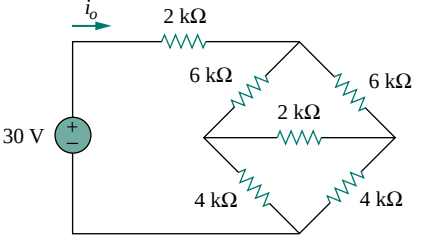


Figure 3.76 For Prob. 3.32.

3.33 Apply mesh analysis to find i in Fig. 3.77.

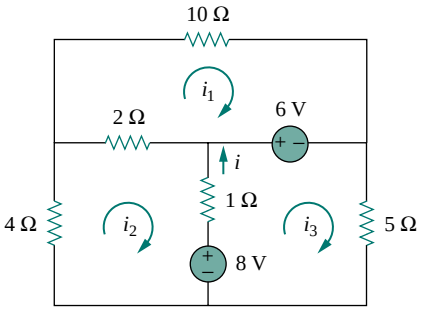


Figure 3.77 For Prob. 3.33.

3.34 Use mesh analysis to find v_{ab} and i_o in the circuit in Fig. 3.78.

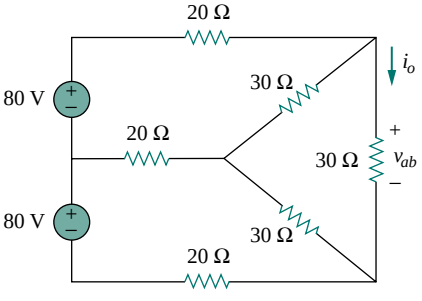


Figure 3.78 For Prob. 3.34.

3.35 Use mesh analysis to obtain i_o in the circuit of Fig. 3.79.

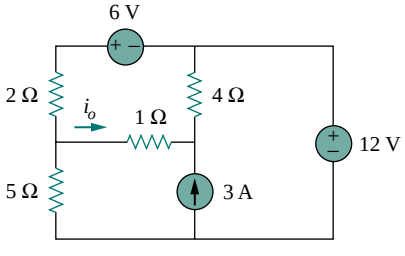


Figure 3.79 For Prob. 3.35.

3.36 Find current i in the circuit in Fig. 3.80.

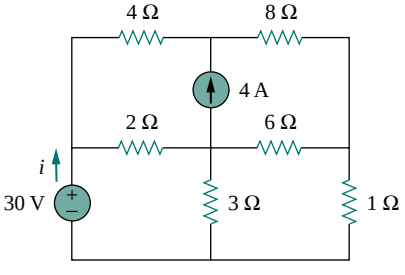


Figure 3.80 For Prob. 3.36.

3.37 Find v_o and i_o in the circuit of Fig. 3.81.

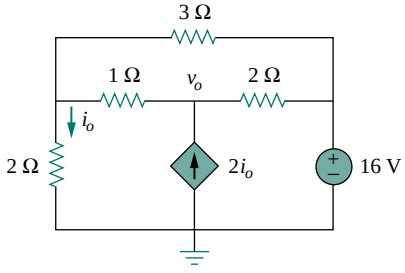


Figure 3.81 For Prob. 3.37.

3.38 Use mesh analysis to find the current i_o in the circuit in Fig. 3.82.

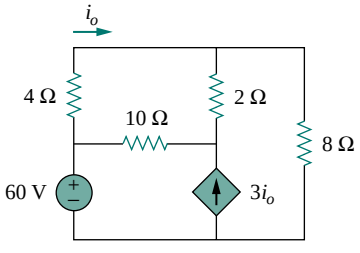


Figure 3.82 For Prob. 3.38.

3.39 Apply mesh analysis to find v_o in the circuit in Fig. 3.83.

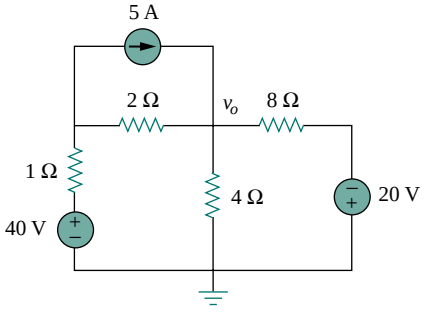


Figure 3.83 For Prob. 3.39.

3.40 Use mesh analysis to find i_1, i_2, and i_3 in the circuit of Fig. 3.84.

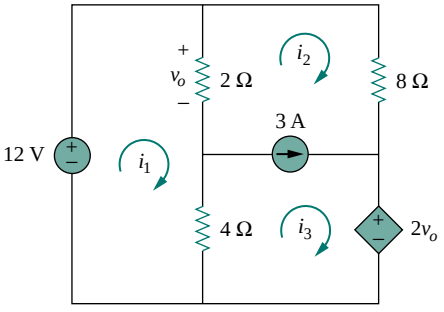


Figure 3.84 For Prob. 3.40.

3.41 Rework Prob. 3.11 using mesh analysis.

*__3.42__ In the circuit of Fig. 3.85, solve for i_1, i_2, and i_3.

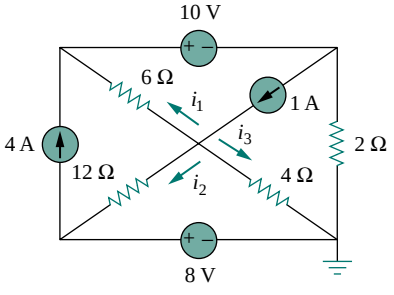


Figure 3.85 For Prob. 3.42.

3.43 Determine v_1 and v_2 in the circuit of Fig. 3.86.

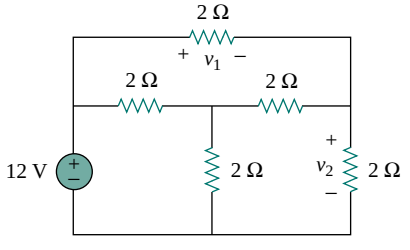


Figure 3.86 For Prob. 3.43.

3.44 Find i_1, i_2, and i_3 in the circuit in Fig. 3.87.

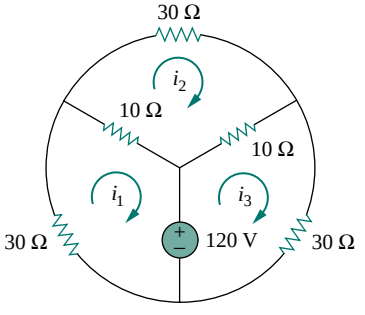


Figure 3.87 For Prob. 3.44.

3.45 Rework Prob. 3.23 using mesh analysis.

3.46 Calculate the power dissipated in each resistor in the circuit in Fig. 3.88.

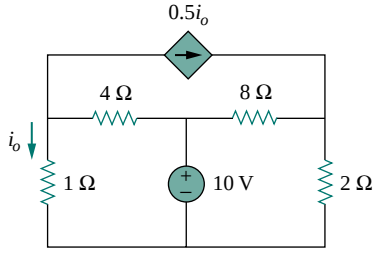


Figure 3.88 For Prob. 3.46.

3.47 Calculate the current gain i_o/i_s in the circuit of Fig. 3.89.

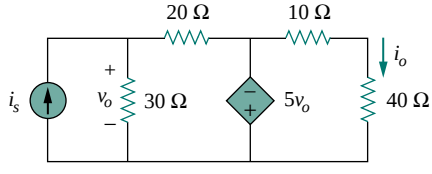


Figure 3.89 For Prob. 3.47.

3.48 Find the mesh currents i_1, i_2, and i_3 in the network of Fig. 3.90.

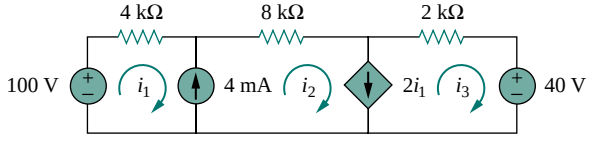


Figure 3.90 For Prob. 3.48.

3.49 Find v_x and i_x in the circuit shown in Fig. 3.91.

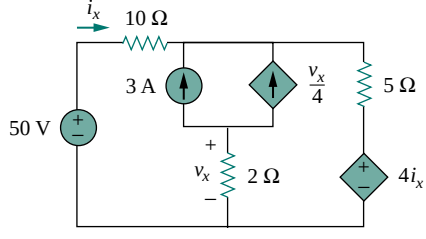


Figure 3.91 For Prob. 3.49.

3.50 Find v_o and i_o in the circuit of Fig. 3.92.

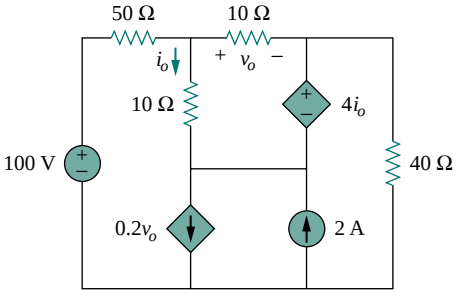


Figure 3.92 For Prob. 3.50.

Section 3.6 Nodal and Mesh Analyses by Inspection

3.51 Obtain the node-voltage equations for the circuit in Fig. 3.93 by inspection. Determine the node voltages v_1 and v_2.

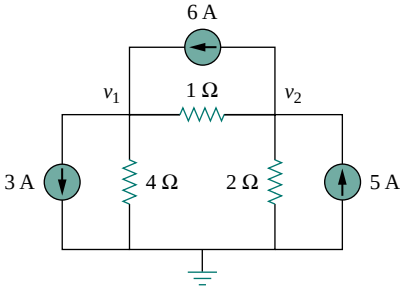


Figure 3.93 For Prob. 3.51.

3.52 By inspection, write the node-voltage equations for the circuit in Fig. 3.94 and obtain the node voltages.

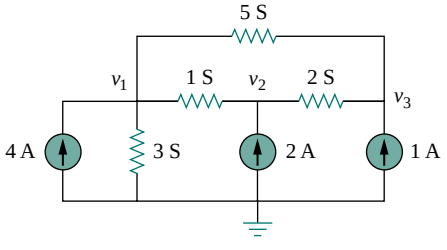


Figure 3.94 For Prob. 3.52.

3.53 For the circuit shown in Fig. 3.95, write the node-voltage equations by inspection.

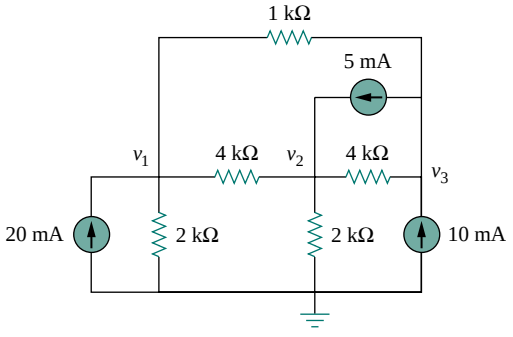


Figure 3.95 For Prob. 3.53.

3.54 Write the node-voltage equations of the circuit in Fig. 3.96 by inspection.

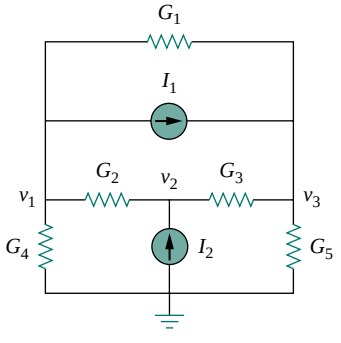


Figure 3.96 For Prob. 3.54.

3.55 Obtain the mesh-current equations for the circuit in Fig. 3.97 by inspection. Calculate the power absorbed by the 8-Ω resistor.

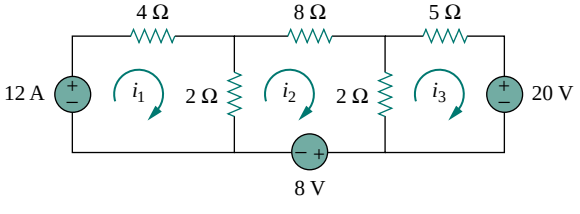


Figure 3.97 For Prob. 3.55.

3.56 By inspection, write the mesh-current equations for the circuit in Fig. 3.98.

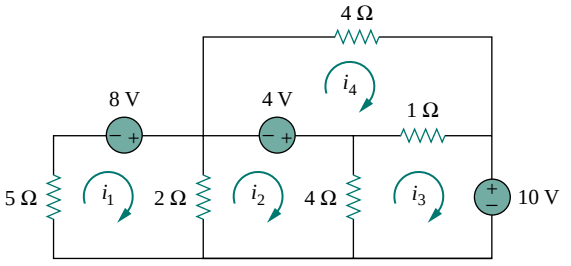


Figure 3.98 For Prob. 3.56.

3.57 Write the mesh-current equations for the circuit in Fig. 3.99.

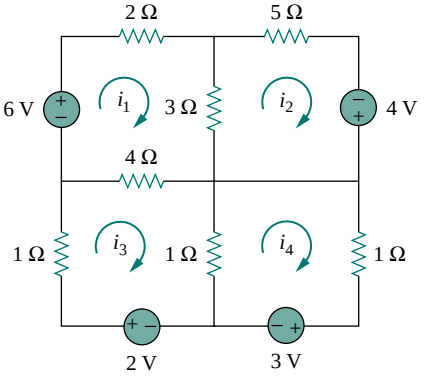


Figure 3.99 For Prob. 3.57.

3.58 By inspection, obtain the mesh-current equations for the circuit in Fig. 3.100.

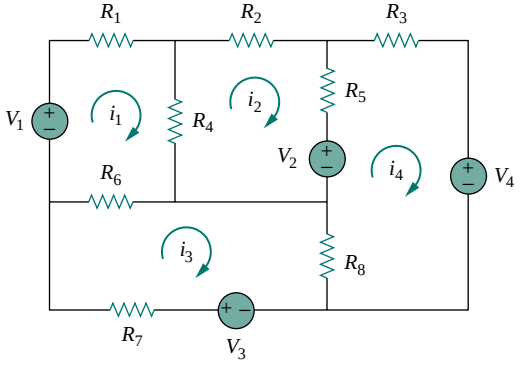


Figure 3.100 For Prob. 3.58.

Section 3.8 Circuit Analysis with *PSpice*

3.59 Use *PSpice* to solve Prob. 3.44.

3.60 Use *PSpice* to solve Prob. 3.22.

3.61 Rework Prob. 3.51 using *PSpice*.

3.62 Find the nodal voltages v_1 through v_4 in the circuit in Fig. 3.101 using *PSpice*.

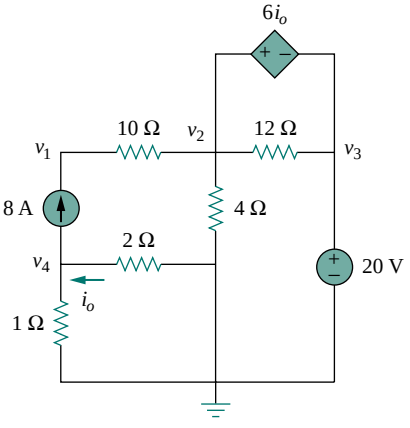


Figure 3.101 For Prob. 3.62.

3.63 Use *PSpice* to solve the problem in Example 3.4.

3.64 If the Schematics Netlist for a network is as follows, draw the network.

```
R_R1    1   2   2K
R_R2    2   0   4K
R_R3    3   0   8K
R_R4    3   4   6K
R_R5    1   3   3K
V_VS    4   0   DC      100
I_IS    0   1   DC      4
F_F1    1   3   VF_F1   2
VF_F1   5   0   0V
E_E1    3   2   1       3     3
```

3.65 The following program is the Schematics Netlist of a particular circuit. Draw the circuit and determine the voltage at node 2.

```
R_R1   1   2   20
R_R2   2   0   50
R_R3   2   3   70
R_R4   3   0   30
V_VS   1   0   20V
I_IS   2   0   DC    2A
```

Section 3.9 Applications

3.66 Calculate v_o and i_o in the circuit of Fig. 3.102.

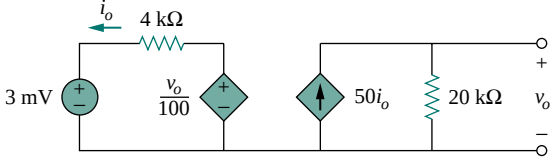


Figure 3.102 For Prob. 3.66.

3.67 For the simplified transistor circuit of Fig. 3.103, calculate the voltage v_o.

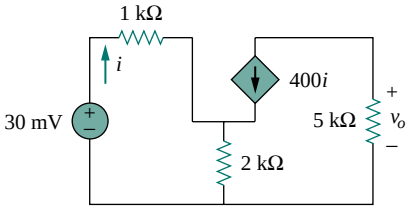


Figure 3.103 For Prob. 3.67.

3.68 For the circuit in Fig. 3.104, find the gain v_o/v_s.

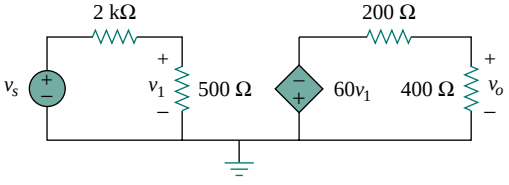


Figure 3.104 For Prob. 3.68.

*__3.69__ Determine the gain v_o/v_s of the transistor amplifier circuit in Fig. 3.105.

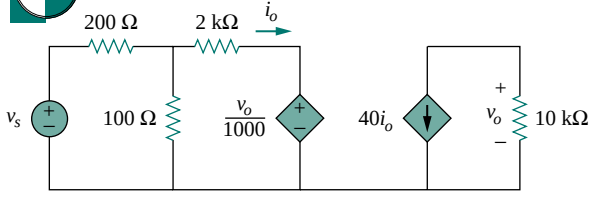


Figure 3.105 For Prob. 3.69.

3.70 For the simple transistor circuit of Fig. 3.106, let $\beta = 75$, $V_{BE} = 0.7$ V. What value of v_i is required to give a collector-emitter voltage of 2 V?

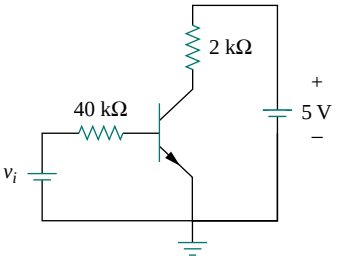


Figure 3.106 For Prob. 3.70.

3.71 Calculate v_s for the transistor in Fig. 3.107 given that $v_o = 4$ V, $\beta = 150$, $V_{BE} = 0.7$ V.

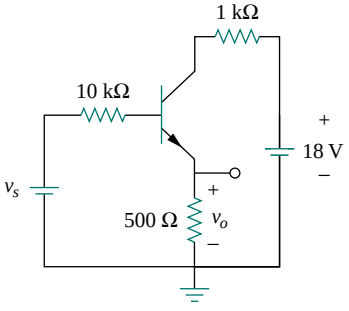


Figure 3.107 For Prob. 3.71.

3.72 For the transistor circuit of Fig. 3.108, find I_B, V_{CE}, and v_o. Take $\beta = 200$, $V_{BE} = 0.7$ V.

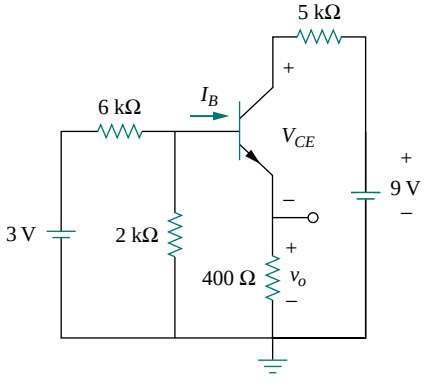


Figure 3.108 For Prob. 3.72.

3.73 Find I_B and V_C for the circuit in Fig. 3.109. Let $\beta = 100$, $V_{BE} = 0.7$ V.

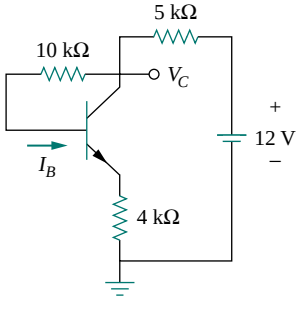


Figure 3.109 For Prob. 3.73.

COMPREHENSIVE PROBLEMS

*__3.74__ Rework Example 3.11 with hand calculation.