Appendix C Sample Layout Rules

The rules given in this appendix were developed for use with the problems presented in the text. The numerical values given here do not correspond to any single process, but they are broadly representative of industry practices during the late 1980s. No attempt has been made to bring the rules in line with the current state of the art because this would greatly increase their complexity without providing any additional insight. For much the same reasons, many seldom-used rules have been omitted entirely or have been relegated to individual problem descriptions.

SECTION C.1 STANDARD BIPOLAR RULES

The standard bipolar process presented here is a 30V process using a single P+ isolation. The isolation spacings for this process are significantly wider than the illustrations in the text might suggest. Modern processes generally use up/down isolation to reduce these spacings, bringing them more in line with the illustrations. Table C.1 lists key electrical parameters of this process.

The baseline process uses eight coding layers: NBL, TANK, DEEPN, BASE, EMIT, CONT, METAL1, and POR. The TANK and POR (protective overcoat removal) layers code for openings in the isolation diffusion and protective overcoat, respectively. Base-over-isolation (BOI) is automatically generated from the geometries coded on the TANK layer. Two process extensions are described, one producing 2kΩ/□ HSR resistors and one generating Schottky diodes. Table C.2 lists the baseline layout rules, while Tables C.3 and C.4 list the rules for the HSR and Schottky contact process extensions, respectively. All of the rules are given in microns, assuming a coding grid of 2μm. Section C.3 explains the syntax used to describe the layout rules.

TABLE C.1 Standard bipolar parametric specifications.

Parameter	Min	Mean	Max	Units
NPN beta	100	200	300	
NPN V_{EBO}	6.4	6.8	7.2	V
NPN V_{CBO}	40			V
NPN V_{CEO}	30			V
Base sheet	130	160	190	Ω/□
Emitter sheet	5	7	10	Ω/□
Pinched base sheet	1.5	3	4.5	kΩ/□
HSR sheet	1.6	2	2.4	kΩ/□
Thick-field threshold	35			V

TABLE C.2 Standard bipolar baseline rules.

1. NBL width	8μm
2. TANK width	8μm
3. TANK spacing to TANK	6μm
4. TANK overlap NBL	22μm
5. DEEPN width	8μm
6. TANK overlap DEEPN	24μm
7. BASE width	6μm
8. BASE spacing to DEEPN	18μm
9. BASE spacing to BASE	14μm
10. TANK overlap BASE	22μm
11. EMIT width	6μm
12. BASE spacing to EMIT	12μm
13. EMIT spacing to EMIT	6μm
14. TANK overlap EMIT	18μm
15. BASE overlap EMIT	4μm
16. CONT width	4μm
17. EMIT spacing to CONT	6μm
18. CONT spacing to CONT	4μm
19. BASE overlap CONT	2μm
20. EMIT overlap CONT	2μm
21. METAL1 width	6μm
22. METAL1 spacing to METAL1	4μm
23. METAL1 overlap CONT	2μm
24. POR width	10μm
25. POR spacing to POR	10μm
26. METAL1 overlap POR	4μm

TABLE C.3 Standard bipolar HSR extension rules.

27. HSR width	6μm
28. HSR spacing to DEEPN	16μm
29. HSR spacing to BASE	14μm
30. HSR spacing to EMIT	10μm
31. HSR spacing to CONT	4μm
32. HSR spacing to HSR	12μm
33. BASE overhang HSR	2μm

34. HSR extends into BASE	2μm
35. TANK overlap HSR	20μm
36. SCONT spacing DEEPN	12μm
37. SCONT spacing to BASE	6μm
38. SCONT spacing to EMIT	4μm
39. SCONT spacing to HSR	4μm
40. SCONT spacing to CONT	4μm
41. SCONT spacing to SCONT	4μm
42. SCONT overlap CONT	2μm
43. METAL1 overlap SCONT	2μm

TABLE C.4 Standard bipolar Schottky extension rules.

SECTION C.2 POLYSILICON-GATE CMOS RULES

This section describes a 10V, N-well, poly-gate CMOS process. The LDD NMOS has a minimum allowed channel length of 4μm, while the SDD PMOS allows channel lengths as short as 3μm. Both transistors use the same N-type gate poly, and a single boron threshold adjust sets both threshold voltages simultaneously. A combination of boron and phosphorus channel stops ensure that both the NMOS and the PMOS thick-field thresholds lie safely above the operating voltage of the process. CMOS latchup is minimized by the use of a P+ substrate and by optional availability of NBL as part of the analog BiCMOS process extension. This process cannot fabricate Schottky diodes because it uses titanium silicide to minimize contact resistance. Table C.5 lists key electrical parameters of this process.

Parameter	Min	Mean	Max	Units
NMOS V_t	0.5	0.7	0.9	V
NMOS k	50	70	90	$\mu A/V^2$
NMOS V_{DS}	10			V
NMOS V_{GS}	12			V
PMOS V_t	–0.9	–0.7	–0.5	V
PMOS k	17	25	33	$\mu A/V^2$
PMOS V_{DS}	12			V
PMOS V_{GS}	12			V
Thick-field thresholds	15			V
Poly-1 sheet	20	30	40	Ω/□
Poly-2 sheet (w/PSD)	160	200	240	Ω/□
Base sheet	400	500	600	Ω/□
Gate oxide capacitance	0.85	0.95	1.05	$fF/\mu m^2$
Poly-poly capacitance	1.3	1.5	1.7	$fF/\mu m^2$
NPN beta	40	80	120	
NPN V_{EBO}	7	8	9	V
NPN V_{CBO}	15			V
NPN V_{CEO}	12			V

TABLE C.5 Polysilicon-gate CMOS parametric specifications.

The baseline process as described in Table C.6 uses eleven masks: NWELL, MOAT, NSD, PSD, CHST, POLY1, CONT. METAL1, VIA, METAL2, and POR. These eleven masks are normally coded using nine drawing layers: NWELL, NMOAT, PMOAT, POLY1, CONT, METAL1, VIA, METAL2, and POR. The NMOAT drawing layer simultaneously produces geometries on the MOAT and NSD masks. The PMOAT drawing layer simultaneously produces geometries on the MOAT and PSD masks. The information for the CHST mask is obtained from the

TABLE C.6 Poly-gate CMOS baseline rules.

1. NWELL width	5.0μm
2. NWELL spacing to NWELL	15.0μm
3. NMOAT width	3.0μm
4. NMOAT spacing to NWELL	9.5μm
5. NMOAT spacing to NMOAT	5.5μm
6. NWELL overlap NMOAT	1.0μm
7. PMOAT width	3.0μm
8. PMOAT spacing to NWELL	7.0μm
9. PMOAT spacing to NMOAT *(note 1)*	4.0μm
10. PMOAT spacing to PMOAT	5.5μm
11. NWELL overlap PMOAT	2.0μm
12. POLY1 width	2.0μm
13. POLY1 spacing to NMOAT	2.0μm
14. POLY1 spacing to PMOAT	2.0μm
15. POLY1 spacing to POLY1	2.0μm
16. POLY1 overhang NMOAT	1.0μm
17. POLY1 overhang PMOAT	1.0μm
18. NMOAT overhang POLY1	4.0μm
19. PMOAT overhang POLY1	4.0μm
20. CONT width	1.0μm exactly
21. CONT spacing to POLY1	2.0μm
22. CONT spacing to CONT	2.0μm
23. NMOAT overlap CONT	1.0μm
24. PMOAT overlap CONT	1.0μm
25. POLY1 overlap CONT	1.0μm
26. METAL1 width	2.0μm
27. METAL1 spacing to METAL1	2.0μm
28. METAL1 overlap CONT	1.0μm
29. VIA width *(note 2)*	1.0μm exactly
30. VIA spacing to CONT *(note 3)*	2.0μm
31. VIA spacing to VIA	2.0μm
32. METAL1 overlap VIA	1.0μm
33. METAL2 width	2.0μm
34. METAL2 spacing to METAL2	2.0μm
35. METAL2 overlap VIA	1.0μm
36. POR width	4.0μm
37. POR spacing to POR	4.0μm
38. METAL2 overlap POR	2.0μm

Notes: [1] PMOAT allowed to abut NMOAT if the two are connected by METAL1.
[2] Except for bondpads.
[3] VIA must not touch CONT.

NWELL and MOAT coding layers. The geometries on the POR mask represent openings in the protective overcoat. All of these layout rules are given in microns and presume a coding grid of 0.5μm. Section C.3 explains the syntax used to describe the layout rules.

This process supports two extensions, the first of which adds a second layer of polysilicon to the process using the POLY2 mask. This poly is deposited in a near-intrinsic state and is doped with PSD using the PSD drawing layer to produce poly resistors. A thin oxide-nitride-oxide dielectric deposited between the two polysilicon layers provides poly-poly capacitors. Table C.7 lists all of the rules associated with this extension.

39. POLY2 width	2.0μm
40. POLY2 spacing to POLY2	2.0μm
41. NSD spacing to POLY2	2.0μm
42. PSD spacing to POLY2	2.0μm
43. POLY2 overlap CONT	1.0μm
44. POLY1 overlap POLY2	1.5μm
45. NSD overlap POLY2	1.5μm
46. PSD overlap POLY2	1.5μm
47. PSD spacing to NMOAT	2.0μm
48. NSD spacing to PMOAT	2.0μm

TABLE C.7 Poly-2 extension rules.

The second process extension adds analog BiCMOS functionality using three additional masks: NBL, DEEPN, and BASE. Data coded on the BASE drawing layer automatically generates geometries on both the MOAT and the BASE masks. The addition of an N-buried layer forces the process to incorporate a second epitaxial layer for compatibility with a P+ substrate. This process extension allows the creation of vertical NPN transistors, lateral PNP transistors, and substrate PNP transistors. Table C.8 lists the layout rules required to construct analog BiCMOS structures.

47. NBL width	5.0μm
48. NBL spacing to NBL	19.0μm
49. NWELL spacing to NBL	16.5μm
50. NWELL overlap NBL	5.0μm
51. DEEPN width	5.0μm
52. DEEPN spacing to NMOAT	6.0μm
53. DEEPN spacing to PMOAT	7.5μm
54. DEEPN spacing to DEEPN	9.0μm
55. NWELL overlap DEEPN	2.0μm
56. BASE width	3.0μm
57. BASE spacing to NMOAT	4.5μm
58. BASE spacing to PMOAT	6.0μm
59. BASE spacing to DEEPN	8.0μm
60. BASE spacing to BASE	6.5μm
61. BASE overlap NSD	1.5μm
62. PSD overlap BASE	1.0μm
63. NWELL overlap BASE	3.0μm
64. NSD spacing to CONT	2.5μm
65. NSD spacing to PSD	3.0μm
66. NSD spacing to PSD	3.5μm
67. NSD overlap CONT	1.0μm
68. PSD overlap CONT	1.0μm
69. BASE overlap CONT	1.0μm

Note: Used for constructing NPN transistors, but not for lateral PNPs.

TABLE C.8 BiCMOS extension rules.

SECTION C.3 LAYOUT RULE SYNTAX

The layout rules listed in this appendix follow a format that is similar (but not identical) to that of Chameleon, a layout verification program developed at Texas Instruments beginning in 1976 and currently supported and marketed by K2 Technologies. This notation resembles plain English and is therefore particularly

easy for novices to understand. Those employing other verification programs should have little difficulty translating the rules into the appropriate format, particularly since all of the rules fall into one of five elementary categories: width, spacing, overlap, overhang, and extent into. The following sections explain each of these types of rules.

Width

A width check verifies that all dimensions of every geometry on a given layer equal or exceed a minimum feature size. The syntax for a width check is

LAYER1 width N μm

where N is the minimum allowed dimension of all geometries on LAYER1. In order for the geometry of Figure C.1 to pass the above width check, dimensions A to D must all equal or exceed the minimum width, N. Occasionally the dimension will be followed by the notation "exactly." In such cases, the width of every figure on the indicated layer must equal exactly N microns, neither more nor less.

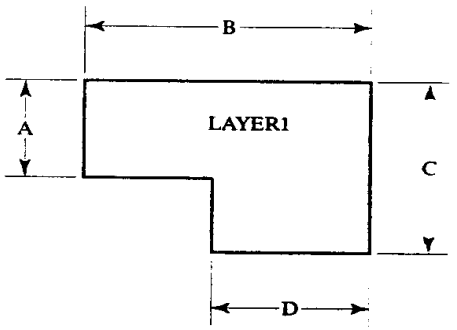

FIGURE C.1 Dimensions checked by "LAYER1 width."

Spacing

A spacing check verifies that all geometries on the specified layers maintain a minimum separation from one another. The syntax for a spacing check is

LAYER1 spacing to LAYER2 N μm

This check determines the minimum distance from each geometry on LAYER1 to each geometry on LAYER2. A violation occurs if any of these distances is less than N. Elements that touch or overlap do not violate the spacing. A spacing check may also be applied to a single layer using the syntax

LAYER1 spacing to LAYER1 N μm

In this case, the check applies not only to the separation between any two geometries on LAYER1 but also to separate portions of a single geometry, such as the turns of a serpentine resistor (for an example, see dimension C in Figure C.2).

Overlap

An overlap check only applies to geometries on a first layer that are partially or wholly enclosed by geometries on a second layer (Figure C.3). The syntax of an overlap check is

LAYER1 overlap LAYER2 N μm

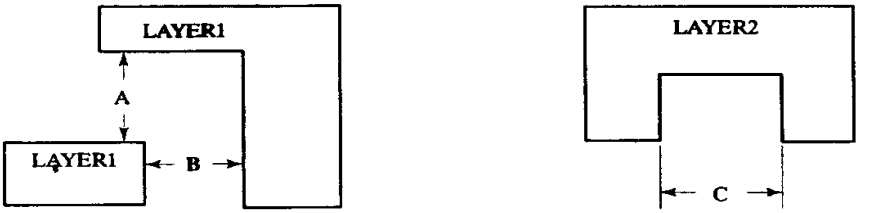

FIGURE C.2 Dimensions checked by "LAYER1 spacing to LAYER1."

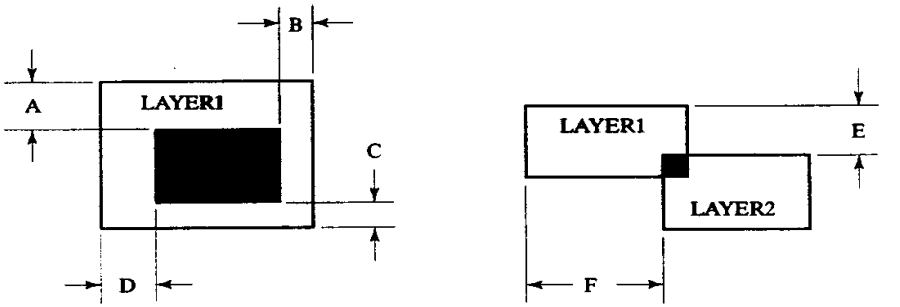

FIGURE C.3 Dimensions checked by "LAYER1 overlap LAYER2."

Wherever a geometry on LAYER1 encloses a geometry on LAYER2, the amount by which the former geometry overlaps the latter must equal or exceed *N*. If the geometries do not completely overlap, the sides that do not overlap automatically pass the check. Figure C.3 shows examples of fully and partially overlapped geometries and the dimensions checked in each case.

Overhang

An overhang check only applies to cases where a geometry on one layer partially overlaps a geometry on another (Figure C.4). The syntax of an overhang check is

LAYER1 overhang LAYER2 *N* μm

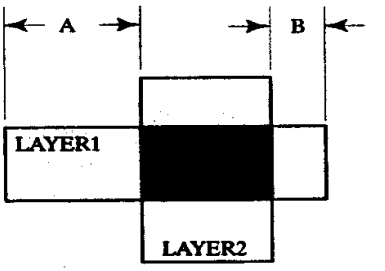

FIGURE C.4 Dimensions checked by "LAYER1 overhang LAYER2."

Wherever a geometry on LAYER1 partially overlaps a geometry on LAYER2, the amount by which the former geometry extends beyond the latter must equal or exceed *N*. Cases where the former geometry is fully enclosed by the latter automatically pass the check.

Extent Into

An extent into check only applies to cases where a geometry on one layer partially overlaps a geometry on another (Figure C.5). The syntax of an extent into check is

LAYER1 extends into LAYER2 *N* μm

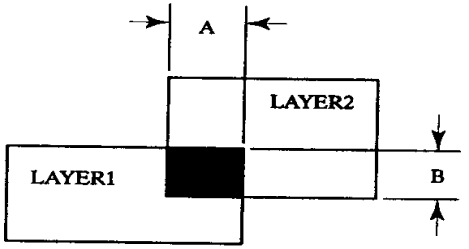

FIGURE C.5 Dimensions checked by "LAYER1 extends into LAYER2."

Wherever a geometry on LAYER1 partially overlaps a geometry on LAYER2, the amount by which the former geometry extends into the latter must equal or exceed *N*. Cases where the former geometry is fully enclosed by the latter automatically pass the check.