Appendix A

Table of Acronyms Used in the Text

AC	Alternating Current
A/D	Analog-to-Digital
BCLDD	Buried-Channel Lightly Doped Drain
BiCMOS	Bipolar and Complementary Metal-Oxide-Semiconductor
BiFET	Bipolar and junction Field-Effect Transistor
BJT	Bipolar Junction Transistor
BOI	Base Over Isolation
BPSG	BoroPhosphoSilicate Glass
CDI	Collector Diffused Isolation
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposited
D/A	Digital-to-Analog
DC	Direct Current
DCML	Differential Current-Mode Logic
DDD	Double-Diffused Drain
DIP	Dual In-line Package
DLM	Double-Level Metal
DMOS	Double-diffused Metal-Oxide-Semiconductor
DRAM	Dynamic Random-Access Memory
DSW	Direct Step on Wafer
ECL	Emitter-Coupled Logic
EEPROM	Electrically Erasable Programmable Read-Only Memory

EOS	Electrical OverStress
ESD	ElectroStatic Discharge
FBSOA	Forward-Biased Safe Operating Area
FET	Field-Effect Transistor
GPM	Gross Profit Margin
HBM	Human-Body Model
HF	Hydrofluoric acid (chemical formula)
HSR	High-Sheet Resistor
IC	Integrated Circuit
ILO	InterLevel Oxide
IPTAT	current Proportional To Absolute Temperature
JFET	Junction Field-Effect Transistor
JI	Junction Isolation
LDD	Lightly Doped Drain
LDMOS	Lateral Double-diffused Metal-Oxide-Semiconductor
LED	Light-Emitting Diode
LOCOS	LOCal Oxidation of Silicon
LPCVD	Low-Pressure Chemical Vapor Deposition
LSTTL	Low-power Schottky-clamped Transistor-Transistor Logic
MLO	MultiLevel Oxide
MM	Machine Model
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NBL	N-type Buried Layer
NMOS	N-channel Metal-Oxide-Semiconductor
NSD	N-type Source/Drain
ONO	Oxide-Nitride-Oxide
OR	Oxide Removal
PBL	P-type Buried Layer
PG	Pattern Generation
PMOS	P-channel Metal-Oxide-Semiconductor
PO	Protective Overcoat
PPM	Parts Per Million
PSD	P-type Source/Drain
PSG	PhosphoSilicate Glass
RIE	Reactive Ion Etch(ing)
SCL	Space Charge Layer
SCR	Silicon Controlled Rectifier
SDD	Single-Diffused Drain (or Single-Doped Drain)
SI	*Systéme Internationale* (the metric system)
SLM	Single-Level Metal
SOA	Safe Operating Area

SOIC	Small-Outline Integrated Circuit
SPICE	Simulation Program with Integrated Circuit Emphasis
SSA	Super Self-Aligned
TCR	Temperature Coefficient of Resistivity
TDDB	Time-Dependent Dielectric Breakdown
TEOS	TetraEthOxySilane
TTL	Transistor-Transistor Logic
UV	UltraViolet
VLSI	Very Large-Scale Integration
VPTAT	Voltage Proportional To Absolute Temperature