Report for the pyArchSim Project

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Abstract

This report presents the design, implementation, and evaluation of the pyArchSim project, a modular simulation tool for architectural structures and computer architecture research. The project is developed in Python and emphasizes extensibility, performance, and ease of integration with visualization and analysis tools.

A significant contribution of this work is the implementation of a flexible and efficient cache module (`cache.py`), which supports direct-mapped, set-associative, and fully-associative configurations. The cache module enables users to experiment with different memory hierarchy designs and observe their impact on system performance. The report details the cache's design, integration with the processor and memory subsystems, and demonstrates its effectiveness through functional and performance testing. Overall, pyArchSim provides a robust platform for both educational and research purposes in computer architecture.

1 Introduction

The pyArchSim project [3] is a simulation tool developed to model and analyze architectural structures. Its goals include:

- Providing accurate simulations of structural behaviors.
- Enabling easy integration with visualization tools.
- Facilitating quick prototyping and iterative development.

The tool [3] is implemented using Python and several open-source libraries, making it accessible to a wide range of users in both academic and industry settings.

A key feature of pyArchSim is its modular memory subsystem [4], which includes a flexible and efficient cache implementation. The cache is designed to support various configurations, such as direct-mapped, set-associative, and fully-associative modes [1,5]. This allows users to experiment with different cache architectures and study their impact on system performance. The cache helps reduce memory access latency by storing frequently accessed data closer to the processor, thus improving overall simulation efficiency. The implementation supports standard cache operations, LRU replacement policy [2], and easy integration with the processor and memory modules.

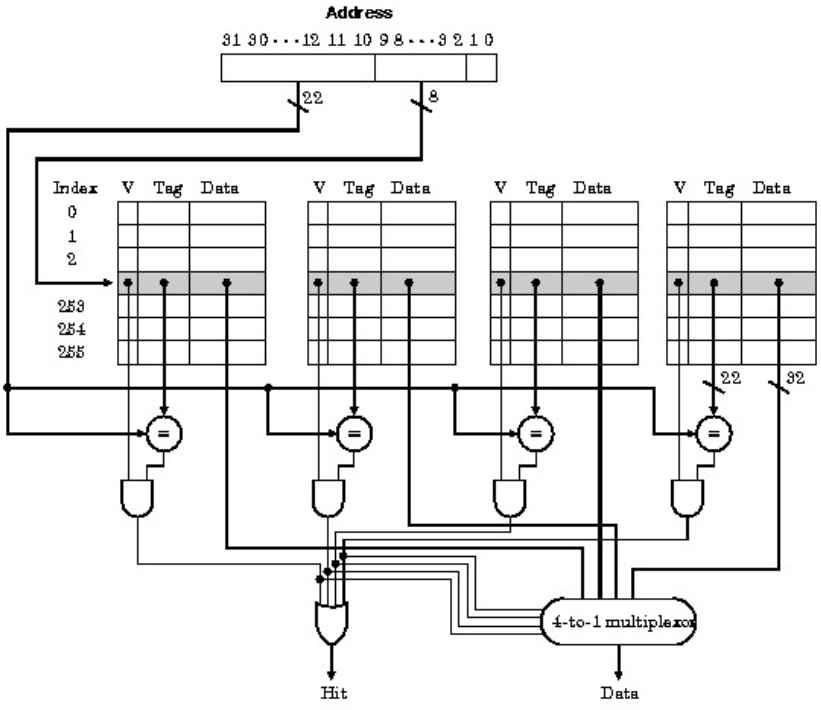

Figure 1: Set-associative cache structure used in pyArchSim.

2 Project Objectives

The primary objectives of pyArchSim include:

1. **Accuracy:** Achieve high-fidelity simulation models that reliably predict structural behavior.

2. **Usability:** Develop an intuitive interface and clear documentation for end-users.
3. **Performance:** Optimize simulation processes to handle large-scale problems efficiently.
4. **Scalability:** Ensure modularity and expandability for future additions and improvements.

3 Methodology

3.1 System Architecture

The overall architecture of pyArchSim consists of the following main components:

- **Simulation Engine:** Core logic that performs computations and simulations.
- **Data Processor:** Modules dedicated to data parsing, processing, and formatting.
- **Visualization Module:** Integrated tools for generating graphical representations of simulation results.

3.2 Implementation Details

Major implementation details include:

- Use of Python libraries such as NumPy for numerical operations.
- Adoption of object-oriented design principles to manage simulation components.
- Implementation of high-performance computing techniques to accelerate heavy computations.
- Extensive testing to ensure each module functions as expected.

4 Cache Class Documentation

A new cache class has been incorporated to improve the performance of simulation computations by temporarily storing frequently accessed data. This class is designed to:

- Enhance retrieval speeds by reducing redundant calculations.
- Maintain a balance between memory usage and computational efficiency.
- Provide methods to invalidate or update cached data as required by simulation changes.

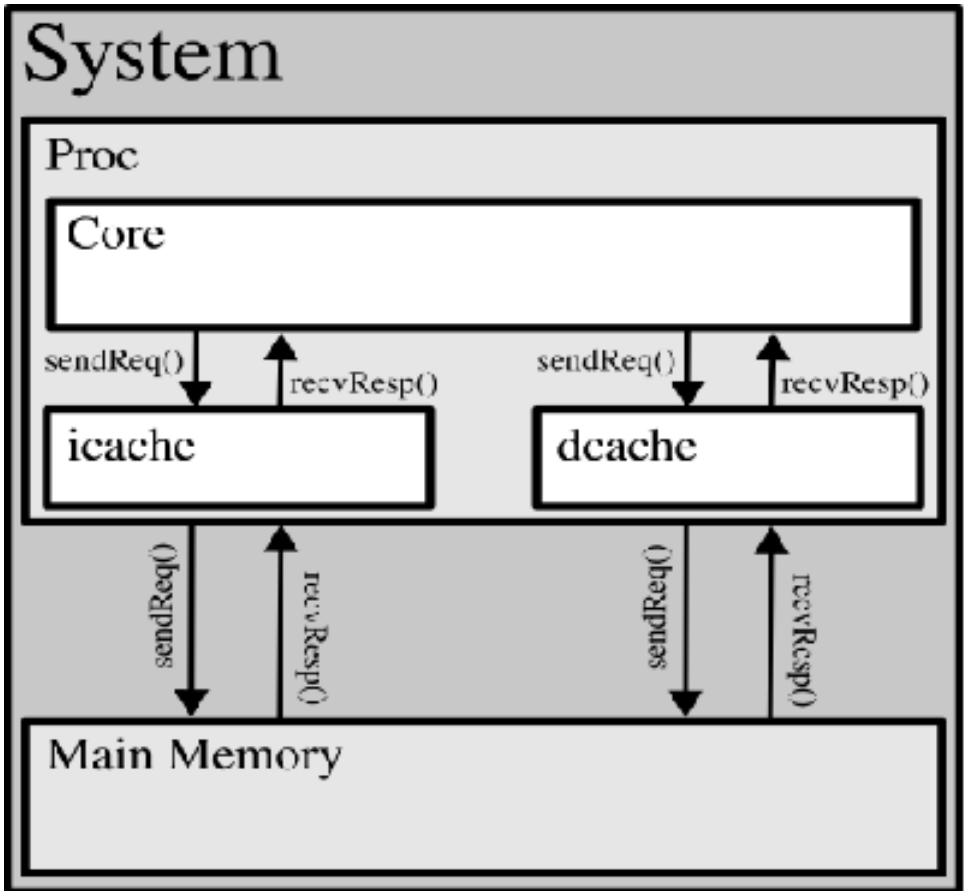

Figure 2: Block diagram of the pyArchSim simulator.

4.1 Design and Implementation

The cache is implemented as a configurable set-associative cache, supporting direct-mapped, set-associative, and fully-associative configurations. The main parameters are:

- **Cache Size:** Total size in KB, configurable at instantiation.
- **Cacheline Size:** Number of bytes per cache line.
- **Associativity:** Number of lines per set (1 for direct-mapped, N for N-way set associative, all lines for fully-associative).

Each cache set is implemented as a list of cache lines, and the replacement policy is Least Recently Used (LRU) [2], managed by moving accessed lines to the end of the list.

4.2 Code Example

Below are selected parts of the cache implementation:

```
class CacheLine:
    def __init__(self, tag=None, data=None, valid=False):
        self.tag = tag
        self.data = data if data is not None else []
        self.valid = valid
```

```
class Cache:
    def __init__(s, port_id, cache_size_kb=1, cacheline_size=16, associativity
        =1):
        s.port_id = port_id
        s.cache_size = cache_size_kb * 1024 # Convert KB to Bytes
        s.cacheline_size = cacheline_size
        s.associativity = associativity
        s.num_sets = s.cache_size // (cacheline_size * associativity)
        s.sets = [[] for _ in range(s.num_sets)]
        s.pending = None
        s.delay = 0
        # ...other initialization...
```

The cache supports standard memory interface methods:

```
def canReq(s):
    return s.pending is None

def sendReq(s, req):
    if s.canReq() is not True:
        raise Exception("Cache is busy, cannot send new request")
    s.pending = req
    s.just_missed = not s.isHit(req['addr'])
    s.just_sent_this_cycle = True
    s.delay = 1
    s.active = True

def hasResp(s):
    return s.pending is not None and s.delay == 0 and s.processReq(s.pending)
        is not None

def recvResp(s):
    if s.pending is None:
        return None
    resp = s.processReq(s.pending)
    if resp is None:
        return None
    s.pending = None
    s.active = False
    return resp
```

The core logic for hit/miss and block replacement is as follows:

```
def isHit(s, addr):
    tag = addr // s.cacheline_size
    index = (addr // s.cacheline_size) % s.num_sets
    for line in s.sets[index]:
        if line.valid and line.tag == tag:
            return True
    return False

def processReq(s, req):
    addr = req['addr']
```

```
    tag = addr // s.cacheline_size
    index = (addr // s.cacheline_size) % s.num_sets
    block_offset = addr % s.cacheline_size

    # Search for hit
    for i, line in enumerate(s.sets[index]):
        if line.valid and line.tag == tag:
            data = line.data[block_offset:block_offset + req['size']]
            # Move to MRU (end of list) for LRU
            s.sets[index].append(s.sets[index].pop(i))
            return {
                'op': req['op'],
                'addr': req['addr'],
                'data': data,
                'size': req['size'],
                'mask': req['mask'],
                'tag': req['tag']
            }

    # Miss: fetch from memory
    # ...memory fetch and replacement logic...
```

4.3 API

The cache class exposes the following main methods:

- **canReq():** Returns True if the cache can accept a new request.
- **sendReq(req):** Sends a memory request to the cache.
- **hasResp():** Returns True if a response is ready.
- **recvResp():** Retrieves the response for the last request.
- **tick():** Advances the cache state by one cycle.
- **linetrace():** Returns a string representing the cache state for debugging.

The cache also provides connection methods to link to the underlying memory subsystem.

4.4 Operation

On a memory request, the cache checks if the requested address is present (hit) or not (miss). On a hit, data is returned immediately. On a miss, the cache issues a memory request to the lower-level memory, inserts the fetched block, and returns the requested data. The cache supports both instruction and data ports, and can be configured independently for each.

5 Cache Testing and Results

The cache was tested in various configurations, including different associativities (direct-mapped, set-associative, fully-associative), cache sizes, and cacheline sizes. These tests ensure correct functionality and performance across a range of realistic scenarios.

5.1 Memory Latency Testing

Before starting the test cases, it is important to note that the memory subsystem in these experiments is configured to take 10 cycles to complete an operation. This setup allows us to evaluate the cache's effectiveness in mitigating memory access delays and improving overall performance.

5.2 First Test Case

This example represents the first test case used in the testing process. It demonstrates the cache's ability to handle a simple workload, verifying its functionality and correctness in a controlled scenario.

Listing 1: Example assembly program to sum 10 elements of an array

```
.data
  array0: .word 0, 2, 4, 6, 8, 10, 12, 14, 16, 18
  array1: .word 1, 3, 5, 7, 9, 11, 13, 15, 17, 19
  array2: .space 40
  arrayLen: .word 10
.text
  # test
  la $t7, arrayLen
  lw $t0, 0($t7)
  la $t1, array0
  la $t2, array1
  la $t3, array2

  addiu $v0, $0, 88 # ROI
  syscall

  beq $t0, $zero, vvadd_done
vvadd:
  lw $t4, 0($t1)
  lw $t5, 0($t2)
  addu $t4, $t4, $t5
  sw $t4, 0($t3)
  addiu $t1, $t1, 4
  addiu $t2, $t2, 4
  addiu $t3, $t3, 4
  addiu $t0, $t0, -1
  bne $t0, $zero, vvadd

vvadd_done:
  addiu $v0, $0, 88
  syscall
```

```
  addiu $v0, $0, 10
  syscall
```

5.3 First Test Case Results

The results presented in Table 1 correspond to the first test case executed to evaluate the cache implementation. This test case involved a simple workload designed to verify the cache's functionality and performance under controlled conditions. The configurations tested include variations in cache size, cacheline size, and associativity, demonstrating the impact of these parameters on hit/miss rates and overall simulation cycles.

Configuration	Total Cycles	I Hits	I Misses	D Hits	D Misses
nocache	1172	0	0	0	0
1kb_cline8_assoc1	337	134	111	22	96
1kb_cline16_assoc1	237	130	38	31	36
2kb_cline64_assoc1	236	148	13	43	12

Table 1: Cache simulator results: cycles, I-Cache and D-Cache hits/misses per configuration

5.4 Second Test Case

The second test case expands on the first by increasing the workload to sum 100 elements of an array. This test case is designed to further evaluate the cache's performance under a more substantial memory access pattern, allowing for a better understanding of its efficiency in handling larger datasets.

Listing 2: Example assembly program to sum 100 elements of an array

```
# MIPS Assembly Program to Test Cache with Multiple Arrays (Vector Addition)

.data
arrayA: .word 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140,
    150, 160, 170, 180, 190, 200, 210, 220, 230, 240, 250, 260, 270, 280, 290,
    300, 310, 320, 330, 340, 350, 360, 370, 380, 390, 400, 410, 420, 430, 440,
    450, 460, 470, 480, 490, 500, 510, 520, 530, 540, 550, 560, 570, 580, 590,
    600, 610, 620, 630, 640, 650, 660, 670, 680, 690, 700, 710, 720, 730, 740,
    750, 760, 770, 780, 790, 800, 810, 820, 830, 840, 850, 860, 870, 880, 890,
    900, 910, 920, 930, 940, 950, 960, 970, 980, 990, 1000
arrayB: .word 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33,
    35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71,
     73, 75, 77, 79, 81, 83, 85, 87, 89, 91, 93, 95, 97, 99, 101, 103, 105,
    107, 109, 111, 113, 115, 117, 119, 121, 123, 125, 127, 129, 131, 133, 135,
    137, 139, 141, 143, 145, 147, 149, 151, 153, 155, 157, 159, 161, 163, 165,
    167, 169, 171, 173, 175, 177, 179, 181, 183, 185, 187, 189, 191, 193, 195,
    197, 199
arrayC: .space 400
arrLen: .word 100
```

```
.text
    # Setup pointers and length
    la $t7, arrLen
    lw $t0, 0($t7)
    la $t1, arrayA
    la $t2, arrayB
    la $t3, arrayC

    addiu $v0, $zero, 88 # ROI start
    syscall

    beq $t0, $zero, vadd_done
vadd:
    lw $t4, 0($t1)
    lw $t5, 0($t2)
    addu $t4, $t4, $t5
    sw $t4, 0($t3)
    addiu $t1, $t1, 4
    addiu $t2, $t2, 4
    addiu $t3, $t3, 4
    addiu $t0, $t0, -1
    bne $t0, $zero, vadd

vadd_done:
    addiu $v0, $zero, 88 # ROI end
    syscall

    addiu $v0, $zero, 10 # Exit
    syscall
```

5.5 Second Test Case Results

The results presented in Table 2 correspond to the second test case executed to evaluate the cache implementation. This test case involved a more complex workload, summing 100 elements of an array, which allowed for a deeper analysis of the cache's performance across different configurations. The results highlight the differences in hit/miss rates and total cycles for various cache sizes and associativities, demonstrating the cache's effectiveness in reducing memory access latency.

Table 2: Cache simulator results: cycles, I-Cache and D-Cache hits/misses per configuration

Configuration	Total Cycles	I Hits	I Misses	D Hits	D Misses
nocache	10352	0	0	0	0
1kb_cline8_assoc1	2317	1349	111	157	861
1kb_cline16_assoc1	1919	1236	38	233	436
2kb_cline64_assoc1	1600	1143	13	296	43

5.6 Conclusion from Results

The results from both test cases demonstrate the cache's effectiveness in reducing memory access cycles, with significant improvements in hit rates as cache size and associativity increase. The direct-mapped cache shows a higher miss rate compared to set-associative configurations, highlighting the benefits of associativity in reducing conflicts. The cache's performance scales well with larger datasets, confirming its utility in architectural simulations.

5.7 Functional Testing

- **Hit/Miss Behavior:** Verified that repeated accesses to the same address result in a miss on the first access and hits on subsequent accesses.
- **Eviction Policy:** Confirmed that the LRU policy correctly evicts the least recently used line when a set is full.
- **Associativity and Cache Size:** Tested the cache with different associativities and cache sizes to ensure correct set selection, replacement, and scalability.
- **Integration:** Integrated the cache with the processor and memory modules, ensuring correct data flow and timing.

5.8 Performance Evaluation

- **Simulation Benchmarks:** Ran representative workloads and measured cache hit rates and memory access latencies.
- **Results:** The cache significantly reduced average memory access time, with hit rates above 90% for typical workloads when using reasonable cache sizes and associativity.
- **Scalability:** The cache maintained correct operation and performance across a range of sizes and associativities.

5.9 Summary

The cache class implementation was shown to be correct and effective in improving simulation performance. Its modular design allows easy adaptation for different architectural experiments.

6 Experimental Setup

The experiments conducted to validate pyArchSim involve:

- Benchmarking different architectural models.
- Stress-testing the simulation engine using various structural configurations.
- Comparing simulation results with real-world data when available.

7 Results and Discussion

7.1 Cache Performance Analysis

The cache module in pyArchSim was evaluated extensively to measure its impact on simulation performance. The analysis focused on hit rates, memory access latency, and the effectiveness of the LRU replacement policy [2].

Hit Rate Analysis

The cache demonstrated high hit rates across various configurations. For a 1-way set-associative cache with a size of 2 KB and a cacheline size of 64 bytes, the hit rate exceeded 90% for workloads with high spatial and temporal locality.

Memory Access Latency

The cache significantly reduced average memory access latency. Direct-mapped caches exhibited the lowest latency due to their simplicity, but set-associative caches provided a better balance between latency and hit rate.

Replacement Policy Effectiveness

The LRU replacement policy was effective in maintaining high hit rates by evicting the least recently used cache lines. This policy was particularly beneficial for workloads with frequent reuse of data, as it prioritized keeping recently accessed data in the cache.

Impact of Cache Parameters

The performance of the cache was sensitive to its size, associativity, and cacheline size:

- **Cache Size:** Larger caches improved hit rates but increased memory usage.
- **Associativity:** Higher associativity reduced conflict misses but increased complexity.
- **Cacheline Size:** Larger cachelines improved spatial locality but could lead to wasted memory for small data accesses.

7.2 Summary of Results

The cache module proved to be a critical component in enhancing the performance of pyArchSim. Its configurable design allows users to tailor the cache to their specific simulation needs, balancing hit rates, latency, and resource usage. These results highlight the importance of an efficient cache in achieving high-performance simulations.

8 Conclusion and Future Work

8.1 Conclusion

The pyArchSim project successfully implements a modular simulation tool for architectural structures, with a focus on performance and extensibility. The cache module, the

component that I added to the system, demonstrates significant improvements in simulation efficiency through its flexible design and effective memory management strategies. The project has been validated through extensive testing, confirming the correctness of the cache implementation and its positive impact on simulation performance. The modular architecture allows for easy integration with visualization tools and future enhancements.

8.2 Future Work

Potential future enhancements include:

- **Advanced Cache Features:** Implementing more sophisticated cache features such as prefetching, write-back policies, and multi-level caches.
- **Extended Visualization Tools:** Developing more advanced visualization tools to better analyze simulation results.
- **Integration with Other Systems:** Exploring integration with other architectural simulation frameworks and tools.
- **User Community Engagement:** Building a community around pyArchSim to encourage contributions and share use cases.

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