Cairo University

Institute of Statistical Studies and Research
Department of Computer and Information Sciences
Digital Logic –CS504
January 2014
Time permitted: Three Hours

Question # 1: (10 points)

Use 12 bits to solve the following problems:

A) Convert the decimal numbers ***+161*** and ***-238*** to binary using the signed ***Two's complement*** representation.

B) Express $527)_{10}$ in (i) ***8421 BCD*** (ii) ***Excess-3*** and (iii) ***2421 BCD***

C) Express the octal number $3545)_8$ in (i) ***Two's Complement Binary*** (ii) ***5421 BCD*** and (iii) ***Unsigned Integer***

D) Express the ***Excess-3*** binary number ***011100110100*** in (i) ***5421 BCD*** (ii) ***Decimal digits*** and (iii) ***octal digits***

Question # 2 (12 points)

A) Minimize the following logical expressions by algebraic manipulations

i. $F(A, B, C) = A'+ABC + A(B \text{ xor })+AB'C'$
ii. $G(A, B,C,D) = (AD+ A'C)(B'(C+BD'))$

B) Draw the schematics for the following functions using **NOR gates and inverters only**.

i. $F1= X(X+Y)$
ii. $F2= (X'+Y')(X'+Z')$
iii. $F3= (X+Y)(X'+Y')$

Question #3 (12 points)

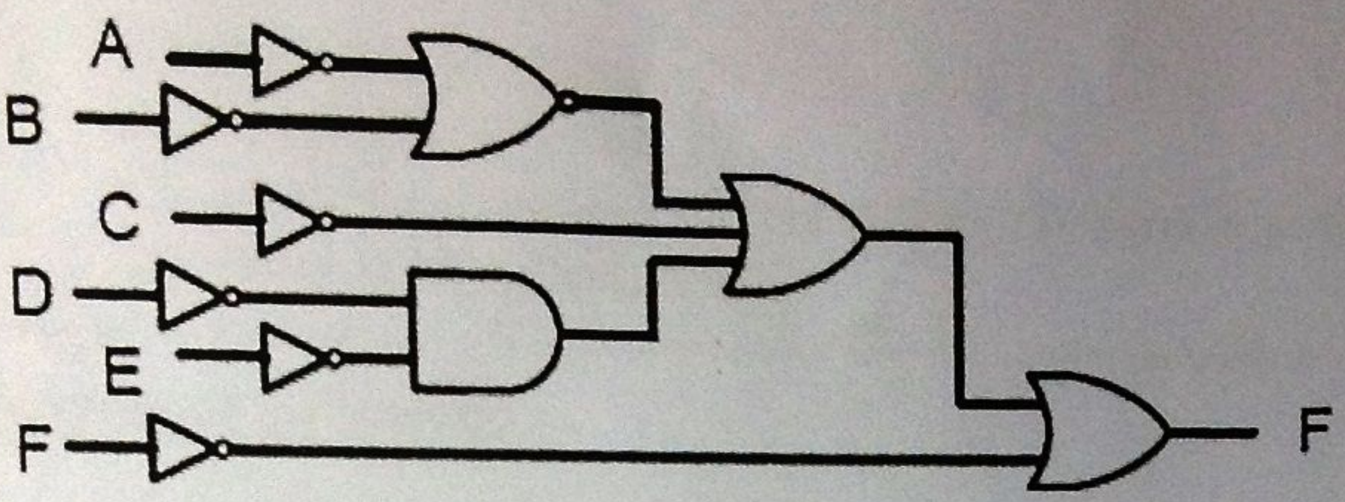
Given The Following Functons:

i- $G(a, b, c, d)= a'b'c'd'+ a'b'c'd + a'b'cd'+ a'b'cd+ ab'c'd'+ ab'cd'$
ii- $H(A, B, C, D) = \Sigma M(1, 3, 8 ,11, 12,14) + \Sigma D(0, 2, 6, 9,10,13,15)$

A) Use ***K-map*** to simplify them in sum of products (***SOP***) form.
B) Implement ***G*** with the minimum number of ***NAND*** gates.
C) Use ***K-map*** to simplify them in product of sums (***POS***) form.
D) Implement ***H*** with the minimum number of ***NOR*** gates

Question #4(6 points)

Redraw the following circuit by using only ***NAND*** gates.
Note: Use only uncomplmented literals ***A, B,…, F*** as inputs and **do not use the complemented signals *A', B',..., F'***



Question #5(10 points)

Design a ***code converter*** that converts a decimal digit from **2421** code to **8, 4, -2, -1** code.
Hint: $1)_{10} = 0001)_{2421} = 0111)_{84\text{-}2\text{-}1}$ code

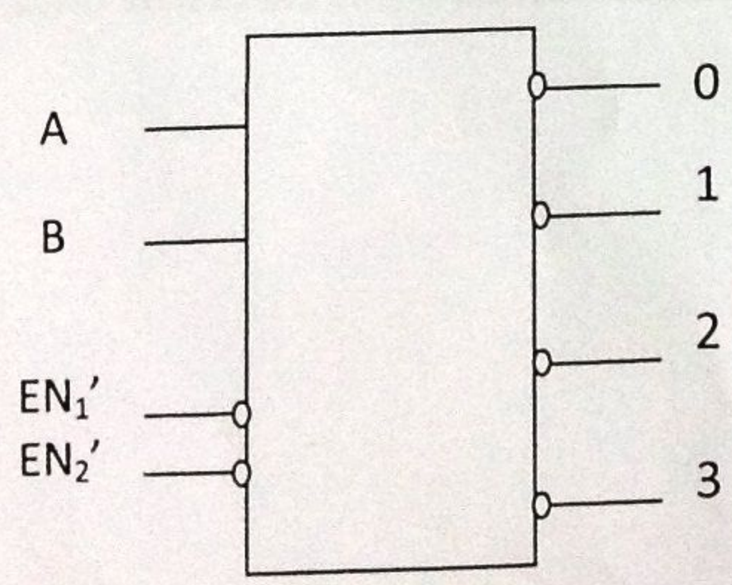
A) Build the ***truth table*** for the converter
B) ***Minimize*** the functions generated by the truth table using ***k_map***

Question #6 (12 points)

Consider the following two functions:

i- F(a, b, c, d)= a'c +cd +b'd'+a'bd+ac'd'
ii- G(a, b, c, d)= ad' +a'b +cd

A) Implement them using ***ROM*** gate arrays, be sure to label the inputs and the outputs.
B) Given the shown decoder, with active low outputs and two active low enables, implement the given functions. Use ***two NAND*** gates and ***at most four*** of the shown decoder.



EN_1'	EN_2'	A	B	0	1	2	3
0	X	X	X	1	1	1	1
X	0	X	X	1	1	1	1
0	0	0	0	0	1	1	1
0	0	0	1	1	0	1	1
0	0	1	0	1	1	0	1
0	0	1	1	1	1	1	0

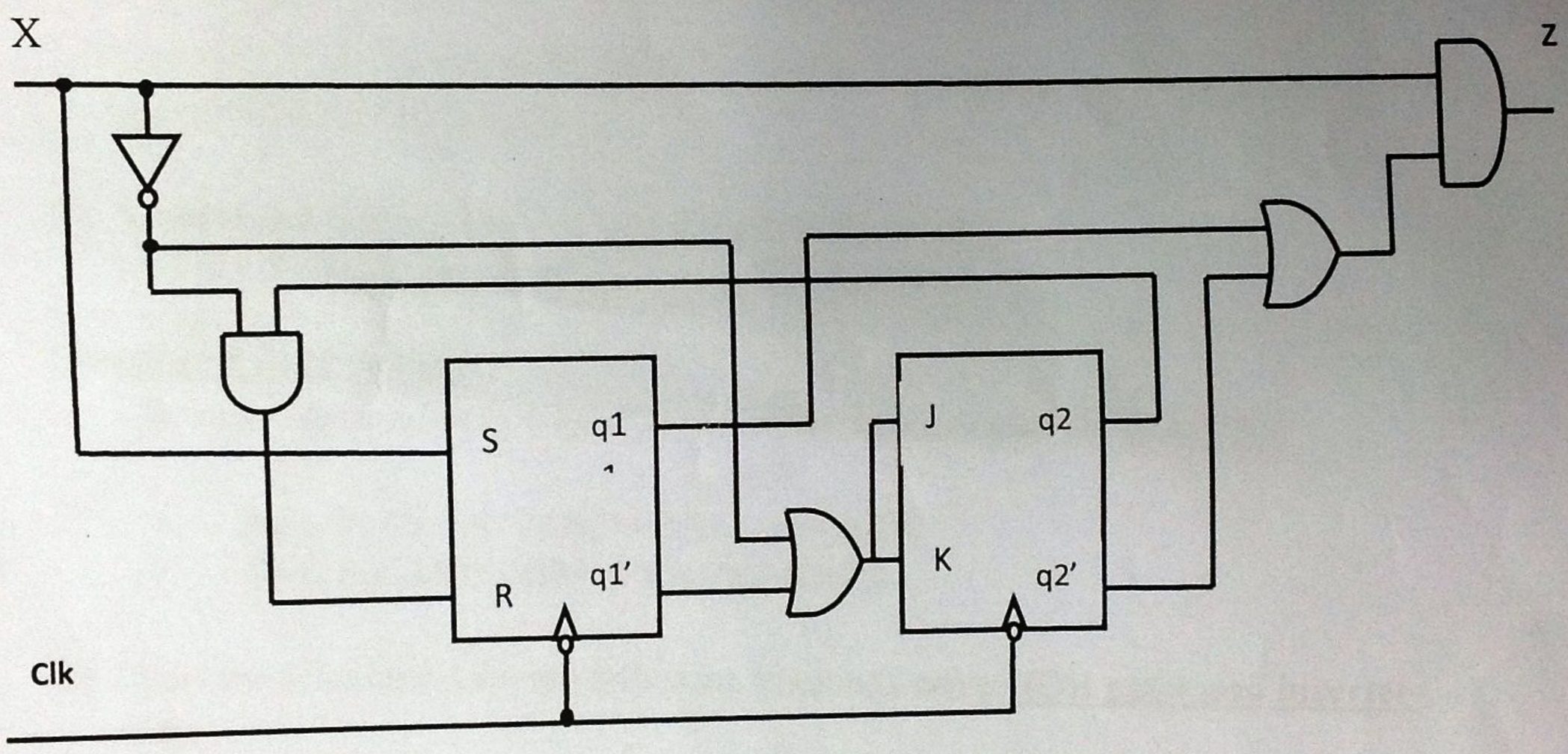
***Question 7*: (8 points)**

A system that has two inputs ($x, y \in \{a,b\}$) and one output ($z \in \{0, 1\}$). The output z is one when x is equals to y for ***at least three consecutive clock cycles***, and is zero, otherwise.

A) Describe the system.
B) State the system Model.
C) Show the transition and the output functions in a state table.
D) Draw the state diagram.

Question #8 (10 points)

Given the following sequential circuit:



A) State the design model
B) Build the state table
C) Draw the state diagram of the sequential system

☺ *Best of LUCK* ☺