Cairo University

Institute of Statistical Studies and Research
Department of Computer and Information Sciences
Digital Logic CS504
June 2012
Time permitted: Three Hours

nswer the following questions: ***Clarify*** *your answer,* ***start*** *each problem in a new page.*
abel your signal lines in each and every ***Design and Table.***

uestion 1: (9 points)

a) Using the version of Hamming code shown, Code the data " *1001*"

a1= a3 ⊕ a5 ⊕ a7
a2= a3 ⊕ a6 ⊕ a7
a4= a5 ⊕ a6 ⊕ a7

b) If the word "*1101101*", was received after being coded with Hamming code, what word was sent (assuming single error).

c) Given the two binary numbers *10010101* and *01110011*,
Show the decimal equivalent of each of the numbers if they are interpreted as:
(i) BCD Exsess3 (ii) BCD 8421
(iv) Signed number (v) Unsigned number

uestion 2: (9 points)

a) Show the Truth Table for a system that has four inputs, *a, b, c* and *d*, and two outputs, *f* and *g*. The first two inputs (*a, b*) represent one binary number (in the range 0 to 3) and the last two (*c, d*) represent another number in the range 1 to 3. The output, *f and g* represent the magnitude of the difference of the two binary numbers inputs (|ab –cd|).

b) Reduce the following expression to a minimum Sum of products, **show** each algebraic step.

$$F(w, x, y, z)= x'z' +x'yz' + xy'z+ xyz+wx'z$$

c) Manipulate the following to sum of product expression

$$F=(b'+c)(a'+c+d')(c'+d)(a+c'+d')$$

estion 3: (9 points)

a) Given the function, *F*, written in the following page, show a block diagram for the implementation of the function using, only, ***two-input NAND*** gates (any number of them). Assume all variables are available, both complemented and uncomplemented.

$$F= abc+ ac'd'e' + a'd'e + ce +cd$$

(helping note: Manipulate the expression to obtain terms containing two literals or less , then draw schematic of the function).

b) Find all minimum Sum of products expressions for the following functions (use K-Map): (three solutions)

$$G(a, b, c, d, e)= \Sigma m(0, 3,5,7, 12,13,14, 15,19,20,21,22,23,25,26,29,30)$$

Question 4: (12 points)

Consider the following three function:

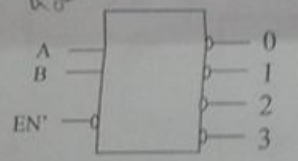
$$F= \Sigma m(1, 2, 3, 5, 6, 7, 8, 10, 11, 15)$$

$$G= \Sigma m(3, 4, 6, 8, 12, 14, 15)$$

$$H= \Sigma m(1, 3, 4, 5, 6, 7, 8,15)$$

a) Implement them using ROM gate arrays, be sure to label the inputs and the outputs.

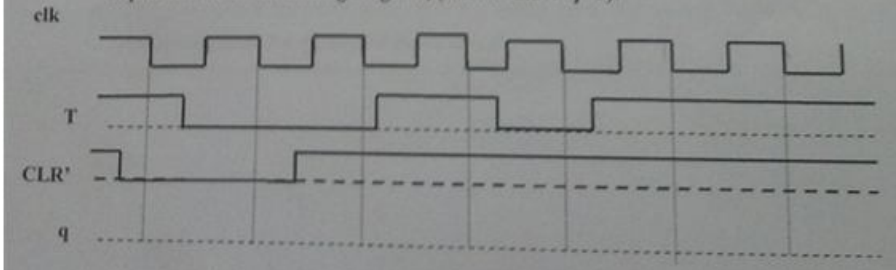
b) Given the shown decoder, with active low outputs, active low enable, implement the given functions. Use three ***NAND*** gates and at most five of the shown decoder.
Extra 5 points credit : Show a diagram that uses, only, three eight-input ***NAND*** gates and four of this decoder.



EN'	A	B	0	1	2	3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Question 5: (9 points)

a) Given a *T* flip flop with an active low clear (CLR'). Show the Flip Flop output for the input shown in the timing diagram, (initial value: *q=1*).



b) We have a new type of a Filp Flop, with inputs A and B, if $A=0$ then $Q^* = QB$. If $A=1$ then $Q^* = Q'B'$.

I. Show a state diagram for this Flip Flop
II. Write an equation for Q^* in terms of A, B and Q.

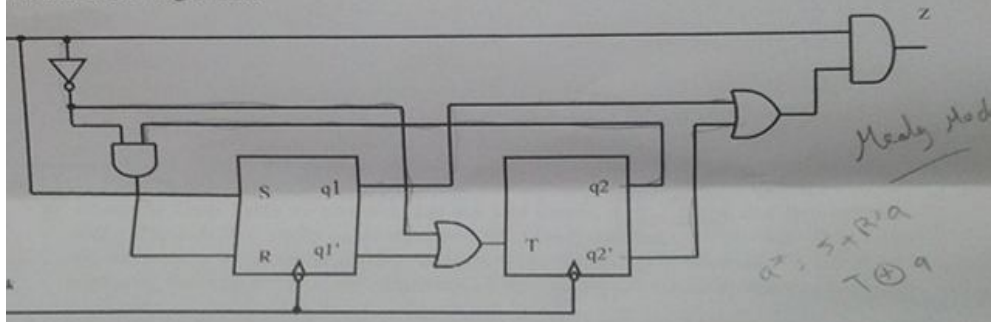
Question 6: (10 points)

A system that has two inputs ($x, y \in \{a,b\}$) and one output ($z \in \{0, 1\}$). The output z is one when x equals to y for at least three consecutive clock cycles, and is zero, otherwise.

a- Describe the system
b- State the system Model
c- Show the transition and the output functions in a state table
d- Draw the state diagram

Question 7: (12 points)

Given the following circuit:



a) State the design model
b) Build the state table
c) Given the initial state (*00*) and following values for x: 00*1100110*, build the time Trace (behavior) table for q_1, q_2 and the output z.

☺ *Best of LUCK* ☺