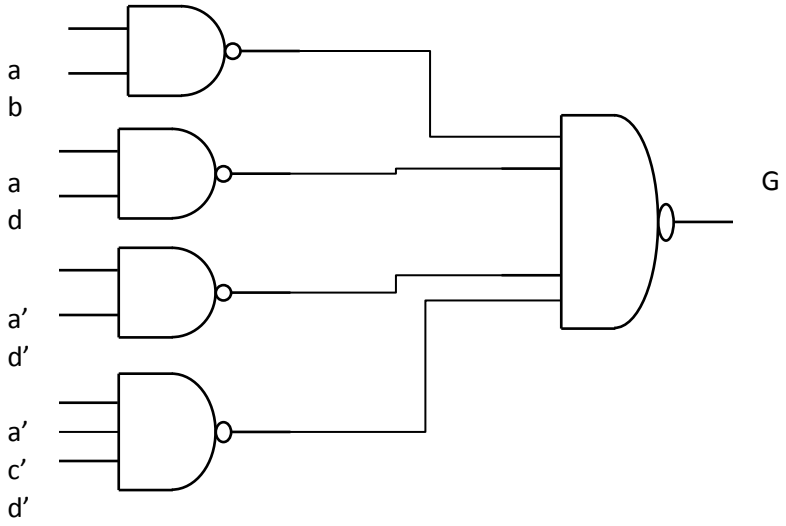
Quiz #3

Q**1.** Assume all input are available both uncomplemented and complemented, show a two-level implementation of:

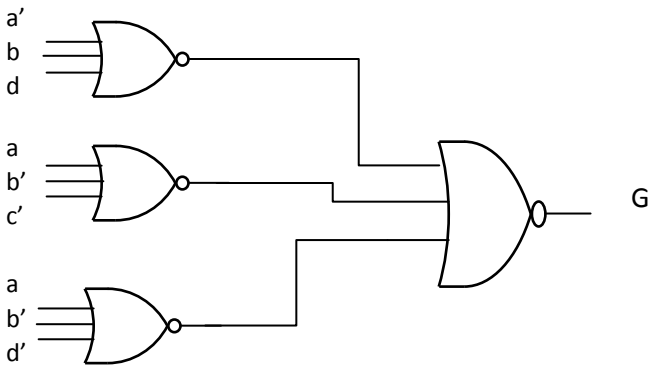
$$G(a,b,c,d) = ab + ad + a'b' + a'c'd' = (a'+b+d)(a+b'+c')(a+b'+d')$$

a- Using Nand gates of any size



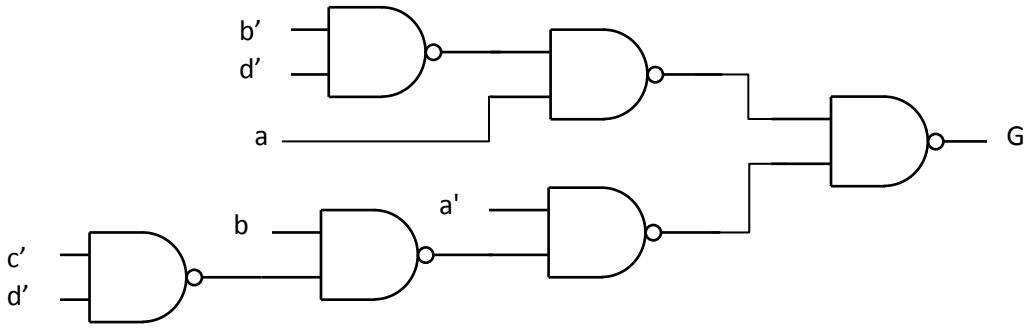
b- Using nor gates of any size

$$G = (a'+b+d)(a+b'+c')(a+b'+d')$$



c- Using tow-input NAND gates (none of which may be used as a NOT)

g= ab + ad+ a'b' + a'c'd'= a(b+d) + a'(b'+c'd')



Q2. Given the following truth table

x	*y*	*z*	*F*
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*1*
0	*1*	*1*	*0*
1	*0*	*0*	*1*
1	*0*	*1*	*0*
1	*1*	*0*	*1*
1	*1*	*1*	*1*

a- Write the sum of minterm function in numeric form

F = Σm(1,2,4,6,7)

b- Write the sum of minterm function in Algbraic form

F = x'y'z + x'yz'+xy'z'+xyz'+xyz

c- Find the minimum sum of products expression

F = x'y'z + x'yz'+xy'z'+xyz'+xyz = x'y'z+ x'yz'+xyz +xz'(y'+y)

= x'y'z + yx'z'+ xyz + xz'= x(z'+yz) + z'(x+yx') + x'y'z = xz' +xy +xz'+yz' + x'y'z

= xz' +xy + yz' + x'y'z

d- Find the minimum product of sum expression

F= = xz' +xy + yz' + x'y'z= z'(x+y)+x'y'z + xy

= (z'+x'y')(z+x+y) + xy = (xy+(z'+x'y'))(xy+(z+x+y))= ((x+y')(x'+y)+z')(z+x+y))=

= (x+y'+z')(x'+y+z')(z+x+y)

Q3. Given the following sequence of 6 state: *4 7 2 0 3 1*

a) Design a counter to generate the sequence using *T Flip Flop*.

b) Show the state diagram indicating what happens if it, initially, is in one of the unused states.

c) Propose a solution for the problems caused by the unused states.

d) Design the solution you proposed in 'c'

Sol

a)

Q2	*Q1*	*Q0*	*Q2**	*Q1**	*Q0**	*T2*	*T1*	*T0*
0	0	0	0	1	1	0	1	1
0	0	1	1	0	0	1	0	1
0	1	0	0	0	0	0	1	0
0	1	1	0	0	1	0	1	0
1	0	0	1	1	1	0	1	1
1	0	1	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X
1	1	1	0	1	0	1	0	1

T0=ΣM(0,1,4,7) + ΣD(5,6)
T1=ΣM(0,2,3,4) + ΣD(5,6)
T2=ΣM(1,7) + ΣD(5,6)

	00	*01*	*11*	*10*
0	*1*		*x*	*1*
1	*1*		*1*	*x*

T0=Q2+Q1'
T1=ΣM(0,2,3,4) + ΣD(5,6)

	00	*01*	*11*	*10*
0	*1*	*1*	*x*	*1*
1		*1*		*x*

T1=Q0'+Q2'Q1

T2=ΣM(1,7) + ΣD(5,6)

	00	*01*	*11*	*10*
0			*x*	
1	*1*		*1*	*x*

T2= Q1Q2/q2q0+Q1'Q0

T0=Q2+Q1'
T1=Q0'+Q2'Q1
T2= Q1Q2/q2q0+Q1'Q0

	T2	T1	T0	
101	1/1	0	1	000/000 used states
110	1/0	1	1	001/101 USED 1, unused 5

b) State Diagram

4 7 2 0 3 1

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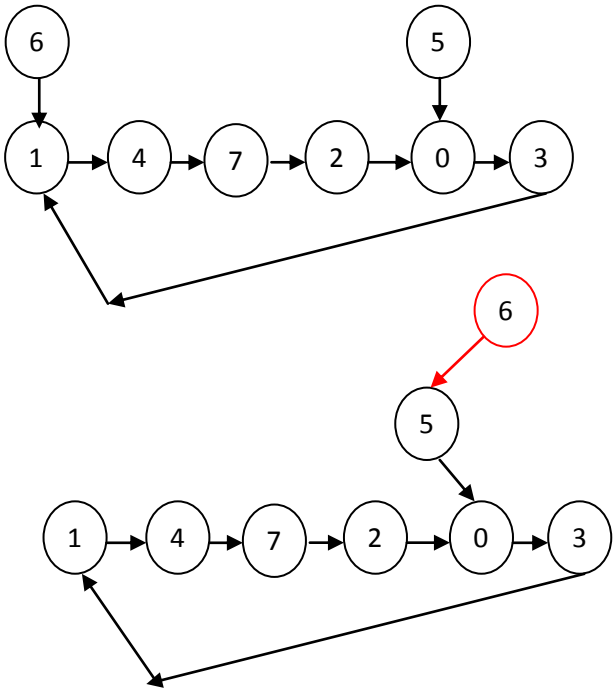

c) THE FIRST SOLUTION IS A SELF STATED DESIGN SOLUTION
OR IF YOU HAVE TO USE THE SECOND SOLUTION THEN YOU must REDESIGN IT.
It SHOULD BE REDESIGNED WITH THE STATE '110' AS A USED STATE

d) design for the same sequence with state '110'→ '001'

Q2	Q1	Q0	Q2*	Q1*	Q0*	T2	T1	T0
0	0	0	0	1	1	0	1	1
0	0	1	1	0	0	1	0	1
0	1	0	0	0	0	0	1	0
0	1	1	0	0	1	0	1	0
1	0	0	1	1	1	0	1	1
1	0	1	x	x	x	x	x	x
1	1	0	0	0	1	1	1	1
1	1	1	0	1	0	1	0	1

T0=ΣM(0,1,4,6,7) + ΣD(5)
T1=ΣM(0,2,3,4,6) + ΣD(5)
T2=ΣM(1,6,7) + ΣD(5)

T0

	00	01	11	10
0	1		1	1
1	1		1	x

T0=Q2+Q1'

T1

	00	01	11	10
0	1	1	1	1
1		1		x

T1=Q0'+Q2'Q1

T2

	00	01	11	10
0			1	
1	1		1	x

T2= Q1Q2+Q1'Q0
T0=Q2+Q1'
T1=Q0'+Q2'Q1
T2= Q1Q2+Q1'Q0
Check self starting

	T2	T1	T0	
101	1	0	1	000 USED 0

The state diagram