Cairo University
Institute of Statistical Studies and Research
Computer and Information Sciences Department

CS 504 ***Digital Logic and Computer Organization***

Final Exam ***5-1-2008***

Answer the Following Questions *[70 Marks]*

Question 1 **[4 marks]**

Consider the following two functions:

$F(X,Y,Z) = XY + Z$, $G(X,Y,Z) = Y Z' + X' Z$

Draw a single logic diagram for both functions using only one (3–to–8) decoder and any gates as needed?

Question 2 **[4 marks]**

Design the full subtractor circuit using multiplexer(s) and any gates as needed? The circuit has three inputs X, Y, Z and two outputs B (output borrow) and D (Difference).

Question 3 **[4 marks]**

Draw a logic unit that perform four different logic operations using a multiplexer and any gates as needed?

Question 4 **[6 marks]**

Design the serial adder using two shift registers, a D-type flip flop and any gates as needed? Show all your work.

Question 5 **[6 marks]**

Design a 3-bit binary counter using T flip flop?

Question 6 **[6 marks]**

Design a single circuit for the (3–bit) odd parity generator and checker? Use the appropriate gates and explain how the circuit works?

Question 7 **[6 marks]**

Design a (4-to-2) priority encoder with inputs D0, D1, D2, and D3. Assume that D0 has the lowest priority and D3 has the highest priority?

Question 8 **[4 marks]**

Find the essential and non essential prime implicants then simplify the following function:

$F(A, B, C, D) = \sum m(2,8,9,10,12,13,14), \sum d(1,3,4,5,6,7)$

Question 9 **[4 marks]**

Draw the logic diagram of a 4-bit Universal Shift Register that operates as follows:

S_1	S_0	Operation
0	0	No Change
0	1	Shift right
1	0	Shift left
1	1	Parallel Load

Question 10

[10 marks]

An industrial robot that places components on a printed circuit board has **3 fail – safe sensors and an emergency shutdown switch**. The robot should keep functioning unless any of the following conditions arise:

- If the emergency switch is pressed , the system shuts down
- If sensor 1 and sensor 2 are activated at the same time, the system shuts down
- If sensor 2 and sensor 3 are activated at the same time, the system shuts down
- If all three sensors are activated at the same time then the system shuts down

a) Derive the truth table for this system?

b) Using K – map, obtain the minimal sum of product?

c) Design the circuit using NAND gates only?

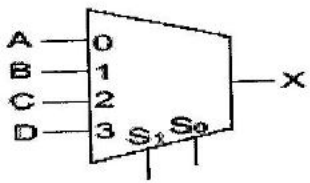
d) Design the circuit using NOR gates only?

e) If the time delay experienced by a NAND is 8 nanosecond and time delay experienced in a NOR is 5 nanosecond. Which implementation is faster? and by how much?

Question 11

[4 marks]

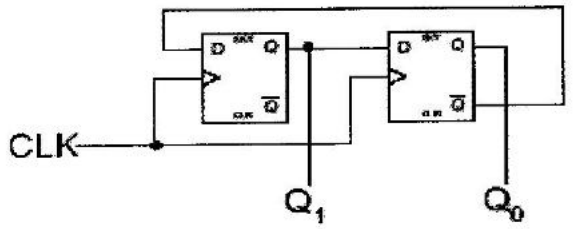
Consider the following multiplexer. What must the inputs A, B, C, D be so that the multiplexer implements the function X = S1 S0 ' ?



Question 12

[4 marks]

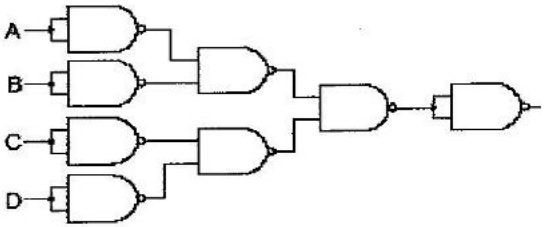
What sequence will the following counter count through?



Question 13

[4 marks]

Express output function of the following figure in the simplest form?



Question 14

[4 marks]

Assume that the circuit below has initially been reset. X is high and Y is low. After 4 clock pulses, What is the value of Q?