

# **Graphene Devices for Beyond-CMOS Heterogeneous Integration**

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# Abstract

Semiconductor manufacturing is the workhorse for a wide range of industries. It lies at the heart of consumer electronics, telecommunication equipment and medical devices. Most semiconductor electronics are made from Silicon, and are fabricated using CMOS technology. The versatility of semiconductor electronics stems from the ever-reducing cost of integrating more computing and memory functions on chip. The small cost for adding extra functions has been maintained in the past 50 years through transistor scaling. Transistor scaling focuses on shrinking the size of transistors integrated on chip. This reduction in transistor size, while keeping the overall cost of the chip fixed allowed us to reduce the cost per function with scaling, and is what is celebrated as Moore's law. Scaling has been working gracefully up to the last decade, where the exponential rise in manufacturing cost and diminishing gains of scaling on device performance reduce its economic benefit. To revive the cost reduction trend, different techniques were proposed such as augmenting CMOS manufacturing with new materials (Beyond CMOS), 3D integration, and integrating more non-transistor elements on-chip (More than Moore).

In this work, we focus on the efficient implementation of several circuit functions using an allotropy of carbon known as graphene. Graphene, a single layer of carbon atoms arranged in a hexagonal lattice, has unique electronic properties that has been taken the solid-state electronics community by a storm since its first experimental conception in 2004. Despite its promising electronic properties, namely the very high charge-carrier mobility and reduced scattering by impurities, graphene circuits has been held back by a plethora of nonidealities and technological roadblocks that hamper its use in traditional transistor-based circuits. In this work, we attempt to leverage the unique physical properties of graphene to implement non von-Neumann neuromorphic computing architectures, low-loss diodes and evaluate the behavior of diffusive-transport graphene couplers. We focus on the the design, fabrication and characterization of graphene devices in the presence of the current performance-limiting technological nonidealities in heterogeneous graphene-CMOS systems. We present the design, fabrication and characterization of all-graphene resistive data converters devices and diodes, discussing their

performance and application as building elements of all-graphene brain-inspired computing architectures. We evaluate the performance of graphene couplers operating in the diffusive transport regime, which serve as a method to analyze the cross-coupling between adjacent graphene interconnects. We also discuss the current technological limitations hampering the performance of graphene devices, and the roles of different processing non-idealities on the characteristics of graphene devices.



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# 1) Introduction

The semiconductor industry has evolved over the decades through aggressively shrinking the sizes of transistors and other integrated circuits building elements over the years. This allowed the reduction of cost per function, leading to the versatile use of electronic components and the rapid growth of the consumer electronics market.

In this chapter, we discuss the economics of scaling, and Moore's law, the driving force behind scaling and the growth of the consumer electronics industry. We then discuss beyond-CMOS techniques; a method used to fuel scaling economics despite the slowdown of Moore's law. We then introduce the advantages of graphene for use in beyond-CMOS systems and present an overview of this document.

## 1.1. Economics of Scaling and Moore's Law

Moore's law focused on reducing the cost per function on an integrated circuit to reduce the overall cost of electronic components[1]. As the cost for a fixed area of the chip was relatively constant, the most straightforward way of reducing the cost per function was to shrink the size of the elements used to implement it, and by using clever circuit techniques to reduce the required area and increase functionality. The shrinking in transistor size is known as scaling[2]. Scaling initially allowed the increase of device performance, as devices performed better as they were scaled down in size.

The cost of scaling started increasing in the last decade with the increase in manufacturing cost. In addition, scaling devices down started degrading their performance, causing the onset of variability and other short channel effects that reduced the technical yield of scaling[3]. This caused a slowdown in the scaling trend and disrupted the economics prospects of scaling.

To overcome the scaling slowdown, the industry identified the three techniques of continuing economic growth:

1. More Moore: More scaling according to Moore’s law and pushing for the continuous scaling down of devices.
2. More than Moore: Integrating more non-transistor components on chip allowing more functions to be integrated, which reduces the overall system cost and allows integrating more functions on chip[4].
3. Beyond-CMOS: Introducing new materials and devices to augment or replace the current CMOS technologies. This can be through the use of SiGe wafers, III-V semiconductors or other non-conventional materials[4]–[7].

In this work, we focus on the use of graphene as a beyond-CMOS material to augment CMOS circuits.

## 1.2. Beyond-CMOS Materials and Devices

Different beyond-CMOS materials and devices are active fields of research. RRAM, FeRAM, magnetic logic, and other devices have been proposed to augment or replace some of CMOS functions[6]–[18]. Different technologies target the replacement of their CMOS counterparts, as well as implementing novel functions and architectures for computation and memory.

The compatibility of beyond-CMOS devices with current CMOS infrastructure is a fundamental pillar in the conception of these devices. The CMOS infrastructure and economics prevents the rapid replacement of CMOS, and all beyond-CMOS technologies focus on augmenting CMOS.

## 1.3. Graphene as a Beyond-CMOS Material

Graphene’s 2D nature and inherent compatibility with CMOS make it an ideal choice for heterogeneous integration. The high charge carrier mobility and large surface-to-volume ratio make it suitable for the implementation of high-performance circuits and sensors[19]–[21]. However, current technological limitations and non-idealities limit the implementation of graphene circuits.

In this work, we focus on the use of graphene to implement non-transistor devices that implement circuit functions directly in function-in-a-device approach. We focus on the use of graphene for the implementation of neuromorphic computing architectures, low-loss diodes and discuss the limits of scaling graphene interconnects by studying graphene current couplers. We also discuss the current technological limitations that hamper the performance of graphene devices. We focus on the use of CVD graphene throughout this work because it is the most suitable for heterogeneous integration with CMOS.

## 1.4. Overview of Document

We begin by discussing the basic electronic properties of graphene in Chapter 2, outlining the basic electronic properties and the role the substrate and contacts play in affecting the behavior of graphene devices. We also discuss the charge transport in CVD graphene, which we used throughout this thesis, and methods to characterize graphene.

Chapter 3 presents an implementation of an all-graphene neuromorphic computing architecture. It focuses on the implementation of nearest-neighbor cellular neural networks using graphene. We discuss how to build the building blocks of the system (neurons and synapses) using graphene and present measurement results from prototype devices used to characterize graphene neurons.

Chapter 4 focuses on the implementation of low-loss, zero turn-on voltage, diodes using graphene. We begin with an overview of previously proposed low-loss graphene diodes, before proposing a new architecture that depends on the photon-like behavior of charge carriers in graphene for rectification. We present measurements from prototype devices used to assess the performance of the proposed diode structure, showing how it outperforms all previously published devices. We conclude with a discussion on the limitations of performance of the proposed architecture.

Chapter 5 focuses on the analysis of current couplers using graphene ribbons operating in the diffusive regime, and using it as a method to analyze the scaling limits of graphene interconnects.

We present a model for the diffusive transport coupler, discussing its performance and limitations before using it to assess the scaling limits of graphene interconnects.

Chapter 6 summarizes a number of technological limitations that limit the performance of graphene devices and circuits. We discuss the role of electrical and thermal contact resistance, the evolution of stress in dual-gated graphene devices and the impact of photoresist chemistry on graphene FET performance. We then discuss the effect of photoresist residuals on graphene performance.

Chapter 7 concludes this work, describing possible ways to alleviate the current technological limitations and proposing different ways graphene can be used in electronics.

We have 4 appendices at the end of this work. Appendix A details the nanofabrication processing parameters used throughout this work; Appendix B describes the steps used to fabricate a dual-gated graphene device; Appendix C outlines the measurement setup used when characterizing the prototype devices presented; and Appendix D gives a detailed derivation of the electrical model of a graphene current coupler operating in the diffusive regime.

## 2) The Electronic Properties of Graphene

In this chapter, we discuss the electronic properties of graphene integral to this work. We start with a description of graphene's band structure, elaborating its basic features. We then discuss the Klein tunneling in graphene, and how it differs from normal quantum mechanical tunneling and how it affects device performance. We then turn our discussion towards experimental aspects that affect graphene's performance, discussing how the presence of a substrate affects graphene. Next, we discuss the nature of charge transport in CVD graphene, followed by a discussion of how metal contacts dope graphene in their vicinity.

We then turn to the characterization methods of graphene, discussing the Raman analysis of graphene, which allows us to identify the number of layers and infer the information about the quality of the material. We then conclude with a description of the electrical model used to characterize and describe the devices presented in this work.

### 2.1. Electronic Band Structure of Graphene

Graphene's atoms lie in a hexagonal lattice with the atoms placed 1.42 Å apart [19], [22]. The hexagonal lattice corresponds to a two-atom unit cell in a triangular lattice as shown in Figure 2.1(a). The corresponding Brillouin zone is hexagonal, but the vertices of the hexagon are grouped into two distinct groups, K and K'. Each group contains the points that can be connected by integral multiples of the reciprocal lattice basis as shown in Figure 2.1(b). The high symmetry points of the Brillouin zone are the center ( $\Gamma$ ), vertices (K and K'), and midpoint between the vertices (M)[19].

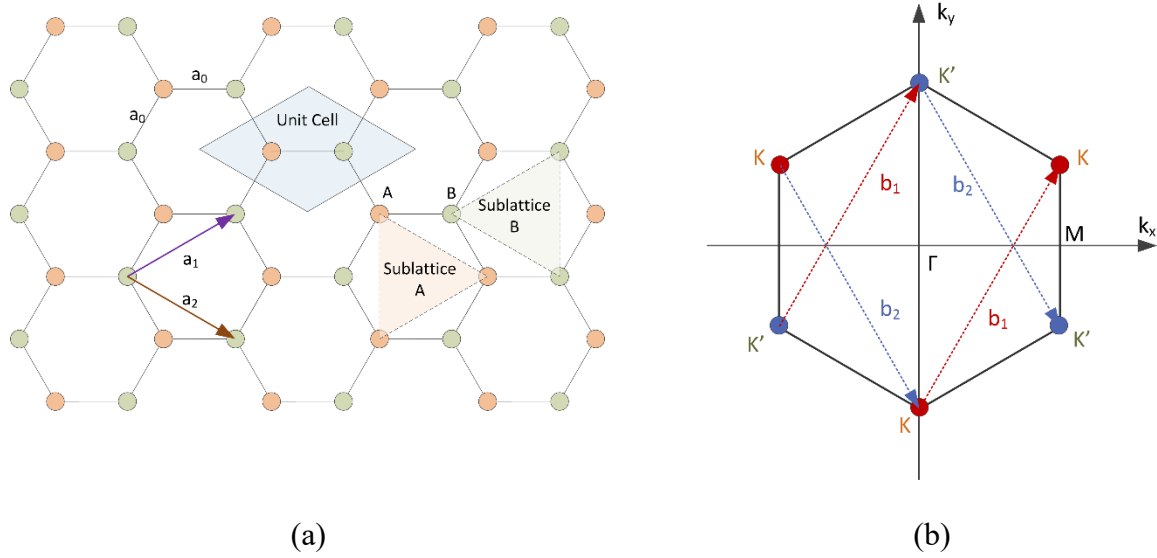


Figure 2.1 (a) Hexagonal placement of Carbon atoms in graphene can be analyzed as two interleaving triangular sublattices or a triangular lattice with a two-atom unit cell. The real spaces basis vectors are  $a_1$  and  $a_2$ . (b) The Brillouin zone of graphene in reciprocal space is hexagonal. The alternate vertices of the hexagon belong to two different groups, each containing the vertices that are reachable from one another by integral multiples of the reciprocal lattice bases  $b_1$  and  $b_2$ .

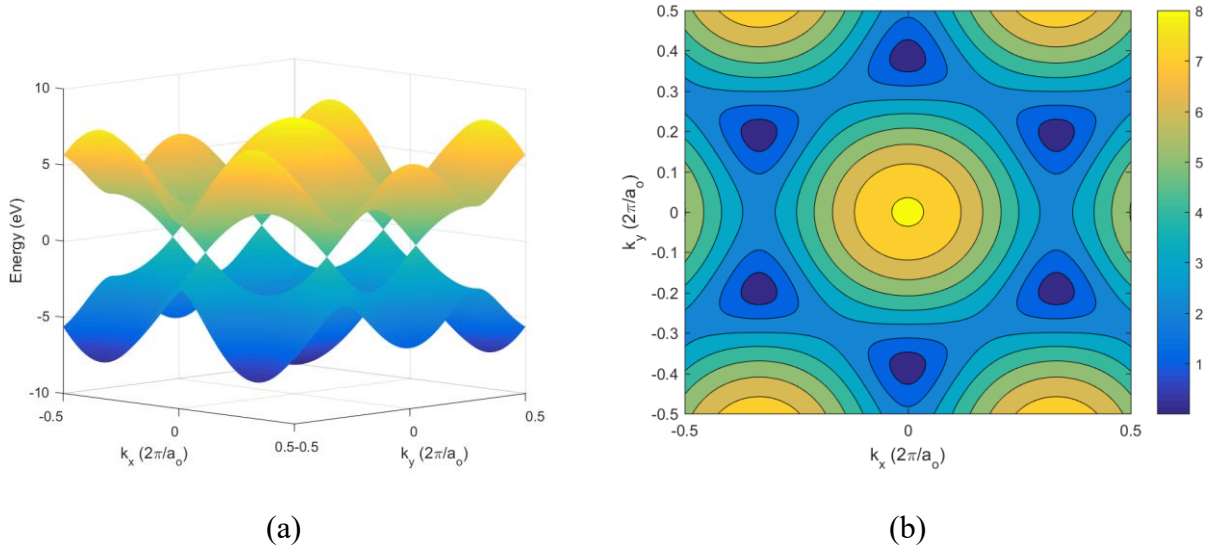


Figure 2.2 (a) The conduction and valence band touch at the vertices of the Brillouin zone. The points of contact have zero energy and are known as the Dirac points. The conduction and valence bands are symmetry around the zero energy plane. (b) Contour plot of the conduction band energy dispersion showing its symmetry. The zero energy points are shown in dark blue.

The electronic band structure of graphene shows the conduction and valence bands touch at the vertices of the Brillouin zone. These are the points of zero energy and are known as the Dirac



points. Near the Dirac point, the energy is proportional to the magnitude of momentum, similar to massless Dirac fermions[19], and the dispersion relation looks conical up to energies in excess of 1 eV [23] as shown in Figure 2.3. All the plots assume a nearest-neighbor hopping energy of 2.7 eV[19].

The linear dispersion relation for energies less than 1 eV make use of Dirac equation to describe charge carriers. It is a very accurate approximation, as most devices operate in this range of energies[23]. In this range as well, the density of states is proportional to the energy of the charge carrier. This unique description of charge carriers in graphene as massless Dirac fermions leads to very interesting electronic properties[19], [20], [22]–[42].

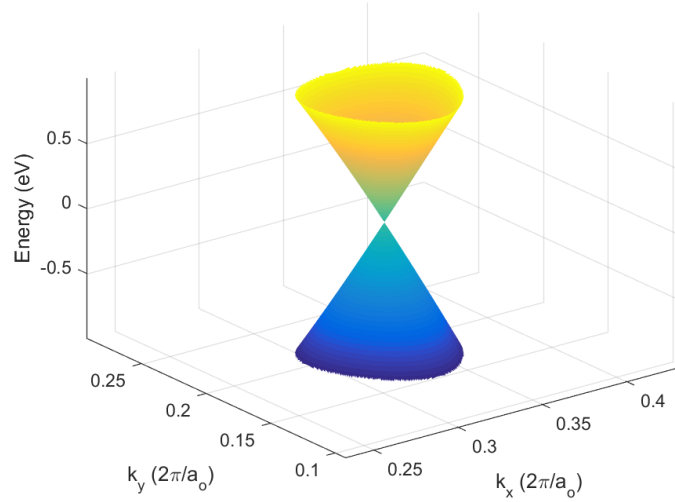


Figure 2.3 Energy dispersion relation around the K point for energies between -1 and 1 eV. The energy is proportional to the magnitude of momentum away from the k point, making the dispersion relation look conical in 3D.

The symmetry of the Brillouin zone allows us to use the 3 high symmetry points to describe the energy describe the energy dispersion relation. The most commonly used cut is the  $\Gamma\text{MK}\Gamma$  cut path shown in Figure 2.4. The energy dispersion relation along the high symmetry cut is shown in Figure 2.5, clearly depicting the Dirac point at the K point.

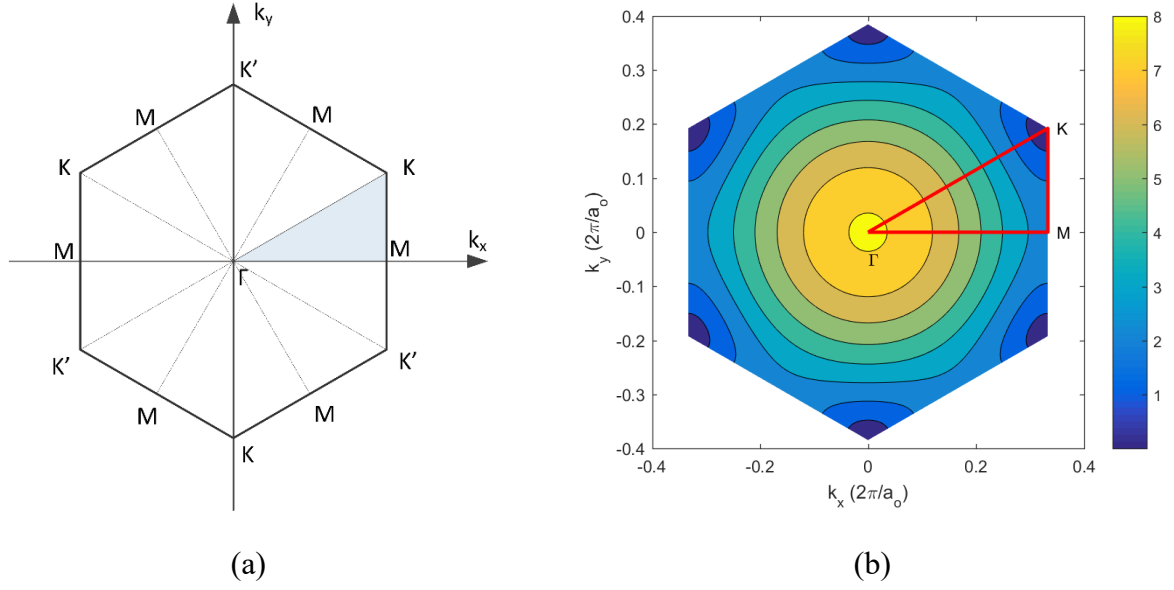


Figure 2.4 (a) Brillouin zone of graphene with the high-symmetry points labelled. The high-symmetry cut path  $\Gamma MK\Gamma$  is marked by the perimeter of the highlighted triangle. (b) a contour plot of the conduction band with the high symmetry cut path highlighted in red.

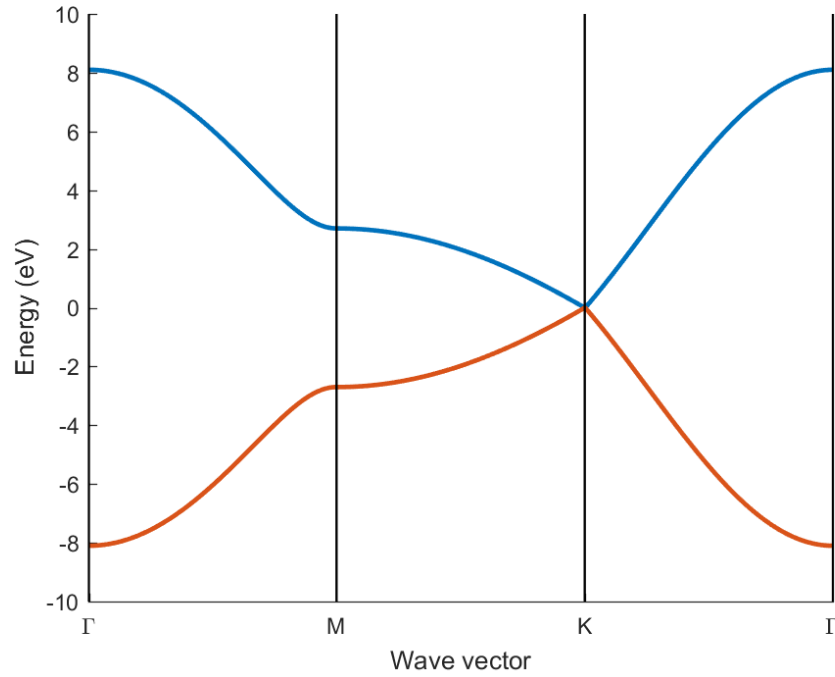


Figure 2.5 Energy dispersion relation across high-symmetry paths in graphene as obtained using the tight-binding approximation with a nearest-neighbor hopping energy of 2.7 eV. The blue curve represents the conduction band while the red curve represents the valence band.

## 2.2. Klein Tunneling and the Absence of Backscattering

Klein tunneling is the absence of back scattering of massless relativistic particles incident normally on a potential barrier[43], [44]. As a virtue of graphene's linear dispersion relation, charge carriers in graphene demonstrate Klein tunneling even in disordered graphene[19], [25], [26], [30], [31], [45]–[58].

Klein tunneling causes the lack of rectification in graphene PN junctions[52], [55], [56]. It allows graphene to operate in the p or n-type doping regimes, or even cascade regions of different doping types without rectification[46], [52], [55]–[57], [59]–[62]. Klein tunneling is the basis of operation of the graphene neurons, synapses and diodes, which are presented in chapters 3 and 4, respectively.

## 2.3. The Role of the Substrate

Simple theoretical analysis of graphene assumes no interaction between the graphene and the substrate. The use of a substrate breaks this assumption by adding different sources of scattering as substrate roughness, substrate phonons, and charges at substrate-graphene interface cause scattering, doping and creates hysteresis in the transfer characteristics, when changing the substrate gating voltage[26], [33], [34], [63]–[82]. In addition, substrate roughness causes structural distortion, which give rise to charge puddles[41], [75], [83].

The substrate role is important in exfoliated graphene, where the optical interference allows the quick identification of graphene optically[84]–[86]. Although graphene can be suspended between contacts[26], [32], [34], [57], [66], [74], the substrate acts as a mechanical support for the graphene ribbon, and substrate dielectric engineering allows the control of top and back gate strengths. Selection of the substrate affects the phonon-induced doping, and proper selection is crucial to prevent mobility degradation[87].

## 2.4. Contact-Induced Doping

Metals in contact with the graphene induce doping and modifications in the band structure of graphene. Ab-initio calculations and experimental results verify that metals contacts dope the graphene, and some metals cause Fermi level pinning[28], [45], [50], [54], [57], [62], [76], [88]–[128]. The shape of resistance vs gate voltage reveals the nature of interaction and its strength. A secondary peak in the resistance vs back gate voltage indicates Fermi level pinning, while asymmetry in the conductance around a single resistance peak reveals contact-induced doping[116], [128].

Contact-induced doping is a strong function of the metal-graphene interface and the metal deposition conditions. Klein tunneling allows graphene channels to have any doping type, but contact-induced doping causes asymmetry in the resistance vs back gate voltage, increasing the resistance at the doping side opposite to that caused by the contact[50], [52], [54], [57], [66], [82], [112], [117], [119], [122], [123], [128].

The effect of contact doping on channel transfer characteristics sets a lower bound on channel length. The finite density of states in graphene causes metal-induced doping for up to 100 nm around the metal contact [123]. In the metal-doped region, the doping level depends strongly on the metal contact characteristics, weakening the control of the gate on the doping, similar to DIBL in deeply scaled CMOS. Contact-induced doping is a physical effect due to the finite density of states of graphene, and should be kept in mind when designing deeply scaled graphene devices.

## 2.5. Charge Transport in CVD Graphene

CVD grown graphene is subject to increased scattering from the grain boundaries, substrate roughness, charged-impurities from transfer chemistry and substrate interface charges[24], [26], [39], [42], [80], [81], [87], [129]–[138]. Careful control of the transfer environment and removal of residuals of transfer residuals is crucial to reduce charged-impurity scattering[29], [67], [71], [76], [78], [87], [104], [139]–[147].

The grain size of CVD grown graphene has risen consistently over the years, reaching few millimeters, allowing the direct measurement of grain-boundary resistance[148]–[153]. However, other effects as substrate roughness and phonon scattering affect the transport in CVD graphene[26], [33], [34], [63]–[82].

Due to the numerous sources of scattering in CVD graphene, charge carrier transport in CVD graphene is predominantly diffusive at room temperature. Charge carriers suffer successive scattering with a mean free path significantly shorter than the device length[154].

## 2.6. Characterization of Graphene

Graphene characterization is essential to determine the quality of graphene, number of layers and for quantitative assessment of the quality of graphene devices. We describe non-destructive ways of determining the number of graphene layers through optical contrast of graphene over a dielectric and by Raman analysis. Raman analysis also allows us to determine the strain and doping in graphene. We also discuss the constant-mobility model, as a way to quantitatively assess the diffusive transport and contact characteristics of graphene devices.

### 2.6.1 Optical Contrast

The contrast of graphene over a dielectric is enhanced by the proper choice of dielectric thickness and dielectric constant. In  $\text{SiO}_2$ , 90 nm and 285 nm are optimal, giving a reflection contrast of up to 15% for single layer graphene; this is the reason why most commercial graphene and exfoliation is done over 90 or 285 nm of  $\text{SiO}_2$ [84]–[86].

The transmission contrast of graphene is about 98% in single layer graphene, making it suitable for flexible and transparent electronics[86].

Both reflection and transmission contrasts are usable in identifying graphene, with the reflection coefficient being more suitable over opaque substrate.

## 2.6.2 Raman Analysis

Raman analysis refers to the use of Raman scattering in studying the properties of materials. Raman scattering is an inelastic scattering process where photons scatter inelastically with phonons, causing a shift in the frequency between the incident and scattered photons[155]. This shift is known as Raman shift. Although Raman shift can be given as a difference in energy, frequency or wavenumber of the incident and scattered light, it is most commonly reported as a wavenumber shift in the unit of  $\text{cm}^{-1}$ . The Raman shift in terms of wavenumber is given as:  $\Delta\omega = \lambda_s^{-1} - \lambda_i^{-1} = \frac{E_{shift}}{hc}$ , where  $\lambda_s$  is the wavelength of the scattered photons,  $\lambda_i$  is the wavelength of the incident photon,  $E_{shift}$  is the Raman shift in energy, and  $h$  and  $c$  are Planck's constant and the speed of light, respectively[156].

Raman scattering can decrease the energy and frequency of the scattered photon due to absorption of some of the incident photon energy to excite a phonon state (Stokes shift), or less-commonly increase the energy of the scattered photon by lowering an already excited phonon state (Anti-Stokes shift). Most Raman processes reported are Stokes processes. Raman processes can be classified as resonant or non-resonant, depending on whether the interactions occur between stationary states of the material involved. Raman scattering occurs with a very low probability compared to elastic (Rayleigh) scattering, making their amplitude very small[156].

Due to the high frequency of photon electric field, Raman scattering is usually electronically mediated, where the charge carriers in a material (typically the low mass electrons) get perturbed by the incident photons then interact inelastically with phonons before returning to their original state, emitting the scattered photon. The momentum conservation requires that the total momentum change in the Raman interaction be almost zero, due to the negligible momentum carried by photons, setting the fundamental Raman selection rule to photons with nearly zero momentum for first-order processes. Accordingly, only optical phonons cause appreciable energy changes through first-order Raman scattering[155], [156]. Multi-phonon and higher-order processes are complicated by the electron-phonon and electron-electron interactions[156]–[159].

Raman analysis is a very versatile tool when it comes to quantifying the properties. Raman analysis can be used to probe the number of graphene layers, strain and doping[93], [156]–[174]. The most prominent features of the Raman spectrum of graphene are the G, D and 2D peaks

occurring at a Raman shift of  $\sim 1580$ ,  $1350$  and  $2700\text{ cm}^{-1}$ , respectively[156]–[159]. An example of the Raman spectrum of a low-defect graphene flake over hBN is shown in Figure 2.6.

The G peak is due to the in-plane transverse optical phonons ( $E_{2g}$  symmetry modes), while the D peak is due to the defect-activated ring-breathing modes ( $A_{1g}$  symmetry modes), in contrast to the 2D peak, which is a double-resonant process that does not require a defect for its activation. As such, G and 2D peaks are always present in any graphene or graphitic sample, while the D peak is mainly present in defective samples[156]–[159].

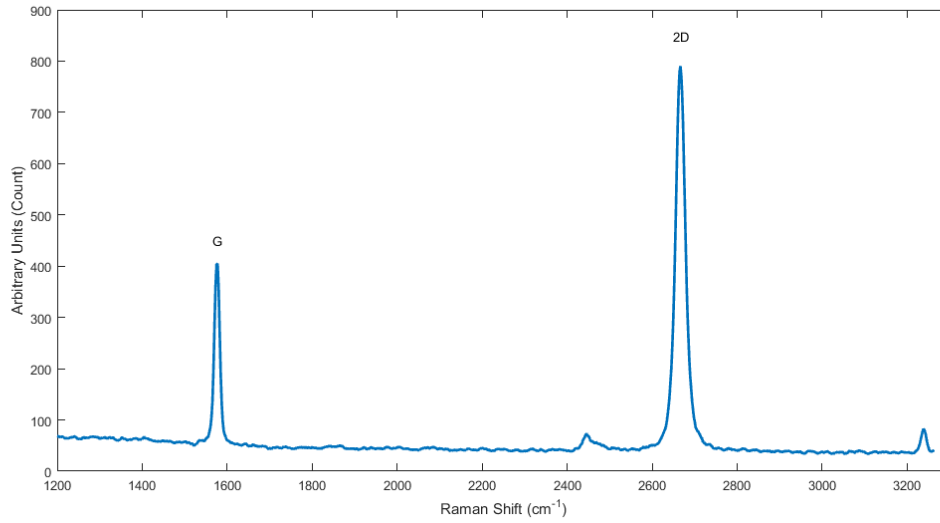


Figure 2.6 Raman spectrum of a graphene sample over hBN showing the distinct G and 2D peaks. The lack of a D peak around  $1350\text{ cm}^{-1}$  demonstrates the low defect density in the graphene flake.

The full-width at half-maximum (FWHM) of the 2D peak is a good indicator of the number of layers of graphene. Single layer graphene shows a symmetry peak, with a  $\text{FWHM} < 50\text{ cm}^{-1}$ [156], [157], [159], [170]. The Raman peaks shift with strain as well, allowing the peak position shift to be used as a strain measure[160], [161], [163], [167], [168], [173], [175], [176]. The ratio of the 2D and G peak values is a function of the substrate thickness and doping of the graphene sheet[156]–[159].

When analyzing measurement data, the use of the integrated area under a curve is less susceptible to noise, compared with the numerical value of the peak maximum, which is very prone to noise and fluctuations. As such, comparing the integrated area is more noise proof.

### 2.6.3 Constant Mobility Model

Transport in CVD graphene at room temperature is diffusive. One of the simplest, yet most versatile models is the constant-mobility model[87]. Unlike more complicated models, it models the transport using bias and back-gate independent numbers, allowing straight-forward statistical analysis of measured data. The model gives a single number for the mobility ( $\mu$ ), Dirac point shift ( $V_D$ ), and charged-impurity concentration ( $n_o$ ). The contact resistance ( $R_C$ ) is assumed to depend assumed to be back-gate voltage dependent, and can be extracted when dual-gated data is available. For single-gated devices, the contact resistance is assumed to be bias-independent.

The constant mobility model fits the results of measurement of device resistance to the equation:

$$R = 2R_C + \frac{L/W}{q\mu\sqrt{n_o^2 + n(V_{bg}, V_{tg})^2}} \quad (2.1)$$

Where  $\frac{L}{W}$  is the number of channel squares, and  $n(V_{bg}, V_{tg})$  is the number of charge carriers in the channel capacitively-induced by voltages shifted from the Dirac point. The Dirac point shift can be included in  $V_{bg}$  by replacing it with  $V_{bg}^* = V_{bg} - V_D$ . In the devices that have no top gate, we use the following Equation:

$$R = 2R_C + \frac{L/W}{q\mu\sqrt{n_o^2 + n(V_{bg})^2}} = 2R_C + \frac{L/W}{q\mu\sqrt{n_o^2 + \left(\frac{C_{bg}}{q}(V_{bg} - V_D)\right)^2}} \quad (2.2)$$

Where  $C_{bg} = \epsilon_{r_{bg}}\epsilon_o/t_{bg}$  is the capacitance per unit area of the back gate oxide. Figure 2.7 shows the results of fitting measured data to Equation (2.2), the value of the Dirac point voltage  $V_D$  is about -12 V. All the important features of the data (peak position, broadening due to  $n_o$ , and resistance dependence on  $V_{bg} - V_D$ ) are captured despite the imperfect fit. We will use Equation (2.2) throughout this work when analyzing data from devices without a back gate.

In Chapter 3, we analyze devices with multiple top gates over the channel and no top gates over the contacts. In such devices, we add the resistances of all sections in series to get the overall device resistance yielding:



$$R = 2R_C + \sum_i \frac{L_i/W}{q\mu \sqrt{n_o^2 + \left(\frac{C_{bg}}{q}(V_{bg} - V_D) + \frac{C_i V_i}{q}\right)^2}} \quad (2.3)$$

Where  $L_i$  is the length of each section, and  $C_i$  and  $V_i$  is the areal capacitance and voltage applied on each top gate. We neglect the interface resistance between regions of different doping and assume all the gates share the same channel width  $W$ .

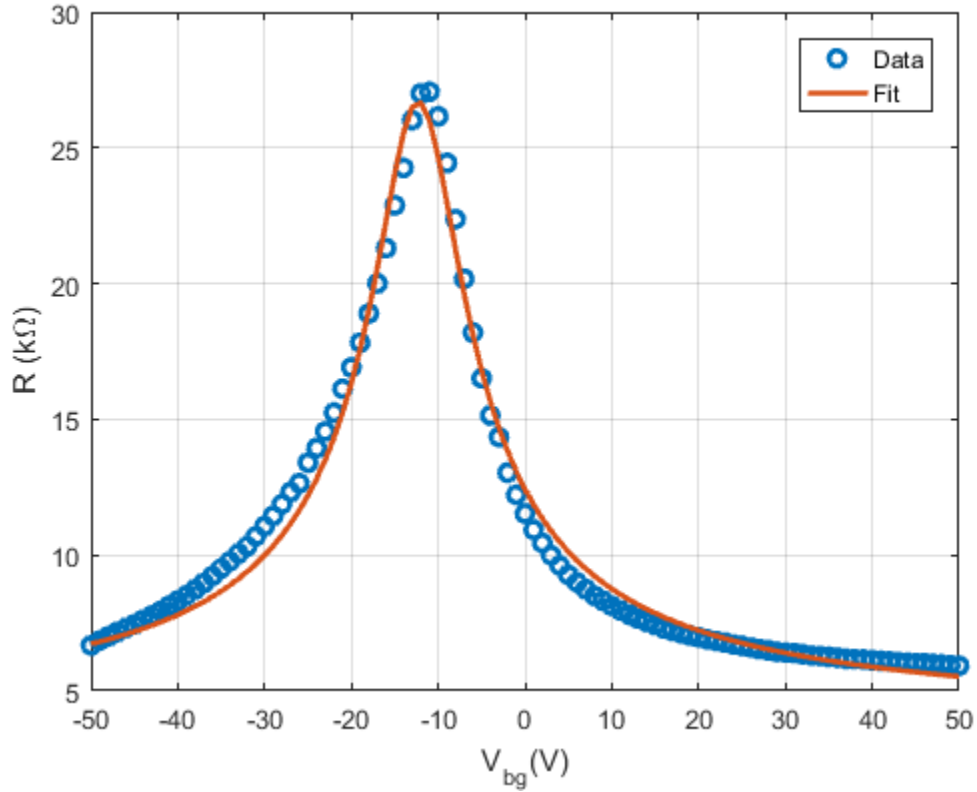


Figure 2.7 Measured data and fit results computed using the constant mobility model for back-gated graphene FETs. The RMSE is 0.653 kΩ.

Throughout this work, we use the constant mobility model for characterizing the devices fabricated. As in all our devices, the gate covers only part of the channel, and the data will be fit using a constant value for  $R_C$ .

# 3) All-Graphene Neuromorphic Computing Architectures

Neuromorphic or brain-inspired computing is a distributed computing paradigm proposed to overcome the bottlenecks of von Neumann machines[177]–[182]. In neuromorphic computing, the data storage and processing is distributed among a network of nodes called neurons, interconnected by a web of connections known as the synapses. There are different architectures for neuromorphic computing, which can be classified by how the synapses interconnect the neurons.

We focus on the implementation of an all-graphene neuromorphic computing system, based on a type of neural networks known as cellular neural networks. We start by a brief introduction to cellular neural networks (CNNs), followed by an overview of an all-resistance CNN architecture that can be efficiently implemented using graphene. We then discuss the implementation of the proposed neurons and synapses and present the results of measured prototype devices. We conclude by a discussion of the performance aspects and limitations of the proposed architecture.

## 3.1. Cellular Neural Networks (CNNs)

There are different families of neural networks, such as Spike-Timing Dependent Plasticity (STDP)[12], [182]–[194], and Oscillator Neural Networks (ONNs)[8], [11], [13], [178], [193], [195], [196]. We focus on a different family of neural networks that is continuous-time and continuous-voltage analog cellular neural networks[197], [198].

In Cellular Neural Networks (CNNs), the neurons act as saturating summing nodes. The neurons sum the input applied to them and the output of a neuron is the sum of the inputs saturated using a sigmoidal saturating function. The saturation of the neuron’s output bounds it and stabilizes the network. The inputs applied to a given neuron are the outputs of its neighbors, weighted by the synaptic weight connecting the neurons together, as well as an external, independent stimulus. In our work, we focus on networks without an external stimulus. We can

thus think of a “cell” as a central neuron with the synaptic weights used to connect it to its neighbors. This is shown schematically in Figure 3.1.

Unlike other neural network implementations where the synaptic weight is set by the spiking activity, a property known as synaptic plasticity [191], CNNs operate in a continuous-time, continuous-voltage fashion. The synaptic weights are determined offline and are used to set the function of the circuit; CNNs to have no synaptic plasticity.

CNNs are asynchronous by nature and all the nodes take part in computations simultaneously. The modularity of the architecture allows it to implement high-complexity, large systems. In addition, CNNs are highly robust against variabilities and non-idealities in its building units, making it very suitable for implementation using technologies with high variability and non-idealities in components[197]–[200].

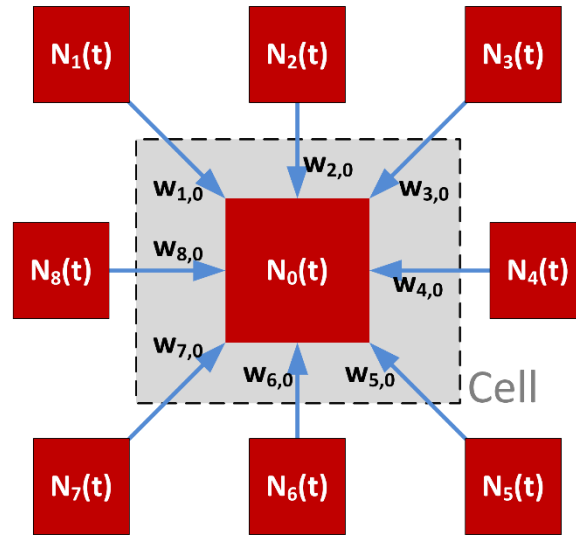


Figure 3.1 Nearest-Neighbor CNN. The neurons (nodes) are shown as red squares, while the synapses are the blue arrows. The Cell, shown in gray, is composed of a single neuron and the synapses connecting it to its neighbors.

Computations are performed by first presetting all the neurons to the initial values used in the computation (network input) and setting the synaptic weights to correspond to the function of interest. The network is then left to relax, reaching a steady state that corresponds to the computed output (network output). A more formal discussion of the theoretical foundations and mathematical model can be found in [197], [198].

### 3.2. All-Resistance CNNs

CMOS implementations of CNNs have been marred by area and power requirements that limit the network size considerably [199], [201], [202]. In analog CMOS implementations of CNNs, one major bottleneck is the matching requirement between component values, which leads to large area overheads and the requirement to tuning circuitry [201], [202].

To overcome these requirements, another implementation using an all-resistive architecture for nearest-neighbor CNNs that only requires local matching between components of the same cell has been proposed [59], [60]. It relies on using local potential dividers to implement the synaptic weighting, and the neuron output is controlled using voltage-controlled resistors, which set the voltage applied to a capacitor that stores the state (voltage) of the neuron. The all-resistive architecture is shown in Figure 3.2.

This architecture has several advantages: 1) the output saturation is inherent in the neurons, as the output DC voltage is set by the potential divider between  $R_{PU}$  and  $R_{PD}$ ; 2) the synaptic weights depend only on the potential divider of two digitally-controlled resistors, relaxing the global matching requirement in CMOS implementations; 3) digitally-controlled resistors used to set the synaptic weights, allowing us to store the synaptic weight settings in CMOS memory, which generally have a very high capacity and low footprint; 4) The synapses are composed of two resistors in series, with complementary code words applied on them making their sum fixed, thus there is no code-dependent loading on the neuron; and 5) the neuron output voltage is determined by the analog voltage-controlled resistors  $R_{PU}$  and  $R_{PD}$ , whose input is an analog voltage coming from neighboring neurons, without the need to do any analog-to-digital or digital-to-analog conversion. The synapse resistors can be made to have negligible loading on the neuron output, mitigating their effect on reducing the dynamic range of the circuit and reducing their contribution to the power consumption.  $R_{PU}$  ( $R_{PD}$ ) is labelled as the connected to the inhibitory (excitatory) outputs because its increase reduces (increases) the output voltage, which is labelled as inhibition (excitation) in neuromorphic terms.

In total we need 2 analog voltage-controlled resistors per neuron ( $R_{PU}$  and  $R_{PD}$ ) and  $2 \times 2$  digitally-controlled resistors per synapse. This means that we need one capacitor, 2 analog voltage-

controlled resistors and 36 ( $2 \times 2 \times 9$ ) digitally-controlled resistors per cell. This allows for a very compact implementation, since the matching is required locally only; the synapse potential divider elements need to be matched to have linear synaptic weighting with the applied code word.

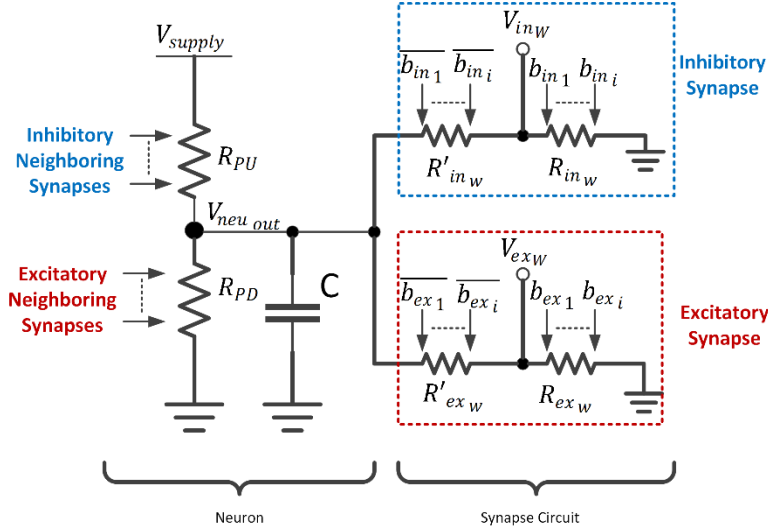


Figure 3.2 All-resistance architecture CNN architecture. The potential dividers inside the red and blue boxes provide the synaptic weighting of the neuron output (capacitor voltage), using digitally controlled resistors. The pull-up- and pull-down resistors ( $R_{PU}$  and  $R_{PD}$ ) are analog voltage-controlled resistors, with the resistance control inputs connected to the synoptically-weighted output of the neighboring neurons.

One of the advantages of using graphene to implement the all-resistance CNN architecture is that graphene contacts do not suffer from the source/drain junction capacitance. If this architecture is implemented using CMOS, the junction capacitors of the synapses add up to the total capacitance in the system, especially at the neuron output node, which would slow down the time constant of the cell and system as a whole.

### 3.2.1 Limitations of All-Resistance CNNs architecture

The proposed all-resistance architecture depends on the strength of the control terminal of the analog voltage-controlled resistors to set the output voltage of the neuron. Accordingly, the control terminal of the analog voltage-controlled resistors should be strong enough to pull the output voltage of the neuron to the required level. The strength of the control terminal is what provides the regeneration in the network; it should be strong enough to regenerate the analog voltage change at the input. Otherwise the signal levels will degrade and the network size would be very limited.

If we use graphene to implement those resistors, the maximal resistance change range is achieved by using strong gate (high capacitance) and having a low charged-impurity concentration. Quantitatively, neglecting the contact resistance, the resistance of a graphene sheet as per the constant mobility model is given as:

$$R = \frac{L/W}{q\mu \sqrt{n_o^2 + \left(\frac{C(V - V_D)}{q}\right)^2}} \quad (3.1)$$

The rate of change per units resistance is given as:

$$\frac{\partial R}{R \partial V} = - \frac{V - V_D}{\left(\frac{qn_o}{C}\right)^2 + (V - V_D)^2} = - \frac{V - V_D}{V_{n_o}^2 + (V - V_D)^2} \quad (3.2)$$

Where we denote the gate voltage that would yield a charge density equal to the charged-impurity concentration  $V_{n_o}$ . This function peaks at  $V = V_D \pm V_{n_o}$ , and the maximum rate of change of resistance is given as:

$$\left. \frac{\partial R}{R \partial V} \right|_{V=V_D \pm V_{n_o}} = \mp \frac{1}{2V_{n_o}} = \mp \frac{C}{2qn_o} = \mp \frac{\epsilon_r \epsilon_o}{2qd n_o} \quad (3.3)$$

Where  $\epsilon_r$ ,  $\epsilon_o$  and  $d$  are the dielectric constant of the oxide, free space permittivity and thickness of gate oxide. The stronger the gate (higher  $\epsilon_r$  and smaller  $d$ ) and the lower the charged-impurity concentration the more resistance change can be achieved by the gate.

Another intuitive explanation is through the impact of charged-impurity concentration on the resistance change range. The higher the charged-impurity concentration the lower high-to-low resistance change range can be achieved by a given gate. If the high-to-low ratio is small enough the output voltage swing would be low and might not be enough to regenerate a small input change at the input.

This discussion elucidates the importance of low charged-impurity concentration and strong gates for successful implementation of graphene all-resistance CNNs.

### 3.3. Graphene Neurons and Synapses

Graphene neurons can be created by dual-gated graphene ribbons with equal length gates, while the synapses can be implemented by using binary-scaled gates. This can be explained by deriving the resistance of a graphene ribbon using the constant mobility model for a ribbon with multiple top gates and a single common back gate, similar to the one shown in Figure 3.3.

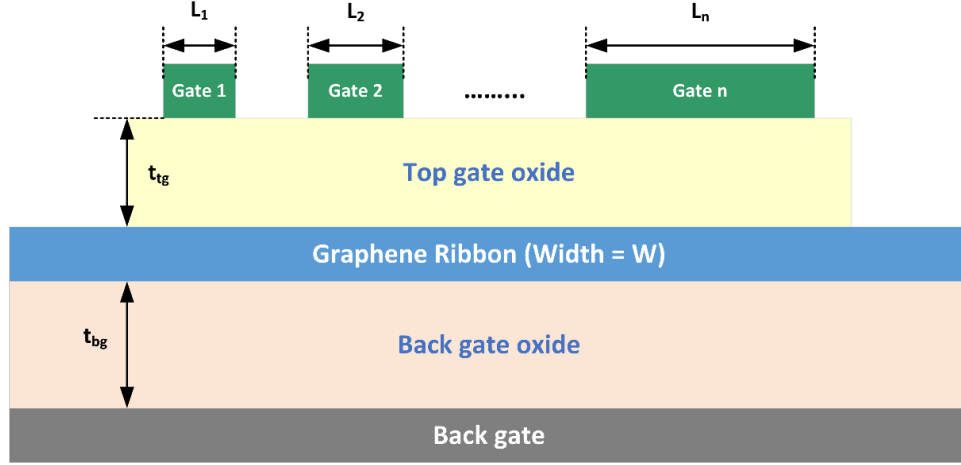


Figure 3.3 Cross-section of an n-gate graphene device. There are n top gates and one common back gate.

The resistance of such a structure, neglecting the contact resistance is given as:

$$\begin{aligned}
 R(V_1, V_2, \dots, V_n, V_{bg}) &= \rho_u(V_{bg}) \frac{L_u}{W} + \sum_{i=1}^n \rho_i(V_i, V_{bg}) \frac{L_i}{W} + \frac{R_{T_i}(V_i, V_{bg})}{W} \\
 &\approx \rho_u(V_{bg}) \frac{L_u}{W} + \sum_{i=1}^n \rho_i(V_i, V_{bg}) \frac{L_i}{W}
 \end{aligned} \tag{3.4}$$

Where  $W$  is the channel width,  $\rho_u$  and  $L_u$  are the sheet resistivity and length of the ungated sections,  $\rho_i$  and  $L_i$  the sheet resistivity and length of the  $i^{\text{th}}$  gates sections,  $V_i$  and  $V_{bg}$  the voltage of the  $i^{\text{th}}$  top gate and back gate,  $R_{T_i}$  is the interface tunneling resistance per unit width for the charge carrier to tunnel from the ungated section to the  $i^{\text{th}}$  gate and back out if the gating causes alternate doping types in the channel.  $R_{T_i}$  can be neglected relative to the sheet resistance due to Klein-tunneling at the interfaces[55], [56]. The ability to have alternating dopant type across the

channel without rectification is a direct result of Klein-tunneling in graphene, even for non-ballistic transport devices[49], [58], [203]. The use of a gate-dependent specific sheet resistance ( $\rho_i$ ) for each gate is due to the possibility of process gradients across the device, the presence of charge puddles and charge inhomogeneity, and because metal gates can alter the phonon scattering modes[41], [80].

In case of neurons, the gate lengths are equal ( $L_1 = L_2 = \dots = L_n$ ), making the contribution of the gates in the resistance change equal, while for synapses, they are binary scaled. For binary scaled gates, we have  $L_2 = 2L_1, L_3 = 2L_2, \dots, L_n = 2L_{n-1}$ , making the device act as a string of binary-scaled resistors. Accordingly, if the binary scaled gates are connected to the corresponding bits of a digital control word, they will act as a digital to resistance converter. This can be quantified by setting  $\rho_i = \rho_g$  for all gates, allowing us to rewrite Equation (3.4) as:

$$\begin{aligned} R(V_1, V_2, \dots, V_n, V_{bg}) &\approx \rho_u(V_{bg}) \frac{L_u}{W} + \sum_{i=1}^n \rho_g(V_i, V_{bg}) \frac{L_i}{W} \\ &= R_u + \sum_{i=1}^n \rho_g(V_i, V_{bg}) \frac{2^{i-1}L_1}{W} = R_u + \Delta R \end{aligned} \quad (3.5)$$

If a digital signal having the values  $V_i = \{\tilde{V}_0, \tilde{V}_1\}$ , corresponding to a digital bit  $b_i = \{0,1\}$ , is applied on the top gates, the resistance change term ( $\Delta R$ ) as a function of code word can be written as:

$$\begin{aligned} \Delta R &\approx \sum_{i=1}^n \left( \rho_g(\tilde{V}_0, V_{bg}) + b_i \left( \rho_g(\tilde{V}_1, V_{bg}) - \rho_g(\tilde{V}_0, V_{bg}) \right) \right) \frac{2^{i-1}L_1}{W} \\ &= \sum_{i=1}^n \left( \rho_g(\tilde{V}_0, V_{bg}) + b_i \Delta \rho \right) \frac{2^{i-1}L_1}{W} = \sum_{i=1}^n 2^{i-1} (R_0 + \Delta R_0 b_i) \end{aligned} \quad (3.6)$$

Equation (3.6) shows how the binary scaling the gate lengths would make the device act as a digital-to-resistance converter, which is what we need for each resistor in the synapses.



Interestingly, this architecture allows for both positive and negative resistance change with the applied code word (voltage), depending on the relation between the back-gate voltage and the Dirac point. This is illustrated using Figure 3.4.

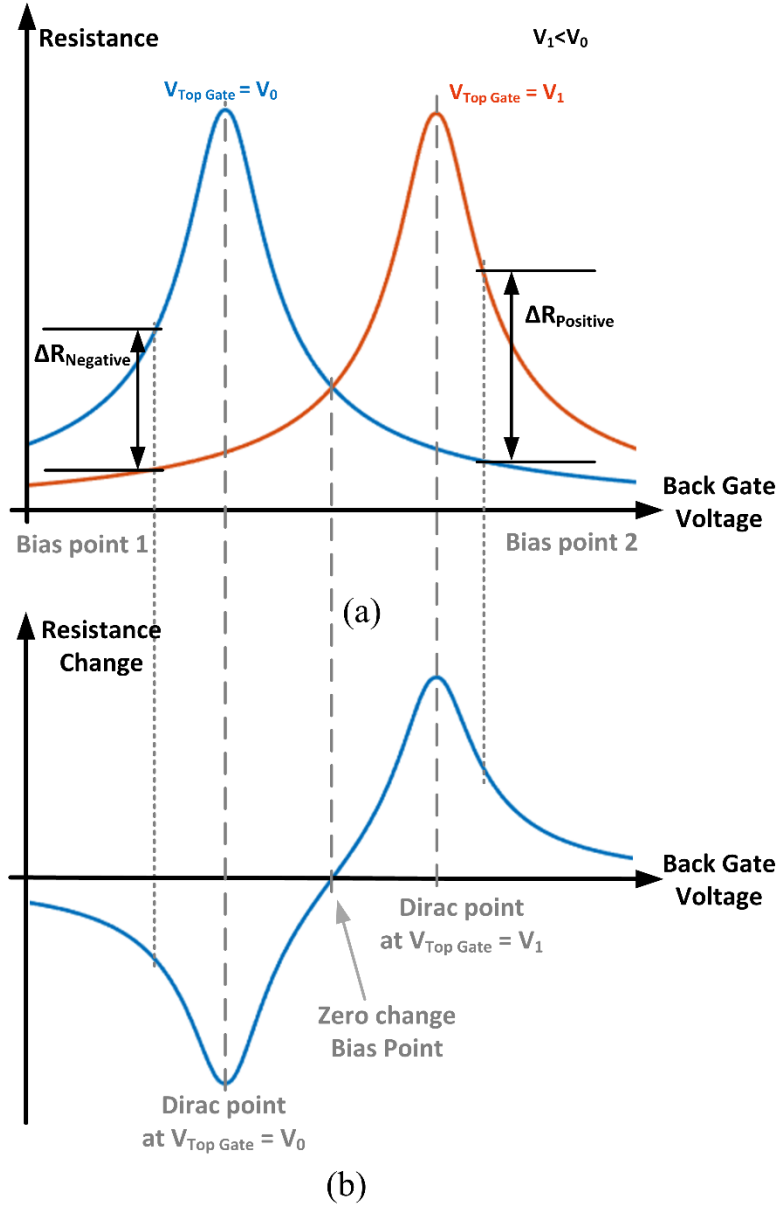


Figure 3.4 (a) Resistance vs back gate voltage of a section of a graphene channel at two top gate voltages  $V_1$  and  $V_0$ , and (b) resistance change, defined as  $R(V_0) - R(V_1)$ , vs back gate voltage. Using a back-gate voltage around  $V_1$  would cause a positive resistance change, while using a back-gate voltage around  $V_0$  would cause a negative resistance change.

Figure 3.4(a) shows the resistance of the ribbon when a at two top gate voltages  $V_1$  and  $V_0$  where  $V_1 < V_0$ . When  $V_1$  is applied on the top gate, the ribbon becomes more p-type relative to

when  $V_0$  is applied, making the Dirac point shift right relative to its position when  $V_0$  is applied. The resistance change, defined as the resistance difference between the case when  $V_1$  is applied and when  $V_0$  is applied, is shown in Figure 3.4(b). When the back-gate voltage is such that the device is biased near the Dirac point when  $V_1$  is applied the resistance increases when  $V_1$  is applied relative to  $V_0$ , and vice versa.

The dependence of the resistance change direction allows us also to use the graphene synapses as digital-to-resistance converters with positive or negative slope (resistance change with code word), depending on the applied back-gate voltage.

The ability to implement PN junctions without rectification, and creating both positive and negative resistance change after fabrication through an externally applied voltage are unique properties to graphene, which allows the device to be used for applications other than neuromorphic computing, such as data converters[204].

### 3.3.1 Scaling limits of graphene all-resistance CNNs

The graphene ribbons used to implement the CNNs could be scaled in width until a band-gap is opened or Line-Edge Roughness (LER) scattering becomes significant, increasing the resistance significantly. A band-gap of 10 meV opens in graphene when the width is about 30 nm[205], and LER-induced scattering degrades the mobility when the width is less than about 60 nm[137]. As such, we do not anticipate problems to occur down to device widths of 60 nm. If we are to design the neurons with an aspect ratio of 10, that would yield a neuron with a size of  $60 \text{ nm} \times 600 \text{ nm}$  or  $0.036 \mu\text{m}^2$ . To our knowledge, the smallest CMOS implementation for a binary (2-level) synapse is  $3.2 \mu\text{m}^2$ , and it implemented integrate-and-fire networks using 45 nm CMOS[206]. Other non-CMOS implementations exist, but they focus on the implementation of STDP and ONN networks[8], [11]–[13], [182]–[184], [186], [190], [207]–[210]. This demonstrates the high scalability, and footprint of the proposed graphene all-resistance implementation of CNNs.

## 3.4. Measurement Results

We fabricated prototype devices for a 3-bit synapse using the flow outlined in Appendix B. An optical microscope and false-color image of the fabricated device is shown in Figure 3.5. The

devices were tested per the test setup shown in Appendix C. An important feature in Figure 3.5 is the use of a common centroid in distributing the gates across the synapse. This reduces the impact of process gradient in modifying the strength of the gate and equalizes the strength of each gate[60]. This was verified experimentally, where using direct binary scaled lengths showed unequal gate strengths in modifying the resistance of the synapse[59].

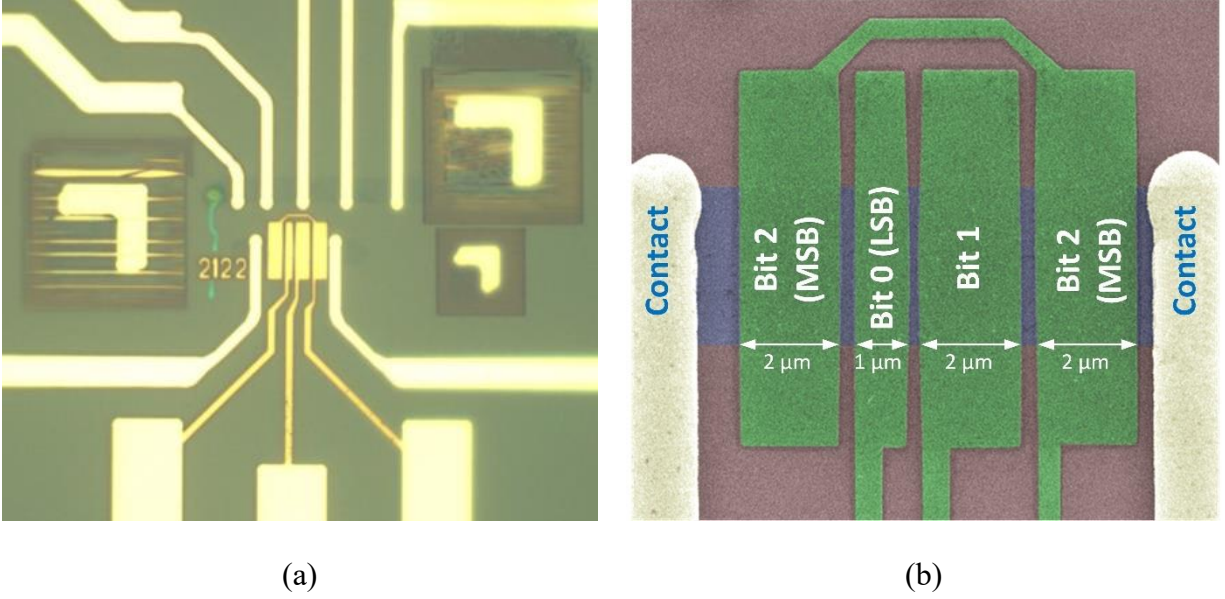


Figure 3.5 (a) Optical microscope, and (b) False color SEM image of 3-bit graphene synapse. The binary-scaled gate lengths are distributed in a common centroid fashion to reduce the effect of process gradient on gate strength. The spacing between the two contacts is  $9\text{ }\mu\text{m}$ , and the width of the channel is  $2.75\text{ }\mu\text{m}$ .

The longest gate was chosen to act as the Most Significant Bit (MSB) because it has the biggest impact on the resistance change compared to the other gates. The measured resistance of the device versus code word at two different back gate voltages corresponding to the maximum positive and negative resistance change is shown in Figure 3.6. The top gate voltage used for binary 0/1 was 0/0.067 V respectively. The resistance changes by about  $15.7\text{ k}\Omega$  in the positive direction ( $19.5 - 35.4\text{ k}\Omega$ ) and  $8.7\text{ k}\Omega$  in the negative direction ( $19 - 27.7\text{ k}\Omega$ ). The inequality between the resistance change ranges and the negative resistance change at a lower back gate voltage despite applying a positive top gate voltage indicates the present of negative oxide charges affecting the field generated by the gate. This was confirmed by evaluating the amount of Dirac point voltage shift created by the top gate when a positive and negative voltages are applied, and it was found that

the negative gate voltage causes more resistance change. The difference in strength was found to be due to a negative oxide charge of density of  $8.74 \times 10^{11} \text{ cm}^{-2}$ .

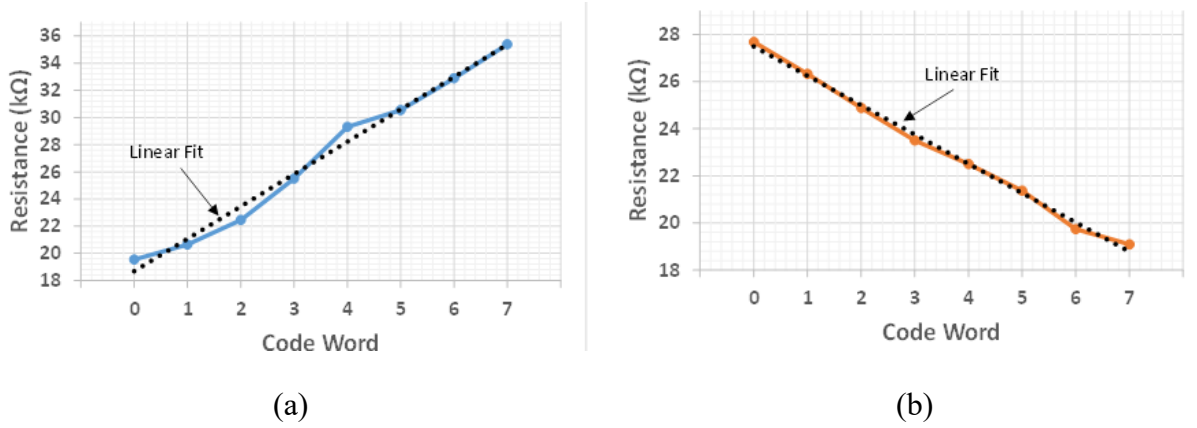


Figure 3.6 Resistance change vs applied digital code word at a back-gate voltage of (a) 22.67 V, and (b) 8V. These back gate voltage correspond to the maximum resistance change in each direction. The top gate voltage used was 0.067 V and 0V for binary 0 and binary 1, respectively. The dotted black line represents the best linear fit.

To evaluate the strength of each gate we extracted the resistance change per unit square of each gate. The extracted gate strengths per square, shown in Figure 3.7, indicate that all the gates show equal strength, with a behavior similar to that shown in Figure 3.4. This equality in strength is in line with the strong linear behavior and small non-linearity seen in the resistance vs code word measurements shown in Figure 3.6. Any inequality in gate strengths manifests itself as a non-linearity in the resistance versus code word characteristics[59], [60].

The measured devices were used to build Verilog-A models that were used for system-level simulations using Spectre. An architecture of  $5 \times 4$  neurons was built and programmed to perform edge and line detection as well as pattern recognitions[59]. Different functions have different synaptic weights, which were determined by calculating them offline, using MATLAB. In each case, the network was precharged to the input value and the network was left to relax, converging to the output of the calculation. The system was able to perform edge and line detection correctly and recover(recognize) distorted patterns with up to 28% distortion[59].

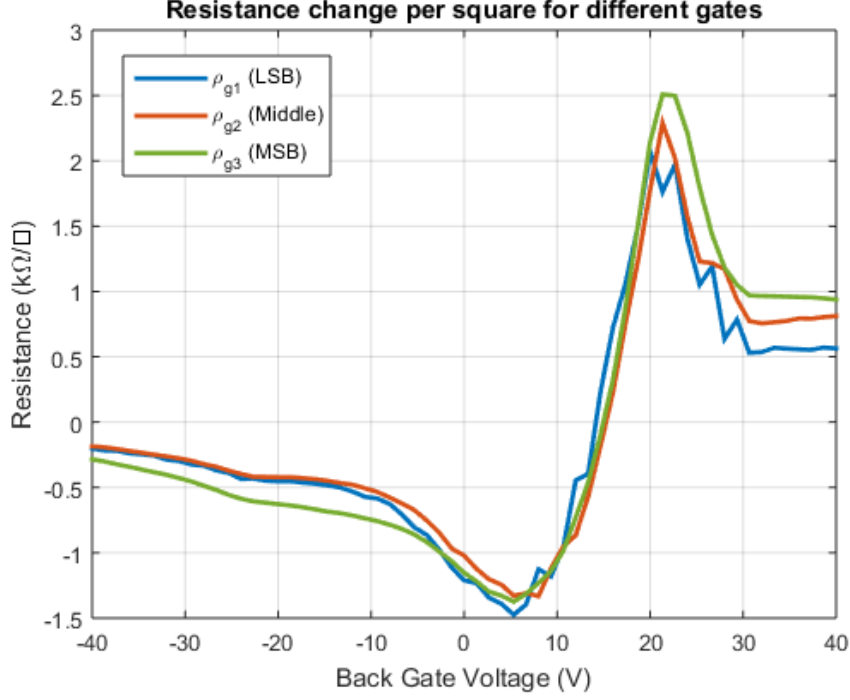


Figure 3.7 Extracted resistance change per unit square for each gate. The extracted values show that the gates have equal strength.

### 3.5. Conclusion

We have demonstrated an area efficient implementation of CNNs using graphene to implement an all-resistance architecture of synapses and neurons. The devices depend on the low charged-impurity concentration and high gate strength to be able to regenerate the voltage changes at the input. The graphene implementation of the all-resistance CNN architecture is highly scalable with very low area compared to CMOS implementations. We fabricated prototype devices for the synapses and used it to extract the information needed to build Verilog-A models for use in system-level simulations validating the viability of the architecture. The less the charged-impurity concentration and the stronger the device gates area, the bigger the network can be.

From a system perspective, more work need to be done on the size limits of the network and the limitations posed by device non-idealities. The maximum number of characters that can be stored in a network of a given size and its relation to the training scheme used to identify the required synaptic weights is still an open problem. Finally, there are no indicators on when a

network has converged, but the network is assumed to have converged once the rate of change of all neuron outputs approaches zero[197], [198]. These problems need to be addressed and the impact of device non-idealities has to be evaluated for this architecture to be deemed mature enough for implementation.

## 4) Graphene Low-Loss Diodes

Graphene's unique electronic properties, make it attractive in designing devices that utilize the photon-like behavior of charge carriers. The photon-like behavior of charge carriers in graphene allows us to build zero turn-on voltage diodes, where the rectification arises due to anisotropic carrier transport across the device. In this chapter, we propose an implementation of low-loss graphene diodes using asymmetric transmission of charge carriers across an oblique barrier. We present measurement results from prototype devices showing how our proposed diodes outperform other implementations and discuss the performance limitations of our proposed structure.

It is important to note that all graphene diodes do not have a turn-on voltage. Graphene diodes show asymmetry with once the voltage polarity on the device is flipped, hence they are all low-loss diodes. When comparing the performance of different low-loss diodes we use the current conduction asymmetry ( $A$ ), defined as the ratio of the forward to reverse current ratio at the same voltage magnitude:

$$A = \left| \frac{I(V +)}{I(V -)} \right| \quad (4.1)$$

Where  $V +$  and  $V -$  represent the same voltage magnitude but applied in the forward and reverse directions, respectively[211]. The asymmetry of a perfect linear resistor is unity, and the asymmetry of an ideal diode approaches infinity as it indicates perfect blocking of reverse current.

We start with a brief overview of geometric diodes, outlining their principle of operation. We then propose a diode architecture based on the total internal reflection of charge carriers incident on an oblique barrier, discussing its principle of operation and performance limitations before presenting measurement results of fabricated prototype devices. We end the chapter by discussing ways to enhance the performance of the proposed device.

## 4.1. Geometric Graphene Diodes

Geometric diodes use the asymmetric transmission of charge carriers across an aperture to achieve asymmetric conduction[211]–[216]. The principle of operation of such diodes can be explained using the toy model shown in Figure 4.1.

Charge carriers incident from the left to right get collimated by the geometry of the channel leading to the aperture, allowing most of them to pass through. On the other hand, charge carriers traveling from the left to right do not get collimated and only a small portion passes through the aperture. A formal analysis of geometric diodes can be found in [212].

The maximum current conduction asymmetry reported for geometric diodes was  $\sim 1.35$  for exfoliated graphene and 1.15 for CVD graphene[211]. The reduction in asymmetry obtained in CVD graphene can be attributed to the increase in scattering, increasing the resistance of the forward path and allowing carriers to pass in the reverse direction[24], [25], [27], [29], [31], [79], [81], [129], [130], [132], [137], [147], [217]. This is a strong indicator of the impact of scattering on the performance of any diode utilizing the photon-like behavior of charge carriers in graphene.

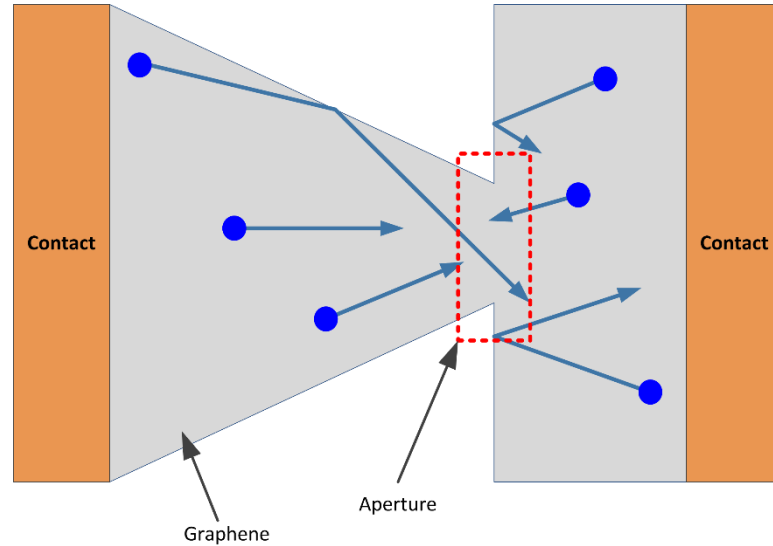


Figure 4.1 Toy model representing the asymmetric transmission across an aperture. Charge carriers (blue circles) get collimated into the aperture when traveling from left to right, causing large transmission. On the other hand, charge carriers travelling from right to left do not get collimated and transmit only through a small area.



## 4.2. Oblique Incidence Diodes

Oblique incidence diodes depend on the concept of total-internal reflection of charge carriers from an oblique junction to cause asymmetric conduction. Klein tunneling in graphene causes normal incident carriers to always pass through, but obliquely incident carriers can be reflected. Asymmetric conductance across graphene oblique PN junction has been predicted theoretically and measured experimentally[47], [49], [51], [52], [58], [218]–[225].

The angular condition on reflection can be obtained by matching the boundary conditions at the barrier, which yields a Snell's law-like relation[44], [49], [58], [203]:

$$|E - E_{D_1}| \sin(\theta_1) = |E - E_{D_2}| \sin(\theta_2) \quad (4.2)$$

The critical angle beyond which reflections of charge carrier occur can be obtained by setting  $\theta_2$  to  $\pi/2$ :

$$|E - E_{D_1}| \sin(\theta_c) = |E - E_{D_2}| \sin\left(\frac{\pi}{2}\right) \quad (4.3)$$

Where  $E$  is the energy of the charge carrier,  $E_{D_1}$  and  $E_{D_2}$  is the energy of the Dirac point in the incidence medium (subscript 1) and the transmission medium (subscript 2) respectively, and  $\theta_c$  is the critical angle of incidence in the first medium. This is depicted in Figure 4.2 for a case when  $E_{D_2} < E_{D_1}$ , causing transmission away from the normal.

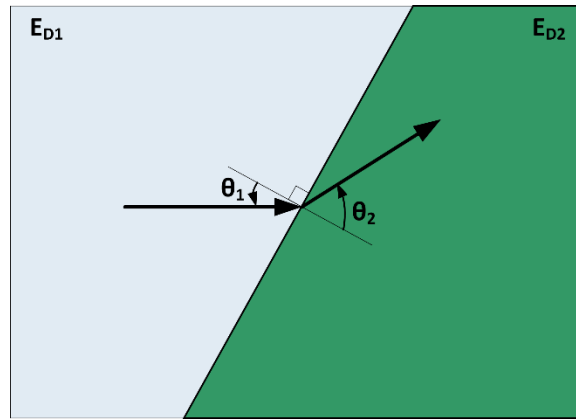


Figure 4.2 Schematic presentation of charge carrier motion across an oblique carrier when  $E_{D_2} < E_{D_1}$ , causing transmission away from the normal. Further increase in  $\theta_1$  will cause  $\theta_2$  to increase till it reaches 90 degrees. Further increase in  $\theta_1$  causes total internal reflection of charge carriers.

The structure of an oblique incidence diode is shown in Figure 4.3. The oblique gate sets the angle of the potential barrier ( $\theta$ ) and the voltages on the top and back gate set the potential barrier height.

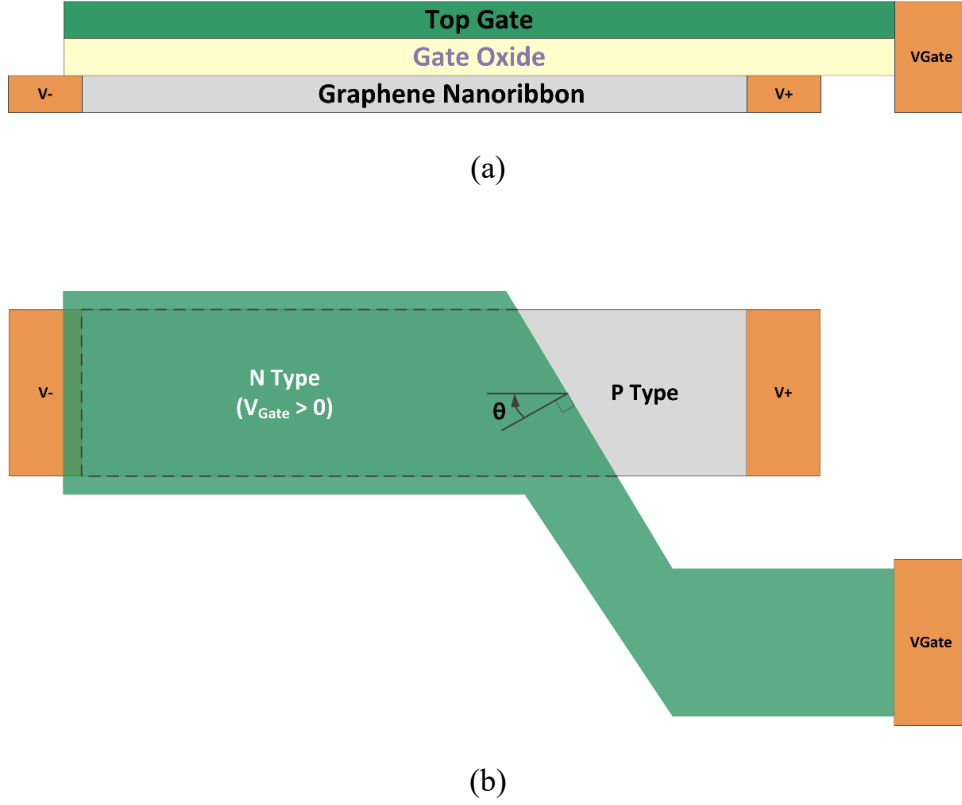


Figure 4.3 (a) Cross-section, and (b) Top view of oblique incidence diode. The whole device lies on a back gate that is not shown for clarity. The top gate is oblique relative to the channel. The potential barrier can be set by controlling the voltage of the top and back gates.

The transmission coefficient across an abrupt junction vs the energy of charge carrier and angle of incidence when tunneling in different directions across regions with  $E_{D_1} = 0.5$  eV and  $E_{D_2} = -0.5$  eV is shown in Figure 4.4. Transmission asymmetry occurs except when  $E = 0$ .

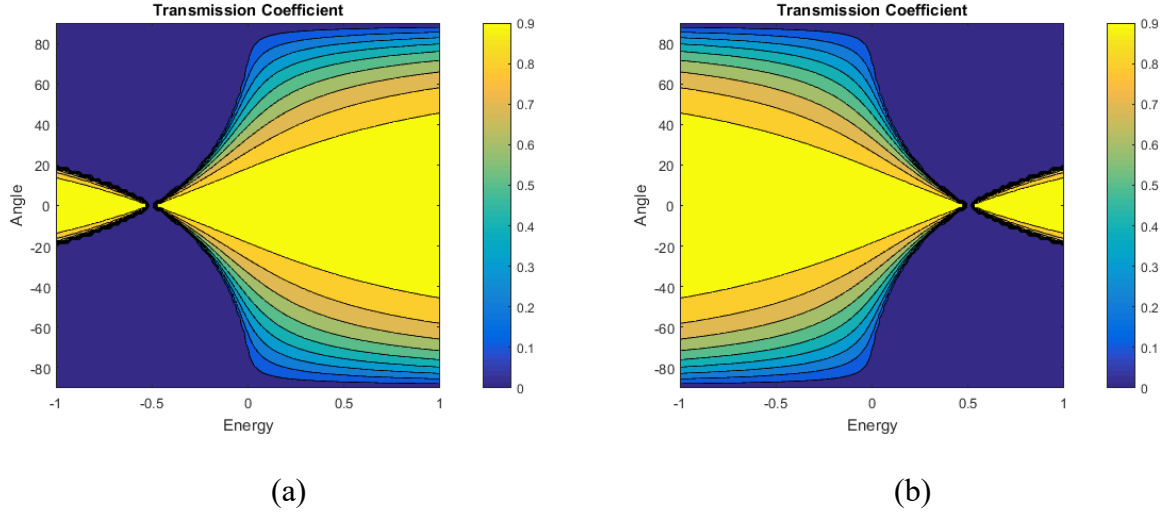


Figure 4.4 Transmission coefficient when crossing abrupt barrier of between  $E_{D_1} = 0.5$  eV and  $E_{D_2} = -0.5$  eV. (a) from region 1 to region 2, and (b) from region 2 to region 1.

### 4.3. Performance Limitations

#### 4.3.1 Lead Resistance

The transmission coefficient across the interface is used for calculating the interface resistance using the Landauer-Büttiker formalism [226]–[228]. However, the asymmetry is controlled by the total resistance of the device in the forward and reverse directions. The metal-graphene contact resistance, and the lead resistance of the graphene ribbon to the interface adds up to the resistance of the device in both directions and reduces the total resistance difference, and asymmetry of the device.

For example, Figure 4.4 shows that maximum asymmetry occurs when the Fermi level of the device causes one of the sides to be intrinsic. However, this causes the lead resistance of that section to be maximum, which can impact the overall asymmetry of the device. In summary, the lead resistance is an important factor that can limit the overall performance of the device.

### 4.3.2 Thermal broadening of energy distribution

The transmission coefficient is a strong function of both the angle of incidence and energy of charge carriers. The thermal broadening of the Fermi-Dirac distribution at non-zero temperature means that a region of energies around the Fermi level take part in conduction[226]–[228]. As such, the total asymmetry depends on the energy thermal broadening. For example, if the device is biased to make one of the sides intrinsic, as the temperature increases, more charge carriers with non-zero transmission ratio take place in conduction, reducing the asymmetry of the interface resistance.

### 4.3.3 Momentum Distribution Smearing by Scattering

Charge carriers in graphene are subject to many mechanisms of scattering[19], [20], [24]–[27], [29], [30], [32], [35], [39], [41]–[43], [46], [48], [49], [56], [62], [66], [67], [79]–[81], [83], [87], [89], [129]–[133], [135], [137], [138], [141], [146], [147], [167], [175], [229]–[240]. Scattering smears the angular distribution of charge carriers[63], [241]–[244]. The angular distribution smearing should be included used in the Landauer-Büttiker to include the effect of such smearing. Accordingly, the Landauer-Büttiker equation for the interface conductance be written as:

$$G = \frac{2q^2}{h} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} d\theta \int_{-\infty}^{\infty} dE T(E, \theta) M(E) \left( -\frac{\partial f_{FD}(E)}{\partial E} \right) P(\theta, E) \quad (4.4)$$

Where  $T(E, \theta)$  is the transmission probability,  $M(E)$  is the number of conduction modes,  $f_{FD}(E)$  is the Fermi-Dirac distribution, and  $P(E, \theta)$  is the momentum smearing angular distribution function of the carriers.

This smearing function will cause more angles to take part in the conduction at the interface, which will noticeably increase the conduction of the interface in the reverse direction, reducing the asymmetry of the device.

Unfortunately, there are no analytical expressions for the momentum angular distribution, but it can be obtained using Monte Carlo simulation[63], [241]–[244]. Equation (4.4) highlights the profound effect scattering has on the performance devices relying on the photon-like properties of graphene charge carriers to achieve conduction asymmetry.

## 4.4. Measurement Results

We fabricated 20 diode devices using CVD graphene on SiO<sub>2</sub>, following the same procedure given in Appendix B. The devices were fabricated with 4 oblique angles: 20°, 30°, 45° and 60°, with 5 devices fabricated at each angle. The measurements were performed using a setup similar to that shown in Appendix C. Figure 4.5 shows a false color SEM image of one of the fabricated devices with an oblique angle of 45°. We will report the asymmetry for the devices by fitting the measurements with a constant forward and backward conduction resistances and use their ratio as the asymmetry. This helps us obtain a statistical average for the measurements and simplifies the performance analysis of multiple devices, and facilitates assessing the behavior of the graphene channel and interface only. An example of the measurement results is shown in Figure 4.6, highlighting the device asymmetry.

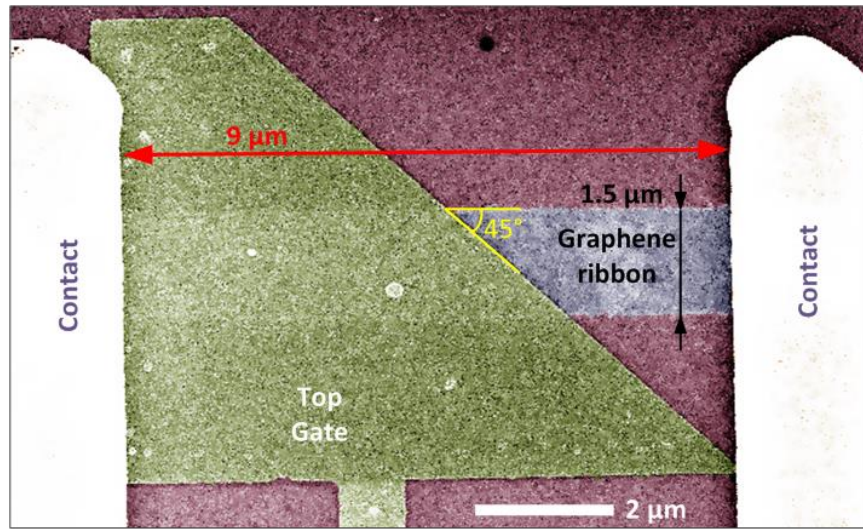


Figure 4.5 False color SEM image of one of the fabricated diode devices with a 45° oblique top gate.

We used the ratio of the backward to forward conduction resistance as a measure of device asymmetry, before and after de-embedding the contact resistance. The measurements shown in Figure 4.7 shows that the highest resistance asymmetry to an oblique angle of 45°. After contact resistance de-embedding, the mean asymmetry at 45° is 1.65, and the smallest mean asymmetry was 1.47 at an angle of 30°. Interestingly, the asymmetry is a weak function of the gate angle.

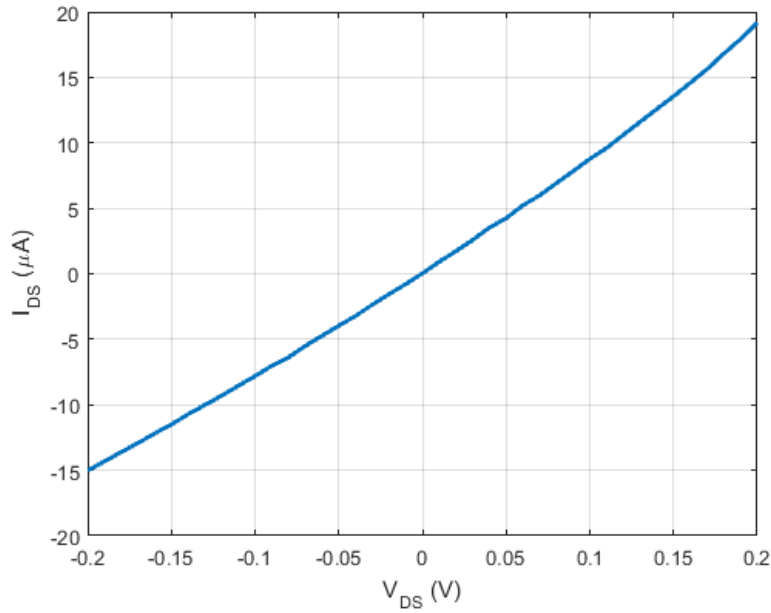


Figure 4.6 Measured I/V characteristics of oblique-incidence diode with a 20° oblique gate. The asymmetry is defined by fitting a constant forward conduction resistance for the range of  $V_{DS} > 0$ , and a constant backward conduction resistance for the range of  $V_{DS} < 0$ , and using their ratio to define the asymmetry. The measurements were performed at a back gate voltage of 10 V and a top gate voltage of -0.1 V yielding an asymmetry of 1.33. The back gate/top gate oxide was 285/10 nm SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> respectively.

The weak dependence of the asymmetry on the gate angle can be attributed to the smearing of the angular distribution of the carriers, distributing the incidence angles of the carriers over a broad range of angles. This angular broadening seems to be wide enough to smear the differences in angle over the range of the fabricated devices to the point of smearing out any trend.

In addition, the proposed diode outperforms the asymmetry of geometric diodes fabricated with either CVD or exfoliated graphene. This can be attributed to the effectiveness of oblique barriers in creating conduction asymmetry compared to apertures. The higher asymmetry however comes at the expense of adding an extra gate, which is not required in geometric diodes. The added gate control terminal is not necessarily a problem, and paves the road for oblique diodes to implement graphene PN junction multiplexers and logic[218]–[220], [222], [223], [245].

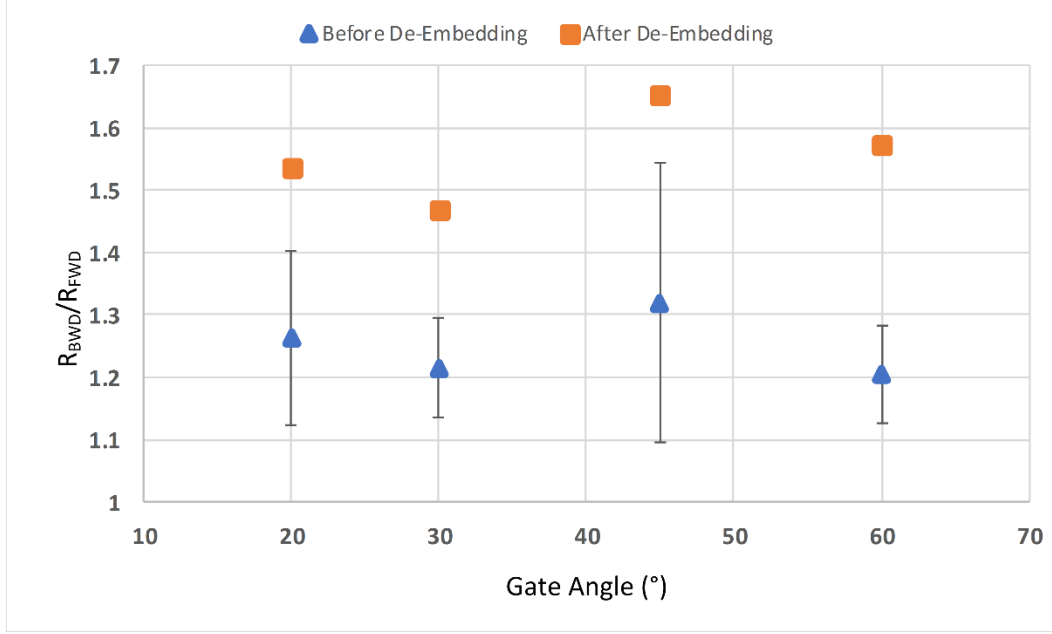


Figure 4.7 Extracted resistance ratio between the backward and forward conductions for each oblique gate angle. The error bars represent the standard deviation of the data. The orange squares are for the data after de-embedding the contact resistance, while the blue triangles show it before de-embedding.

## 4.5. Conclusion

Oblique incidence diodes outperform geometrical diodes in terms of the asymmetry. The added asymmetry comes at the expense of adding an extra terminal, making the oblique incidence diodes a 3-terminal device. The added terminal adds to the functionality of the device, allowing it to be used to implement graphene PN junction multiplexers and logic. The largest asymmetry was obtained for a gate angle of 45°.

Quantitatively, the asymmetry numbers have a large spread and a low mean, and need to be improved for the devices to be application worthy. The major culprit in limiting the asymmetry is the scattering, which smears the angular distribution of the carriers incident on the gate to the point of smearing the differences in angles from 20° to 60°. Higher performance might be achievable using better channel and dielectrics. For example, using exfoliated graphene encapsulated by hBN would reduce the scattering, achieve ballistic transport over a larger mean free path[238], [246]–[249], which could potentially yield higher asymmetry.

## 5) Diffusive-Transport Graphene Couplers

The similarity between the dispersion relation of photons and charge carriers in graphene appeals to designing optics-inspired electronic devices. An interesting optics-inspired analog is the electronic directional coupler. Optics directional couplers allow coupling light between two branches, where the coupling coefficient varies periodically with the coupling distance[250]. The electronic wave modes in graphene ribbons and the resistive coupling between graphene ribbons in close proximity has been analyzed for ballistic transport [30], [48], [251]. The problem of analyzing resistive coupling in diffusive graphene ribbons is different from that in ballistic graphene ribbons. The successive scattering events randomize the wavefunction phase information [226]–[228] prohibiting the direct application of the coupled-mode theory. A direct consequence of this phase randomization is losing the spatial periodicity of the coupling coefficient predicted in ballistic devices.

Modeling of resistive coupling is crucial for deeply scaled interconnects, in which transport will inadvertently be diffusive due to line-edge roughness[130], [137], [252]. Graphene interconnects in close proximity have been studied previously to evaluate their losses and cross-talk performance [253]–[259]. Prior work focused on analyzing the delay and energy metrics of a single graphene interconnect, accounting only for the capacitive coupling among interconnects and resistive losses along the interconnect.

While capacitive coupling and cross-talk have a profound effect on signal integrity for high-frequency signals, especially for deeply scaled interconnects [253]–[259], resistive coupling has a detrimental impact on low-frequency signal integrity. The impact of resistive coupling in CMOS is negligible due to the good insulation properties of inter-layer dielectrics [260] and the large impact of capacitive coupling on signal integrity. Accordingly, it is important to reassess the impact of resistive coupling on the performance of graphene interconnects, due to the different geometric structure, capacitive coupling behavior [253]–[259], and tunneling mechanisms compared to CMOS[261], [262].



In this chapter, we study the coupling between graphene ribbons operating in the diffusive transport regime. We start by developing an analytical model for the coupling resistance between two graphene ribbons separated by a dielectric, highlighting the impact of different fabrication non-idealities on the coupling. We then evaluate the spatial dependence of the coupling coefficient, showing its monotonic saturating behavior, and assess the impact of such coupling on the performance of deeply scaled interconnects.

## 5.1. Modeling Diffusive-Transport Current Coupling

An electronic current coupler consists of two graphene ribbons in close proximity as shown in Figure 5.1. The phase incoherence associated with diffusive transport devices prohibits the direct application of coupled mode theory to evaluate the coupling between two coupled graphene ribbons. A more direct approach would be to model the coupling using the tunneling resistance between the two branches of the coupler; this emphasizes the diffusive nature of the transport and the lack of phase coherency in the associated wave functions.

The modeling of the tunneling resistance between the two graphene ribbons must take into account the difference in energy dispersion relations across the tunneling barrier. The energy dispersion relation of charge carriers changes from a linear dispersion relation in graphene, to a parabolic dispersion relation with an energy gap in the oxide regions, as shown in Figure 5.2. The lack of states in the dielectric energy gap translates to decaying wavefunctions from the graphene ribbons on either side of the dielectric. In other words, despite the linear energy dispersion relation of graphene, the lack of states in energy gap region of the parabolic dielectric gives rise to a decaying wavefunction, reminiscent of tunneling in parabolic bandstructure systems.

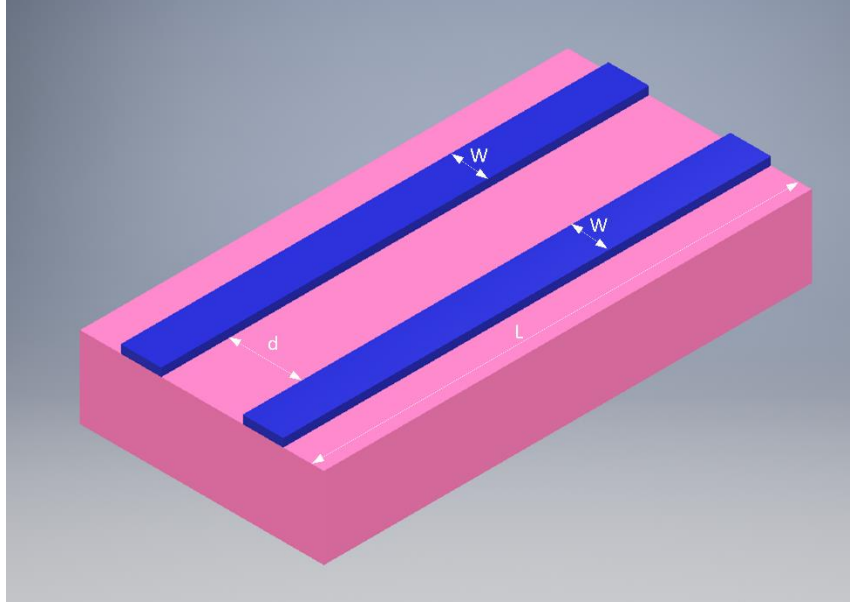


Figure 5.1 Schematic representation of an electronic graphene coupler. The ribbons are spaced by a distance  $d$  apart, over a length of  $L$ , while each ribbon has a width of  $W$ . The graphene is shown in blue while the surrounding oxide is shown in pink. The oxide is only shown below the graphene ribbon for clarity.

The calculation of the tunneling resistance is based on the analysis of Graphene-Insulator-Graphene (GIG) junctions[261], [262]. The major difference between the prior work on GIG junctions and the current problem is that in this device tunneling occurs between the edges of the graphene ribbons rather than between the surfaces of the graphene sheets. The edge tunneling nature modifies the results presented in [261], [262] slightly, but follows its essence otherwise. We defer the estimation of the tunneling resistance to Section 5.3, but stress on the fact that it is a tunneling resistance whose value is very large compared to the ribbons' resistance; its value is limited by how close the two ribbons can be spaced apart, and for all practical purposes, this tunneling resistance value is significantly larger than the resistance of the graphene ribbons. This observation will prove useful when analyzing the electrical model of the device.

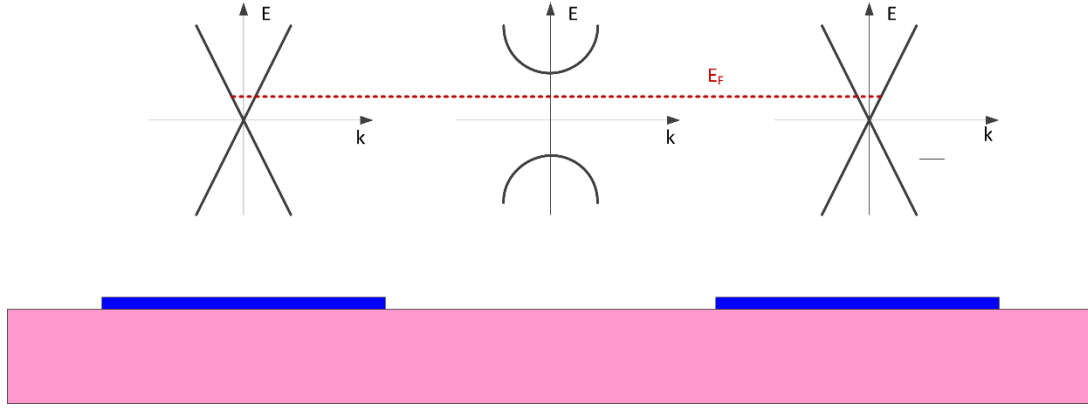


Figure 5.2 Cross-section of the graphene coupler with the bottom oxide shown for clarity. The electronic energy dispersion relation for each region is shown above it with the Fermi level depicted by the dotted red line; it is linear in each graphene region and parabolic with a band gap in the dielectric surrounding them. The energy gap in the parabolic region is significantly larger than the energy of charge carriers in each graphene ribbon.

The electrical model of the device is composed of three distributed resistors: a distributed resistor for each of the graphene ribbons with a distributed tunneling conductance connecting them together, as shown in Figure 5.3. We label one of the ribbons as the input ribbon, and the other as the output ribbon. For this analysis, we apply a current stimulus at the input ribbon and calculate the output current at the other end of each ribbon.

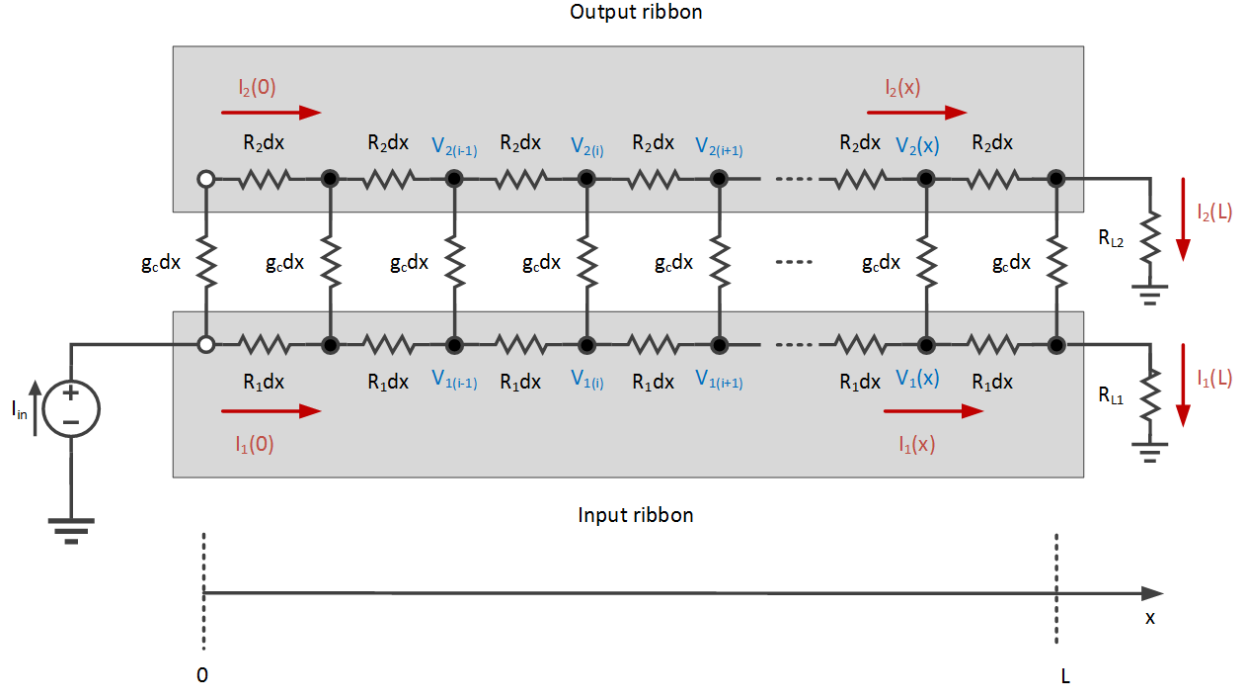


Figure 5.3 Electrical model of graphene coupler. The graphene ribbons are modelled using two distributed resistors with a resistance per unit length of  $R_1$  and  $R_2$ , and the tunneling resistance coupling them is modelled using a distributed conductance with conductance per unit length  $g_c$ .

The coupling coefficient between the current in the two ribbons is defined as the ratio between the output ribbon and input ribbon branch currents as:

$$C_I(x) = \frac{I_2(x)}{I_{in}} \quad (5.1)$$

A detailed analysis of the electrical model and a derivation of the coupling coefficient is provided in Appendix D. The current distribution and coupling are a strong function of the load at the output of each branch. This is expected due to the passive nature of the device that does not provide any buffering. Throughout this chapter, we assume that the ratio of the two loads matches the ratio of the ribbons' resistance per unit length, that is  $\frac{R_{L1}}{R_{L2}} = \frac{R_1}{R_2}$ . A more general analysis can be found in Appendix D.

Under the matching load condition, we can approximate the current distribution in each branch of the coupler as:

$$\begin{aligned}
I_1(x) &\approx \frac{I_{in}}{R_2 + R_1} \left( R_2 + R_1 e^{\frac{-x}{L_c}} \right), \\
I_2(x) &\approx \frac{I_{in} R_1}{R_2 + R_1} \left( 1 - e^{\frac{-x}{L_c}} \right)
\end{aligned} \tag{5.2}$$

where  $L_c^{-1} = \sqrt{g_c(R_1 + R_2)}$ .

## 5.2. Dependence Current Coupling Coefficient on Coupling Distance

Under the condition of matching load ratios,  $\frac{R_{L1}}{R_{L2}} = \frac{R_1}{R_2}$ , the current coupling coefficient is:

$$C_I(x) = \frac{I_2(x)}{I_{in}} = \frac{R_1 \left( 1 - e^{\frac{-x}{L_c}} \right)}{R_2 + R_1} \tag{5.3}$$

In the limiting case where  $L \gg L_c$ , Equation (5.3) reduces to:

$$C_I(L) \approx C_I(\infty) = \frac{R_1}{R_1 + R_2} \tag{5.4}$$

Equations (5.2), (5.3) and (5.4) provides a very intuitive way of explaining the behavior of the diffusive-transport coupler: given enough length, the coupler will divide the current by the ratio of the resistances of the two branches, just as if they shorted only at the input end. Unlike the ballistic-transport coupler or the optical directional coupler, the coupling coefficient does not show any periodicity on the coupling coefficient. The lack of coupling coefficient periodicity is due to the loss of the phase information due to successive scattering associated with diffusive transport. The diffusive-transport coupler rather acts as a current divider that divides the current with according to the ratio of the two branch resistances. However, rather than being an ideal current divider, the current division takes places over a special distance dictated by the characteristic length  $L_c^{-1} = \sqrt{g_c(R_1 + R_2)}$ , which is a function of the ratio between the coupling and branches conductance.

An example of the spatial variation of the current coupling coefficient and the voltage across the branches of a balanced coupler is shown in Figure 5.4 as obtained using SPICE simulations.

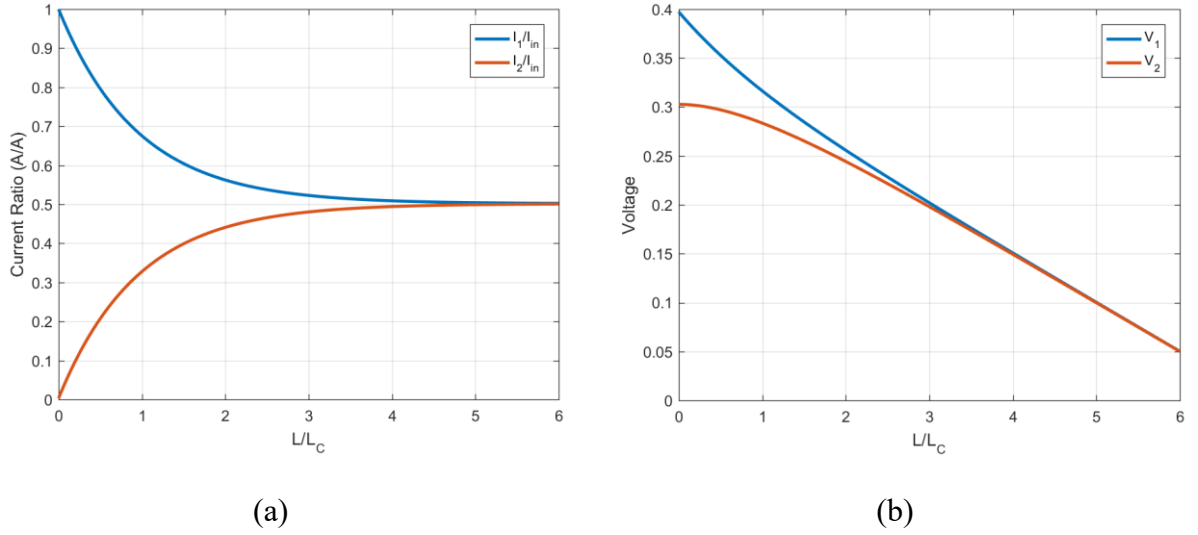


Figure 5.4 (a) Spatial variation of the current and (b) Spatial variation of the voltage across a balanced coupler. The simulations were performed using SPICE over a discretized model comprised of 1000 sections.

### 5.3. Estimation of the tunneling resistance

The tunneling resistance can be estimated using the Bardeen Hamiltonian approach as in other Graphene-Insulator-Graphene junctions [261], [262]. The tunneling current evaluated using the Bardeen Transfer Hamiltonian [261], [262] is given as:

$$I = g_v g_s \left( \frac{2\pi e}{\hbar} \right) \sum_{\alpha, \beta} |M_{\alpha\beta}|^2 [f_i(E_\alpha) - f_o(E_\beta)] \delta(E_\alpha - E_\beta) \quad (5.5)$$

Where  $g_v$  is the valley degeneracy factor (2 in graphene),  $g_s$  is the spin degeneracy factor ( $g_s = 2$ ),  $M_{\alpha\beta}$  is the tunneling matrix element,  $\alpha$  and  $\beta$  are all the states in the electrodes in between which tunneling occurs,  $f_i$  and  $f_o$  is the Fermi Dirac distribution in the input and output electrodes respectively, and  $E$  is the energy of the state. The matrix element is given as:

$$M_{\alpha\beta} = \frac{\hbar^2}{2m} \int dS \left( \Psi_\alpha^* \frac{d\Psi_\beta}{dr} - \Psi_\beta^* \frac{d\Psi_\alpha}{dr} \right) \quad (5.6)$$

Where  $\hbar$  is the reduced Planck constant,  $m$  is the free-electron mass,  $\Psi_i$  is the wavefunction of state  $i$ ,  $r$  is the direction of tunneling current flow and the integral is performed on a plane

midway between the two tunneling electrodes. The matrix element in the case of graphene electrodes is given in [261], [262] as:

$$M_{\alpha\beta} = \frac{\hbar^2 \kappa}{2mD} e^{-\kappa d} g_{\omega}(\theta_i, \theta_o) \int dS e^{j\vec{Q}\cdot\vec{r}} e^{j(\vec{k}_i - \vec{k}_o)\cdot\vec{r}} \quad (5.7)$$

Where  $\kappa$  is the wavevector of the decaying exponential function inside the parabolic region barrier (also known as the extinction coefficient),  $d$  is the separation between the two tunneling electrodes,  $D$  is the wavefunction normalization constant,  $g_{\omega}(\theta_i, \theta_o)$  is a scaling factor in the order of unity that accounts for the wave vector misalignment between the overlapping tunneling wavefunctions,  $\vec{Q}$  is the misalignment vector with an angle  $\omega$  similar to the  $\omega$  in  $g_{\omega}(\theta_i, \theta_o)$  accounting for rotational misalignment between the tunneling bands, and  $\vec{k}_i$  and  $\vec{k}_o$  is the wavevector between the input and output electrodes. In low-field transport in graphene, the wavevector of the charge carriers taking part in tunneling is close to the Dirac points ( $\vec{K}$  and  $\vec{K}'$ ).

The lateral tunneling and the use of lithography to form the junction requires some modifications to tunneling matrix element that significantly simplify its analysis:

1) Lithography creates rough edges. An example of the edge roughness of metal lines obtained when creating metal lines using PMMA photoresist is shown in Figure 5.5. The edge roughness standard deviation is 3 nm and there is no correlation between the edges. As such, the tunneling distance ( $d$ ) and corresponding tunneling resistance is a random variable, and the differential equations used to describe the transport in the electrical model should replace a constant  $g_c$  with a random variable  $g_c(x)$ , converting Equation (D.1) into a set of coupled stochastic differential equation. This level of detail is only required when the edge roughness represents a considerable portion of the ribbon width or ribbon spacing, and should be kept in consideration when developing statistical models for the coupler. When the roughness of the edge is small relative to the ribbons separation or the width of each ribbon, using the average separation distance to derive a single constant value for tunneling conductance ( $g_c$ ) is enough.

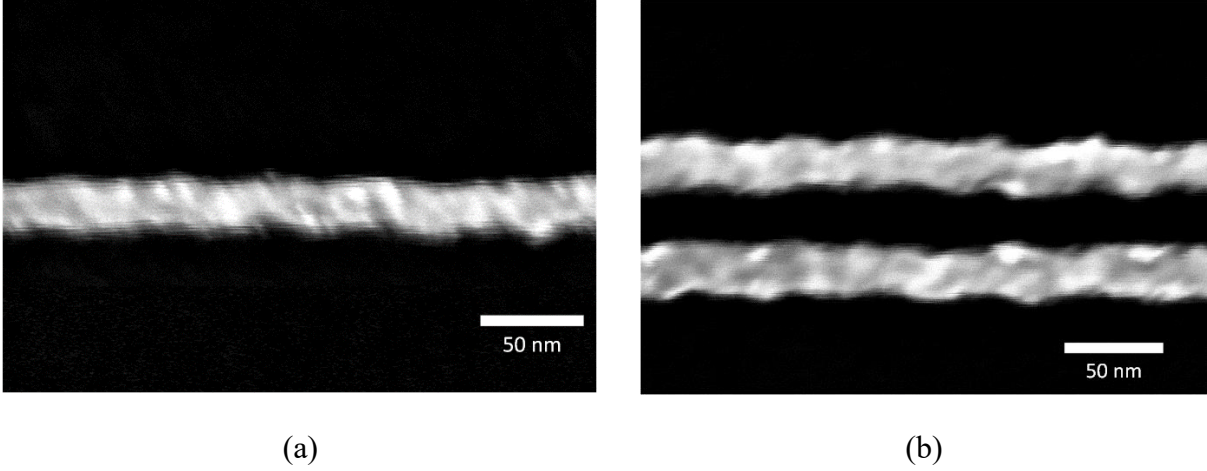


Figure 5.5 SEM images of 25 nm metal lines created using PMMA photoresist. The images show an edge roughness standard deviation of 3 nm and the lack of correlation between edges in close proximity; (a) single metal wire, and (b) two metal wires with a separation of 25 nm.

2) In this device, tunneling is from a 1D edge to the opposite 1D edge across a 2D barrier, not from a 2D surface of a graphene sheet to another across a 3D barrier. The tunneling probability across a 2D barrier falls exponentially away from the normal connecting the two closest points across the barrier. As such, a 1D model is suitable to describe the tunneling probability between the edges. In the 1D model the tunneling probability is:

$$M_{\alpha\beta} = \frac{\hbar^2}{2m} \left( \Psi_{\alpha}^* \frac{d\Psi_{\beta}}{dr} - \Psi_{\beta}^* \frac{d\Psi_{\alpha}}{dr} \right) \Big|_{x=\frac{d}{2}} \quad (5.8)$$

Where  $x = d/2$  is a point midway the 2D barrier assumed to be in the x direction.

3) The two branches of the coupler are fabricated from a single CVD graphene sheet over  $\text{SiO}_2$  with a single common back gate. Since the devices are in close proximity, their Fermi level should be closely aligned. However, the surface roughness of the substrate will cause the formation of charge puddles, which causes random shifts in the Fermi level, and the barrier height, across the graphene ribbons. Our first order estimate will neglect these charge puddles and assume Fermi level alignment, but a more elaborate analysis should account for charge puddles and roughness.

4) The region between the two branches of the coupler is typically composed of an oxide. The effective mass in the oxide should be taken into account when calculating the tunneling matrix element, not the free-electron mass.



5) The tunneling resistance is a function of the Fermi level separation between the two ribbons, which is a function of the potential different between them. The voltage drop between the two ribbons is small, thus the variation of tunneling resistance due to the spatial variation of the Fermi level difference can be neglected. This is further justified by the fact that we are interested in the low-field transport phenomena occurring across lithographically defined barriers (roughly  $\geq 10$  nm apart), a condition under which electrode charging occurs.

Taking the above points into consideration we can rewrite the tunneling current in the low-field transport regime at  $T=0$  K as:

$$I = 2\hbar \left( \frac{e}{mv_f} \right)^2 (\kappa e^{-\kappa d})^2 u_N V \quad (5.9)$$

Where  $u_N$  is a constant in the order of unity that captures the effects of misalignment and normalization constants (it has the units of  $m^{-1}$ ), and  $V$  is the applied voltage. The extinction coefficient in this case is given as:

$$\kappa = \sqrt{\frac{2m}{\hbar^2} (\phi_G - E_f - \chi_{\text{SiO}_2})} \quad (5.10)$$

Where  $\phi_G$  is graphene's work function,  $E_f$  is the ribbon's Fermi level, and  $\chi_{\text{SiO}_2}$  is the electron affinity of  $\text{SiO}_2$ . Equation (5.4) yields the tunneling current per unit length of the ribbons in the low field transport regime. The conductance per unit length of the ribbon is thus given as:

$$g_c = 2\hbar \left( \frac{e}{mv_f} \right)^2 (\kappa e^{-\kappa d})^2 u_N \quad (5.11)$$

Evaluating Equation (5.11) without the constant  $u_N$  to estimate the order of  $g_c$  and the extinction factor  $\kappa$ , we find it is a strong function of the separation distance  $d$  and weak function of the ribbon's Fermi level  $E_F$  as shown in Figure 5.6.

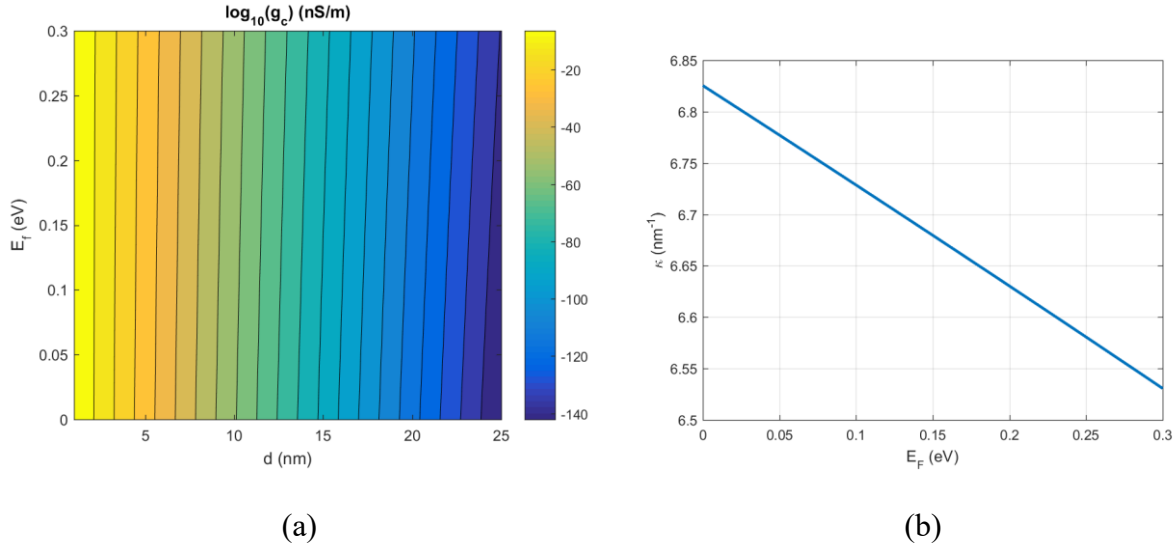


Figure 5.6 (a) Logarithm of tunneling coupling conductance ( $\log_{10}(g_c)$ ), and (b) Extinction coefficient ( $\kappa$ ) while varying the Fermi level from 0 to 0.3 eV and the separation distance from 1 to 25 nm.

The numbers obtained show that the coupling is extremely weak. This is due to the use of a non-resonant tunneling device [261], [262]. In addition, with the separation distances achievable in the order of 10 nm, the extinction of the coupling wave function is very weak to yield appreciable coupling ( $\sim 10^{-70}$  nS/m). This translates to a very large, impractical, coupling characteristic length, which means that the device operates essentially as two independent ribbons.

#### 5.4. Impact of Current Coupling on Deeply Scaled Interconnects

Resistive coupling between neighboring interconnects is a hazard to signal integrity. From our analysis, resistive coupling will not impact deeply scaled graphene interconnects till the spacing between them falls well below 5 nm. However, care should be taken when discussing the limits on stacking graphene interconnects [21], [253], [255]–[259], [263]. Resonant-tunneling [261], [262], can play a significant role in the engineering of graphene interconnects.

Resonant tunneling between neighboring interconnects would increase the coupling conductance and cause resistive leakage of current among neighboring interconnects. and should be prevented if the interconnects do not belong to the same route.

Similarly, resonant tunneling can be used to reduce the overall interconnect resistance. It can be used to reduce the overall resistance of a stacked, multi-layer graphene interconnect, where the layers belong to the same route and carry the same signal. The large coupling distributed conductance will help shunt the resistance of each layer and reduce the overall resistance.

In addition to resonant tunneling, the role of non-resonant tunneling in CVD graphene interconnects should not be underestimated. In CVD graphene ribbons with multiple grains of different orientations, the non-resonant tunneling can contribute significantly to resistive coupling[261], [262].

Proper design of stacked graphene interconnects, or different graphene-metallization layers in multi-layer graphene chips should take into account the resonant stacking constraints. If two ribbons are routed normal to each other on successive graphene-metallization layer (Manhattan Routing), the spacing between the layers should be carefully chosen to prevent resonant tunneling as long as they carry independent signals.

## 5.5. Conclusion

A graphene-insulator-graphene electronic coupler operating in the diffusive-transport regime does not show a periodic dependence on the coupler length, unlike ballistic-transport couplers. Diffusive-transport coupler show an asymptotic, monotonic dependence of the coupling coefficient on the coupling length due to the loss of wavefunction phase information by successive scattering events.

Diffusive-transport graphene couplers are not practically viable without creating a resonant tunneling structure. Otherwise, the tunneling-based coupling conductance between the graphene ribbons will be too small to yield any practically significant effect.

The analysis of the graphene coupler shows that graphene interconnects are highly scalable laterally, where resistive coupling will not be effective even when the inter-ribbon spacing falls below 5 nm. However, care should be taken when stacking graphene interconnects to prevent resonant tunneling between independent routes when using multi-layer graphene interconnects.

Similarly, resonant tunneling can be used in multi-layer graphene interconnects to reduce the overall interconnect resistance, where a low inter-layer coupling conductance would reduce the overall resistance of the interconnect.

## 6) Current Technological Limitations on Graphene Devices and Circuits

The performance of graphene FETs and devices is hampered by numerous technological limitations. In this chapter, we discuss the technological limitations limiting the electrical performance of graphene FETs. We focus on electrical and thermal interface contact resistance, the evolution of stress in dual-gated graphene FETs, and the impact of photoresist chemistry, specifically metal-ion content, on the performance of graphene FETs.

### 6.1. Contact Engineering

Graphene FET architectures typically utilize top contacts to graphene sheets as shown in Figure 6.1. Although not as good as edge contacts[249], they are simpler to fabricate. Contacts play an important role in the device's performance. In this section, we discuss the current limitations in terms of electrical contact resistance and thermal interface resistance of metal-graphene contacts, and how they affect the performance of a graphene FET.

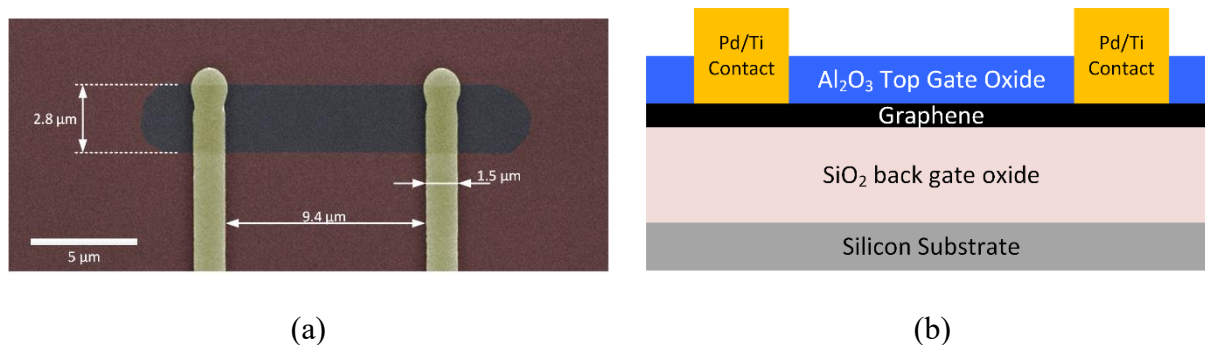


Figure 6.1 (a) False Color SEM image, and (b) Cross-section of a typical graphene FET. The top gate oxide is used to passivate the device against environmental effects when used or exposed to air.

### 6.1.1 Electrical Resistance

Electrical contact resistance between metal and graphene has been studied extensively. Different contact models differ in the complexity and accuracy[45], [50], [54], [88], [93], [94], [102], [109], [113], [115], [122], [127], [128], [264], [265]. Experimental measurements of contact resistance to graphene are marred by many non-idealities, such as low adhesion of the contact metal to graphene, and a perceived negative contact resistance due to the metal contact doping the graphene region around it[266]. The use of circular TLM structure helps in mitigating adhesion issues due to the large surface contact area[126], [267]. The metal doping graphene around the contacts due to the finite density of states of graphene has been predicted theoretically[54], [57], [94], [100], [109], [112], [118], [119], [123], [128], measured experimentally[62], [94], [95], [102], [112], [115], [117], [121], [146], and its impact on the interpretation of experimental data evaluated[266].

The proper choice of a metal contact to graphene involves a compromise between finding a metal that adheres well to graphene, but does not damage its electrical through excessive interaction[45], [50], [91], [93], [94], [100], [109], [112], [115], [116], [118], [120], [122], [123], [127], [128]. Palladium and nickel have been identified as the metals with lowest contact resistance with graphene[50], [88], [91], [94], [105], [112], [120], [122], [126], [128], [268], with Pd giving lower contact resistance results. The low adhesion of Pd to graphene necessitates the use of an adhesion layer. Titanium and chromium has been both commonly used as adhesion layer materials[93], [103].

To compare Ti/Pd vs Cr/Pd stacks, we fabricated 25 devices of each and fitted it to the constant mobility model[87], which provides a single value for the contact resistance. The fabrication procedure is similar to that outlined in Appendix B, without the top-gate metal deposition. The devices are similar to those shown in Figure 6.1, and were fabricated using CVD graphene on SiO<sub>2</sub>. We found that titanium consistently gives lower contact resistance, with less spread in statistical data; a box plot of the fitted data is shown in Figure 6.2.

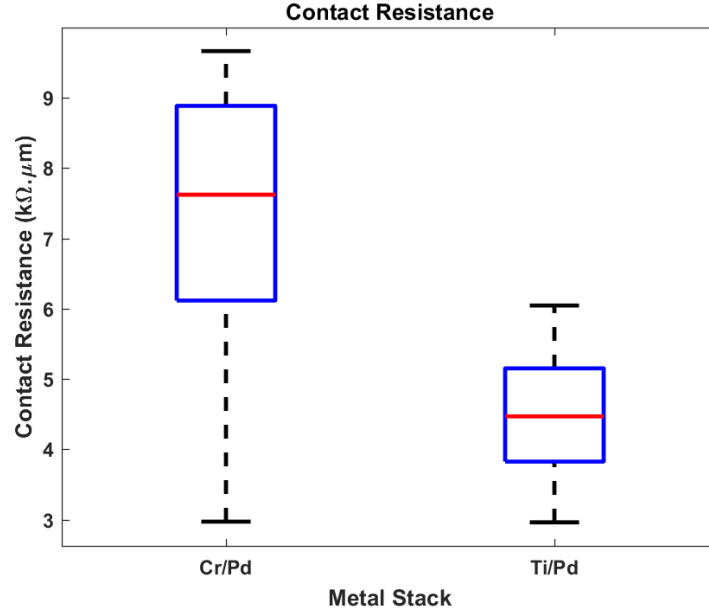


Figure 6.2 Box plot of extracted contact resistance value for Cr/Pd and Ti/Pd metal stacks. The layer thickness was 1.5/40 nm for each stack. The data analysis was performed using measurements from 25 devices for each metal stack. The box plot whisker edges correspond to the extreme data points, the blue box limits correspond to the 75% and 25% percentile points and the red horizontal line is the median of the data. The results show the the Ti/Pd stack shows less spread and lower contact resistance compared to Cr/Pd.

The spread in Ti/Pd and Cr/Pd can be attributed to the formation of metal oxides at the adhesion layer/graphene interface[126]. The lower spread and median in Ti/Pd points towards less oxidation of Ti in our process relative to Cr. The spread of the data and the dependence of the stack contact resistance on the metal deposition conditions elucidates the importance of fully reporting the deposition conditions. When reporting contact resistance measurement data, deposition system-dependent characteristics (deposition rate, deposition pressure, purity of the metal source) can have a profound effect on the reported data. This sensitivity can lead to unreliable or contradicting results if the deposition condition are not highlighted [28], [97], [102], [112], [116], [117], [120], [122], [126], [128].

### 6.1.2 Thermal Interface Resistance

The thermal interface conductance of the contacts on graphene play a crucial role in allowing heat to flow out of the device; combatting performance limiting thermal effects from operational Joule heating. Figure 6.3 shows a simplified contact thermal circuit depicting how Joule heating

affects the temperature of the channel. Figure 6.3 is valid when a doped graphene FET is operating in the low-field transport regime, causing a negligible amount of Joule heating inside the channel. This model is different from the high-field transport models, where the Fermi level spatial variation can cause the formation of a hot spot inside the channel at the position of the charge neutrality point[107], [269]–[271].

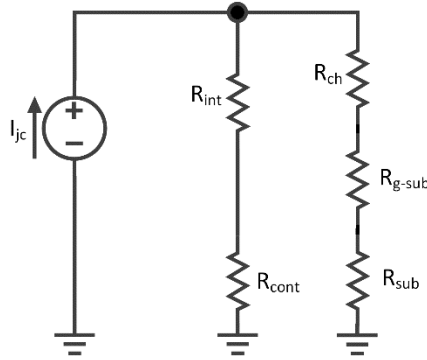


Figure 6.3 A simplified thermal circuit showing how heat flux generated by Joule heating distributes into the channel and the contact. The thermal current  $I_{jc}$  is the heat current generated due to Joule heating at the metal-graphene interface ( $I_{jc} = I_e^2 R_C$ ), where  $I_e$  is the electrical current flowing through the contact and  $R_C$  is the electrical contact resistance.  $R_{int}$ ,  $R_{cont}$ ,  $R_{ch}$ ,  $R_{g-sub}$  and  $R_{sub}$  are the thermal resistances of the metal-graphene interface, metal contact, graphene channel, the graphene-substrate interface and substrate, respectively. All the grounds shown are thermal grounds, representing the temperature of the surrounding.

The heat flux flowing out of the device through the contacts is given as:

$$\begin{aligned}
 I_{ch} &= I_{jc} \frac{R_{int} + R_{cont}}{R_{int} + R_{cont} + R_{ch} + R_{g-sub} + R_{sub}} \\
 &= I_e^2 R_C \frac{R_{int} + R_{cont}}{R_{int} + R_{cont} + R_{ch} + R_{g-sub} + R_{sub}}
 \end{aligned} \tag{6.1}$$

The temperature difference between the channel and the surrounding is given as:

$$\begin{aligned}
 \Delta T_{ch} &= I_{ch} (R_{ch} + R_{g-sub} + R_{sub}) \\
 &= I_{jc} \frac{(R_{int} + R_{cont})(R_{ch} + R_{g-sub} + R_{sub})}{R_{int} + R_{cont} + R_{ch} + R_{g-sub} + R_{sub}} \\
 &= I_e^2 R_C \frac{(R_{int} + R_{cont})(R_{ch} + R_{g-sub} + R_{sub})}{R_{int} + R_{cont} + R_{ch} + R_{g-sub} + R_{sub}}
 \end{aligned} \tag{6.2}$$

The thermal resistance of the metal contact  $R_{cont}$  is typically low due to the high thermal conductivity of metals. We can thus approximate Equation (6.2) as:



$$\Delta T_{ch} \approx I_e^2 R_C R_{int} \frac{(R_{ch} + R_{g-sub} + R_{sub})}{R_{int} + R_{ch} + R_{g-sub} + R_{sub}} \quad (6.3)$$

Equation (6.3) shows that the thermal interface resistance plays a crucial role in determining how much heat flux flows into the channel, causing its temperature to increase. In deeply scaled graphene FETs with lengths less than 0.5  $\mu\text{m}$ , the thermal interface resistance between the graphene and metal contact controls how the generated heat flows: if the thermal interface conductance is low, most of the generated heat flux will flow out through the contact instead of through the channel. For long length devices, most of the heat flows through the graphene-dielectric interface into the substrate[107], [271]. The metal-graphene thermal interface resistance is also important in the high-field transport regime, as it a low thermal interface resistance reduces the amount of temperature rise inside the channel[107].

Thermal interface resistance is a strong function of the interface and bonding between the metal and graphene. The interaction between the metal and the graphene plays a crucial role. Gold, palladium and nickel span the interaction spectrum from no interaction in the case of gold, weak interaction in the case of palladium, and strong interaction forming a carbide in the case of nickel. The corresponding thermal interface conductances vary from 20  $\text{MW/m}^2\text{K}$  for Au, 25  $\text{MW/m}^2\text{K}$  for Pd, and 45  $\text{MW/m}^2\text{K}$  for Ni.

Equation (6.3) highlights the importance of co-optimization of the electrical and thermal-interface contact resistances. The optimization of thermal contact resistance typically involves a proper choice of the metal contact material[110], [272], [273], and co-optimization should focus on the reduction of the electrical and thermal interface resistance product[110].

## 6.2. Stress in dual-gated Graphene FETs during Processing

Stress in thin films is inversely proportional to the thickness of the film, and graphene being single layer, represents the lower limit of thickness. Graphene channels are typically sandwiched between two oxides; the fabrication of graphene FETs usually entails the deposition of a top-gate oxide, whether for use as a top-gate dielectric or for passivation[144], [274]. Even when fabricated

over a single oxide layer, graphene being the lowest thickness element in the stack is the most prone to stress, and stress affects the electronic properties graphene[19], [156], [161].

To study the evolution of stress in graphene during fabrication, we used Raman analysis. We used the 2D peak position as a metric to evaluate the evolution of strain in the graphene channel after each process of fabrication outlined in Appendix B [156], [160], [161], [163], [164], [167], [168], [173], [176]. We evaluated the stress in the graphene channel before processing, after contacting, after ALD seed evaporation and after ALD of the top-gate oxide. We performed the experiment using 3 different photoresist and developer pairs and the results were consistent across all 3 pairs. The Raman analysis was performed on the photolithography defined graphene channel similar to that shown in Figure 6.4. The Raman analysis was performed on data obtained from area scans over the exposed channels.

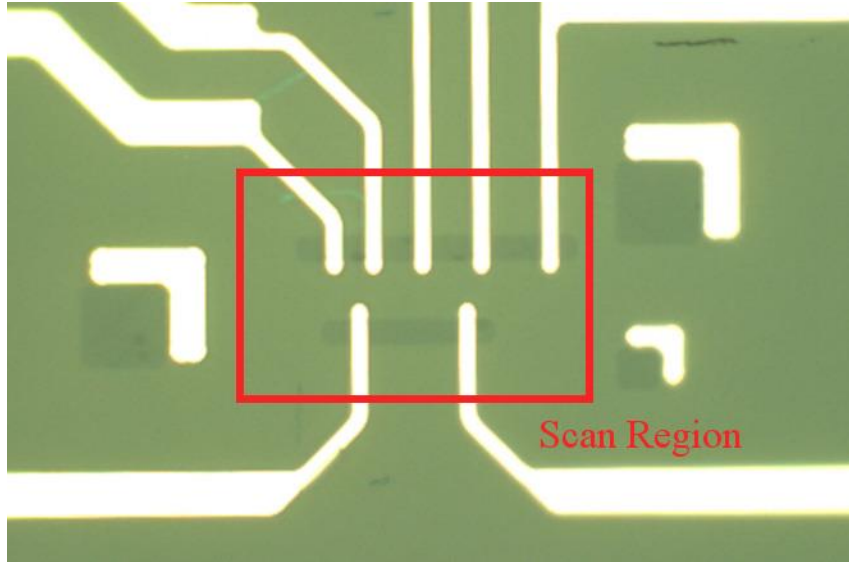


Figure 6.4 Optical microscope image of graphene FET device used to evaluate the stress evolution during fabrication. The graphene channels inside the red box was analyzed using Raman analysis to evaluate the stress during fabrication.

The 2D peak position was used as a metric for the strain in the channel. The 2D red shifts under tensile strain. The exact value of the strain was not calculated from the 2D peak shift due to the different values of the reported shift rates[161], [163], [167]–[169], [173]. The 2D peak position is also a function of doping[75]. We cannot fully decouple the contribution of stress and doping in shifting using only the 2D peak position. However, we will use the ratio of the 2D and G peak intensities to qualitatively estimate the doping incurred during processing.

The Raman spectrum from a single point and an aggregate of the 2D peak position after each fabrication step is shown in Figure 6.5. The single point spectrum shown in Figure 6.5(a) shows that the slight 2D peak red shift occurs after contacting indicating a slight tensile strain of the channel, followed by a distinctive shift in after the  $\text{Al}_2\text{O}_3$  seed layer deposition followed by a return to its original position after the completion of the top gate oxide ALD.

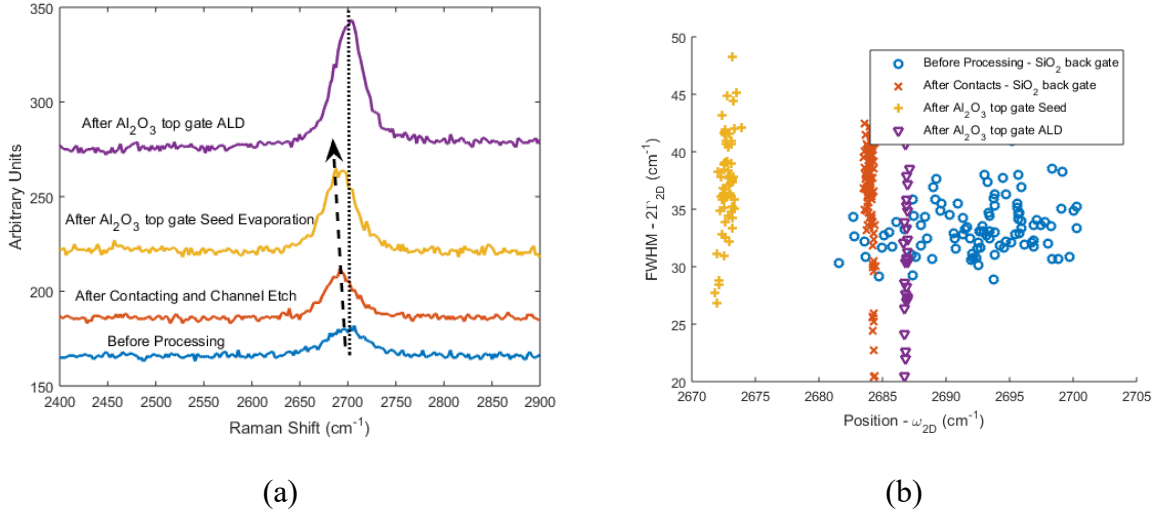


Figure 6.5 (a) Raman spectrum around the 2D peak, (b) 2D peak data aggregate across the graphene channel after different fabrication steps. The arrows in (a) show clarify the evolution of the 2D peak position. The 2D peak position initially redshifts, indicating tensile strain, after contacting. The red shift is maximum after the  $\text{Al}_2\text{O}_3$  seed layer deposition, indicating that this is the process inducing the maximum strain in the graphene channel. The 2D peak position almost moves back to position prior to the seed deposition after ALD. The 2D peak FWHM is not included in the analysis, as it is a weak function of the strain and due to its high sensitivity to impurities and substrate roughness.

The aggregate of 2D peak positions from the scan of the graphene channel shown in Figure 6.5(b) confirms the behavior shown in Figure 6.5(a). Initially, the 2D peak positions are scattered over a range of peak positions due to the roughness of the substrate[75]. Once the channel is contacted the spread of the points reduces significantly. This reduction of 2D peak position can be attributed to the tension in the graphene channel caused by anchoring of the graphene ribbon by the contacts on the ends. After the depositions of the  $\text{Al}_2\text{O}_3$  seed layer (1.5 nm of aluminum left to natively oxidize in air) the 2D peak positions redshift significantly. We speculate that this shift is likely due to the high tension in the graphene between the high-stress thin top oxide and the substrate. Graphene has a negative thermal expansion coefficient unlike  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$  [164], exposing it to a high tensile stress by the thin top oxide seed layer. After the completion of the

ALD, which takes about 1 hour at 150 °C, the peak position almost moves back to its original position, blue shifting by about 3  $\text{cm}^{-1}$ . This can be attributed to the thickness increase of the top gate oxide and the thermal processing causing a reduction in the overall stress in the top gate oxide, and the graphene channel subsequently.

To estimate the role of doping in shifting the 2D peak, we use the ratio of the intensities of the 2D ( $I_{2D}$ ) and G peak ( $I_G$ ) [75], [166]. The ratio  $I_{2D}/I_G$  increases as graphene becomes more intrinsic and is a weak function of stress. As seen in Figure 6.6, the relative invariance of the peaks intensity ratio distribution after the contacting and evaporation of the seed signifies the relatively fixed level of dopants after these two steps. After the ALD of the top gate oxide, the distribution of the peak intensity points shows a slight redistribution towards higher ratios, signifying reduction in doping of the graphene ribbon towards more intrinsic level. However, the extent of the point spread did not change significantly, indicating that the overall doping level of the graphene channel did not change. Accordingly, we rule that the role of doping level change in causing a significant shift in the 2D peak position is negligible.

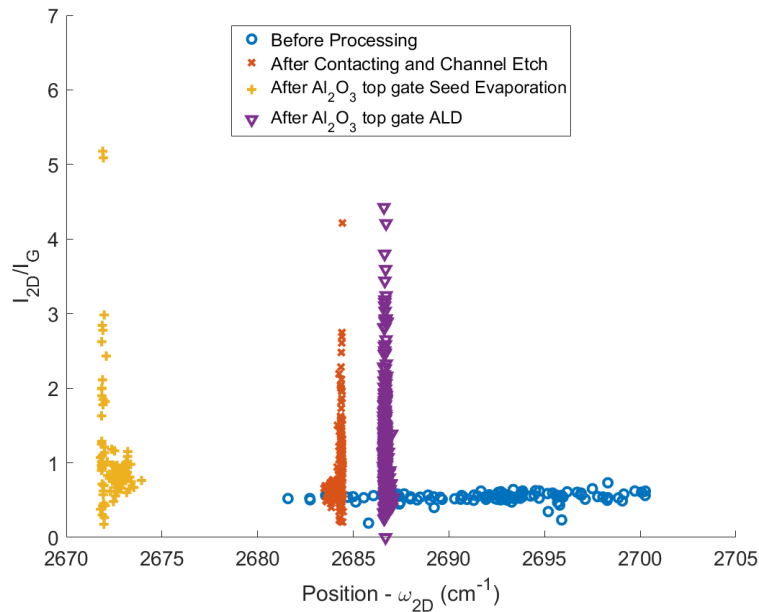


Figure 6.6  $I_{2D}/I_G$  (peaks intensity ratio) versus the 2D peak position ( $\omega_{2D}$ ). As peak position and peaks intensity ratio does not change significantly after deposition of the contact metal and deposition of seed oxide, this signifies a minimal doping change between these two steps.

We cannot ascertain whether the long time anneal or the thickness increase is the cause of stress reduction, but experimenting with different growth times and temperatures could allow the evaluation of the effect of each parameter more accurately.

In addition, we cannot fully ascertain that doping has not a role in shifting the 2D peak position. However, as the graphene channel and edges were subject to n-type dopants after contacting (aluminum causes n-type doping in graphene [100]) we anticipate it to have a small effect due to the relatively small impact of n-type dopants on the 2D peak position[75].

### 6.3. Impact of Metal-Ion Containing Developers on the Performance of Graphene FETs

Photoresist developer chemistries can be divided into metal-ion free and metal-ion containing. The choice of a developer chemistry depends on its compatibility and if it has desirable properties with respect to the fabrication process.

We studied the impact of metal-ion free (MIF) developer and metal-ion containing (MIC) developers on the performance of graphene FET transistors. We used CD26 (TMAH-based developer) as the MIF developer, for use with Shipley S1805 photoresist with LOR3A lift-off layer, and used AZ Developer (Na-based developer) and AZ400K (K-based developer) as MIC developers, for use with AZ4110 photoresist. We fabricated 25 devices using each photoresist using commercial CVD graphene and evaluated the performance of the devices by fitting their characteristics to the constant mobility model[87]. Electrical measurements included a hysteresis sweep of the gate to extract the resulting hysteresis in Dirac point voltage occurring because of interface trapped charges between the graphene and SiO<sub>2</sub> substrate[64], [65], [69]–[71], [73], [76], [77], [104], [144], [274]–[276]. The devices were fabricated using the same steps outlined in Appendix B, but without the top gate metal deposition. The devices were measured using the setup outlined in Appendix C. Each box corresponds to measurements from 25 devices. In all box plot figures in this section, the box plot whisker edges correspond to the extreme data points, the blue box limits correspond to the 75% and 25% percentile points and the red horizontal line is the median of the data.

Figure 6.7 shows the Dirac point voltage obtained using the different developers. The data shows that the MIF CD26 developer yields the lower Dirac point voltage. This is expected as the lack of metal ions in the MIF developer causes less doping compared to the MIC developers, which dope the graphene significantly due to the metal ion content.

The hysteresis of Dirac point voltage shown in Figure 6.8 shows that the MIC developers have the lowest magnitude of hysteresis. This can be attributed to the screening of graphene-dielectric interface charges by the metal-ion dopants, reducing their effect in causing hysteresis.

The extracted charged-ion concentration is shown in Figure 6.9. It confirms that the charged-impurity concentration of MIF developers is considerably less than that obtained using MIC developers. This results is expected, as the more metal ions are essentially charged impurities.

The extracted mobility is shown in Figure 6.10. We note that MIF developers yield significantly higher charge carrier mobility compared to MIC developers. This result can be attributed to the reduction in charged-impurity scattering when using MIF developers as they cause less charged-impurity concentration.

The extracted contact resistance normalized per device width is shown in Figure 6.11. Although the median values are close, the spread is significantly lower when using MIF developers. This indicates a more consistent metal-graphene interface as the contact resistance is a strong function of the state of the metal-graphene interface.

The results conclusively indicate the MIF developers are superior when processing graphene compared with MIC developers, unless the graphene channel is to be doped intentionally.

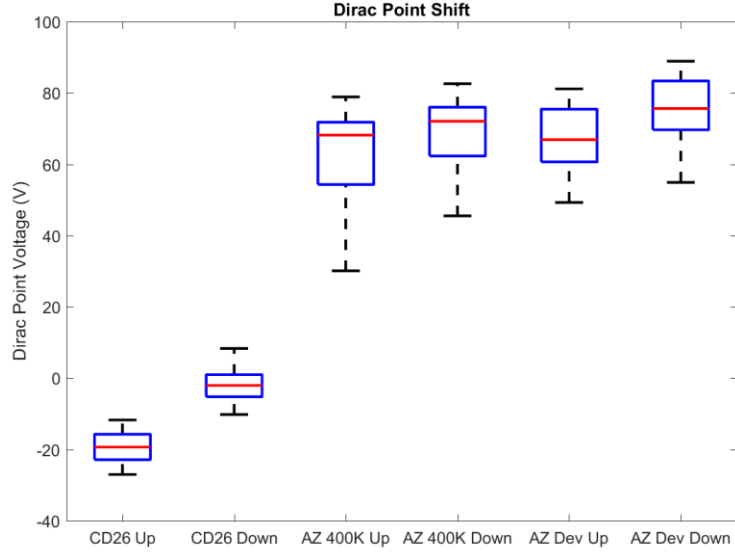


Figure 6.7 Dirac point voltage measured for the devices fabricated using different photoresist. Labels "Up" and "Down" correspond to sweeping the back-gate voltage up and down.

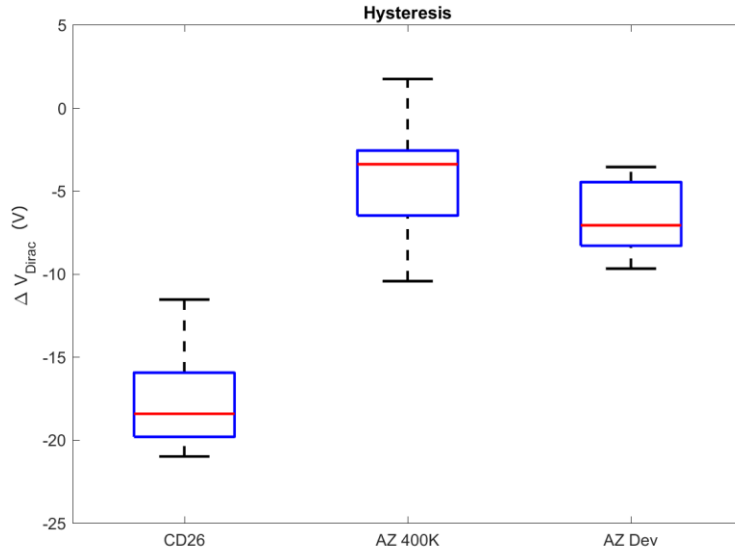


Figure 6.8 Hysteresis in Dirac point voltage, defined as the difference between the up and down voltage sweep Dirac point voltages. The MIC developers show small hysteresis, which can be attributed to the large density of metal-ion doping, screening the interface charges and reducing the hysteresis caused by them.

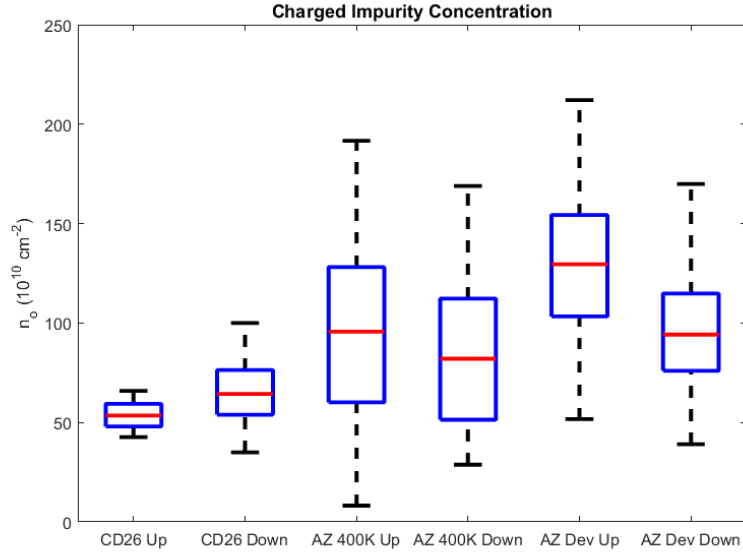


Figure 6.9 Extracted charged-impurity concentration using different developers. As expected, the MIF developers cause the least density of charged-impurities.

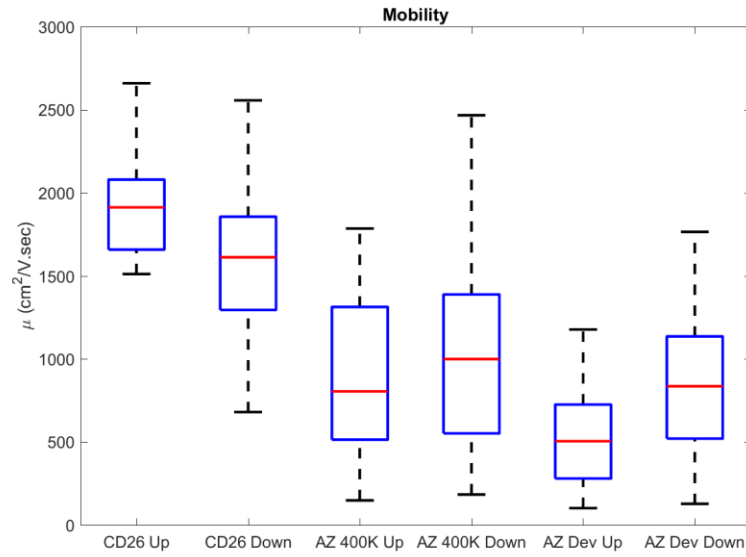


Figure 6.10 Extracted charge carrier mobility using different developers. MIF developers show higher mobility, which can be attributed to the less charged-impurity scattering as they yield lower charged-impurity concentration.



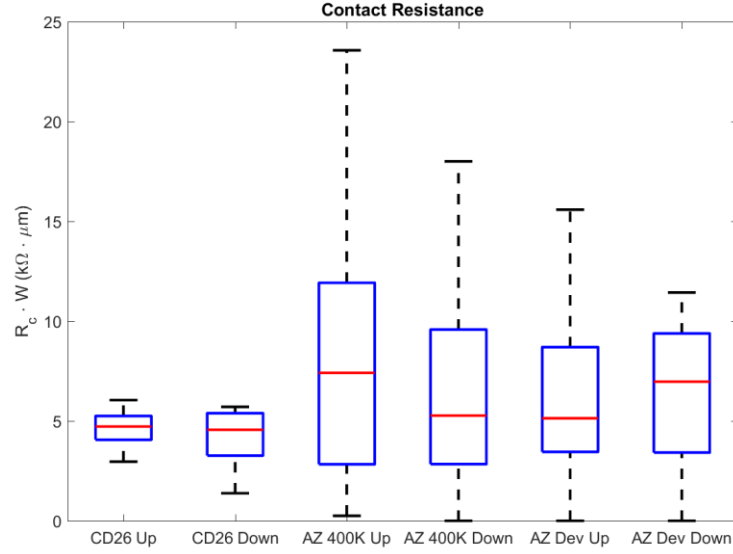


Figure 6.11 Extracted contact resistance. The median values are considerably far apart, but MIF developers show the lowest spread, indicating the most consistent metal-graphene interface.

### 6.3.1 Relation Between Charge Carrier Mobility and Charged-Impurity Concentration

Charge carrier mobility ( $\mu$ ) and charged-impurity concentration ( $n_o$ ) are inversely proportional[24]. It was shown theoretically that the charge carrier  $\mu \cong 33 \frac{q}{0.2 h} \left( \frac{1}{n_o} \right)$ [87]. The study of impact of MIF and MIC developers on graphene FET performance allowed us to experimentally evaluate the relation between charge carrier mobility and charged-impurity concentration.

The extracted charge carrier mobility and the inverse of charged-impurity concentration is shown in Figure 6.12. The data shows a clear inverse relationship between  $\mu$  and  $n_o$ . To evaluate the proportionality constant between the inverse relationship, the data was fit to using the equation  $\mu = k \frac{q}{h} \left( \frac{1}{n_o} \right)$ . The best fit shows  $k \approx 4.24$ , which is significantly different from the theoretically predicted data. This result suggests that the charged-impurity scattering is stronger than what has been predicted theoretically.

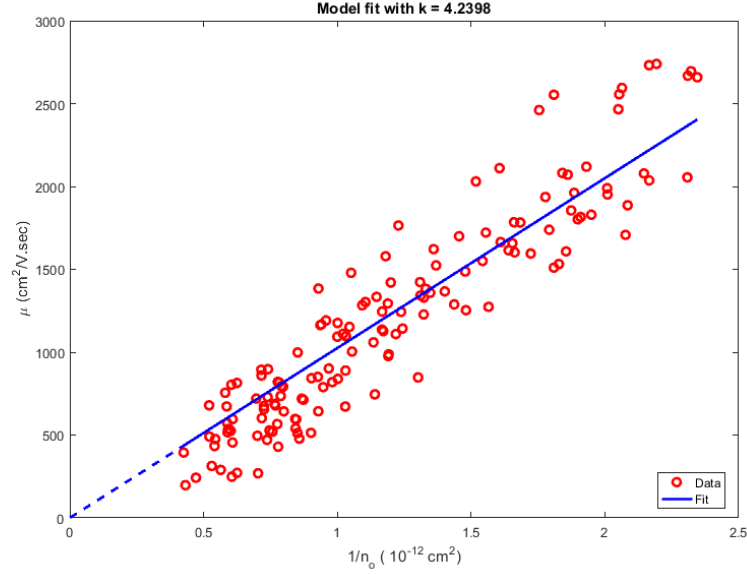


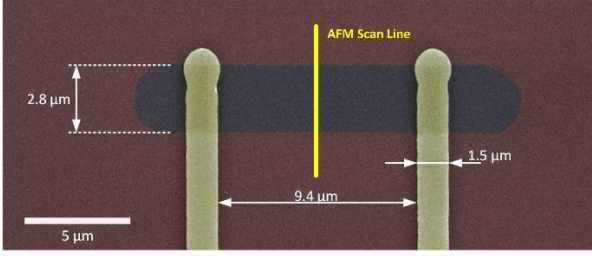
Figure 6.12 Extracted charge carrier mobility vs inverse of charged-impurity concentration. the results show a clear inverse relation between the charge carrier mobility and charged-impurity concentration. The best fit equation is  $\mu \cong 4.24 \frac{q}{h} \left( \frac{1}{n_o} \right)$ . The dashed line shows the extension of the fit to the origin.

## 6.4. Photoresist Residuals on Graphene Channels

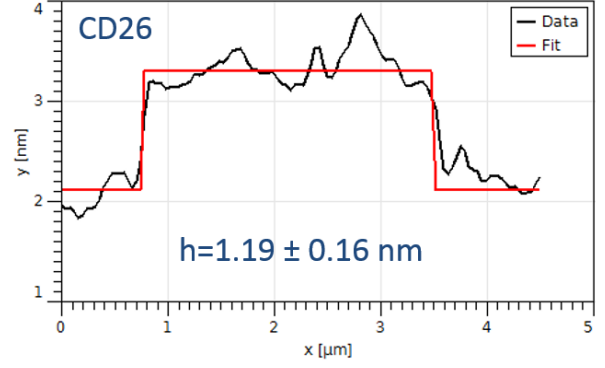
Photoresists are organic, which makes them adhere well to graphene. However, this high adhesion to graphene causes resist residuals to stay on the graphene surface, increasing the contact resistance and acting as a dielectric barrier between the graphene and top gate oxide. The use of oxygen plasma, or milder ozone, to remove the organic contaminants on the graphene and enhance the contact resistance has been reported in the literature[106], [108], [124], [145].

We studied the residual left over graphene channels after the channel definition step. We used AFM analysis to evaluate the step height over the graphene channel right after removing the sacrificial photoresist layer used as an etch mask, as outlined in Appendix B. The step heights using the different photoresists and developers used in Section 6.3 are shown in Figure 6.13.

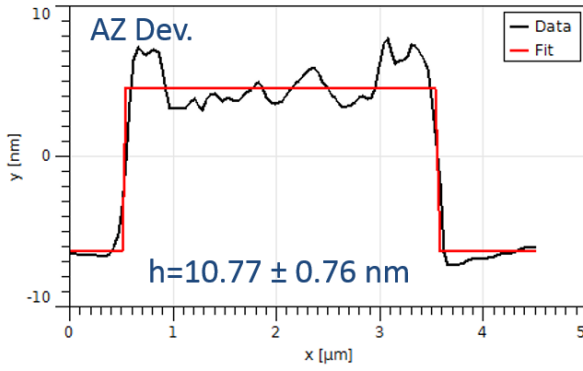
The CD26 developer with S1805 resist shows the smallest step height,  $1.19 \pm 0.16$  nm, which is quite close to the expected AFM step height of graphene, indicating a very thin residue[37], [170], [275].



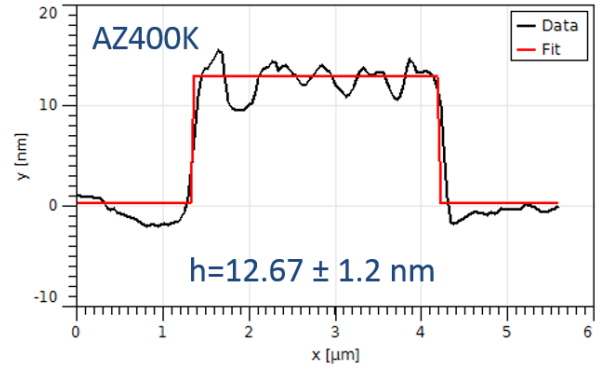
(a)



(b)



(c)



(d)

Figure 6.13 (a) False color SEM image showing the graphene FET with the scan area shown as a yellow line. (b)-(d) AFM scan results for when using CD 26, AZ Developer and AZ400 developer, respectively.

On the contrary, the channels defined using AZ Developer and AZ400K with AZ4110 photoresist show step heights in the excess of 10 nm. These results point towards high adhesion between the photoresist and graphene. The large step height also mean that the interface of graphene is covered with a relatively thick residue, which will certainly affect the transport and interface properties. This might be one of the reasons behind the large spread in extracted model values in Section 6.3 for the devices fabricated using AZ Developer and AZ400K.

## 7) Conclusion and Future Work

In this work, we explored the use of graphene devices for use in heterogeneous integration with CMOS. In this section, we discuss some of the techniques that can allow us overcome the current technological limitations and create high-performance graphene-CMOS heterogeneous systems.

### 7.1. Alloyed Contacts for Optimized Thermal and Electrical Contact Resistance

Losses in metal-graphene electrical contacts leads to Joule heating. The generated heat in the contact and the channel can dissipate through the channel-dielectric interface or the metal-graphene interface. Generally, the metal-graphene interface has a larger thermal conductance, allowing most of the heat to dissipate through it. Co-optimization of the electrical contact and thermal interface resistance will reduce the Joule heating and allow more efficient heat dissipation, reducing the temperature of the channel and hence reducing the scattering of electrons by phonons. This is especially important in deeply scaled graphene FETs with channel lengths  $< 0.5 \mu\text{m}$ , where most of the generated heat tends to flow through the channel and contact[107], [271].

The thermal interface and electrical contact resistance are a strong function of the interface quality and bonding between the materials. Metals on graphene interface change the graphene band structure if they chemisorb on it, and dope it when they adsorb to it[100], [118]. Pure metals span the interaction spectrum from of no interaction as gold on graphene, to weak interaction as in palladium on graphene, and finally strong interaction that leads to band structure changes as in the case of nickel on graphene[96], [100], [118]. An example of the thermal interface and electrical contact conductance is shown in Figure 7.1[110], [126], [272], [273], [277]. The optimal contact would be one in the top right corner with high thermal interface and electrical contact resistance.

The use of metal alloys allows us to fine-tune the interface properties. Pd-Ni and Au-Pd alloys could span the interaction spectrum between their respective elements. However, the experimental evaluation of electrical contact and thermal interface and conductance using one sample per alloy composition would be tedious and time consuming. The use of compositionally spread alloy films (CSAF) allows the rapid experimental evaluation of the electrical and thermal properties of metal-graphene contacts. Using CSAFs of different metals, for example a Pd-Ni CSAF, we can evaluate the whole interaction spectrum from Pd to Ni using a single sample. As such, the use of CSAF metal films would allow us to rapidly determine the optimal composition of metal-graphene contacts.

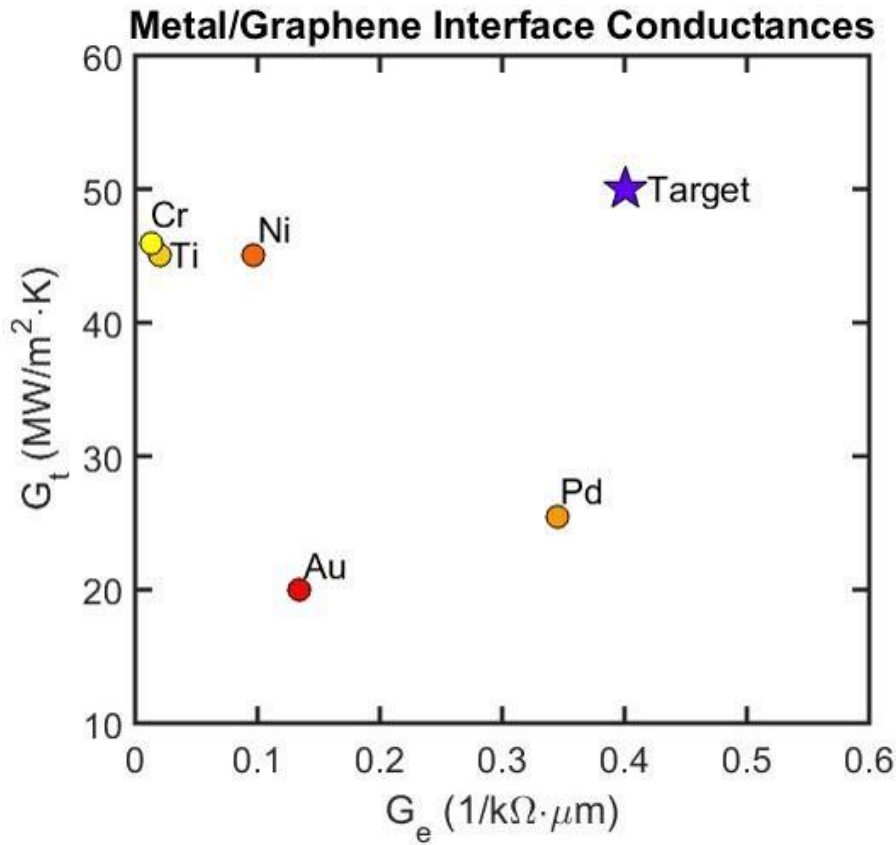


Figure 7.1 Thermal Interface and Electrical Conductances of different elemental metals on graphene.

Our preliminary results using alloy films show that Pd-Ni alloys to be a strong candidate for the co-optimization of both electrical and thermal interface contact resistance. Yet, more work is needed to investigate how alloying affects the interface properties[110].

## 7.2. Mixing 2D Materials for Optimized Contacts

Contacts to 2D materials poses a challenge. Contacts dope 2D materials, and 2D materials with a band-gap, such as MoS<sub>2</sub>, the contact doping determines the device type[50], [278]. In addition, reduction of the contact resistance is crucial for the realization of high-performance devices. Using graphene as an intermediary lead between the contact metal and other 2D material channels is a promising alternative for alleviating contact doping [50], [279]–[281]. The combination of alloyed metals with graphene intermediate contacts to 2D materials might pave new ways in the understanding of 2D material contacts, and pave the road for high-performance 2D electronics.

## 7.3. Oblique incidence diodes using exfoliated graphene encapsulated by hBN

Charge carrier scattering limits the performance of devices that rely on ballistic transport for proper operation, as in oblique incidence diodes. The use of hBN as a substrate has been shown to yield very high mean free paths even at room temperature[247], [248]. Accordingly, designing oblique incidence diodes using exfoliated graphene encapsulated by hBN is expected to reduce charge carrier scattering leading to a narrower angular distribution of charge carriers [247], [248]. The projected reduction in angular distribution spread would increase the forward-to-backward current ratio significantly, allowing the realization of practical graphene diodes.

It is worth noting that encapsulation of graphene might not be enough to reduce the angular spread of charge carriers. Top-contacted graphene devices show large contact resistance relative to edge contacts, which can be contributed to more scattering at the contact[249]. As such, the optimal device structure would incorporate hBN-encapsulated exfoliated graphene, with edge contacts.

## 7.4. CVD Graphene over CVD hBN

The heterogeneous integration of graphene with CMOS requires the use of CVD graphene to be able to achieve full coverage of CMOS-sized samples. With hBN being the best dielectric to use with graphene in terms of reduced scattering and compatibility[238], [246]–[248], [274], [280], [282], [283], it is the rational choice for use with graphene in heterogeneous graphene-CMOS circuits. The growth of wafer-scale hBN opens the way for integration of CVD graphene devices with CVD hBN[284]–[286], which would allow the creation of wafer-scale, high-performance graphene devices. More work is needed to evaluate the performance of heterostructures created using CVD graphene with CVD hBN and to understand the processing and performance limitations of such devices.

## 7.5. Conclusion

Heterogeneous integration of graphene with CMOS allows the utilization of the advantages of both CMOS and graphene. In this work, we presented several non-transistor graphene devices that implement different circuit functions. These graphene devices show performance traits that are better than CMOS in some aspects, but technological obstacles limit their applicability in practical systems.

The implementation of high-performance graphene-CMOS heterogeneous systems requires surmounting the current technological constraints. However, novel graphene devices show promising performance when used in non-conventional transistor architectures.

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# Appendix A) Graphene Processing

## A.1. Preprocessing Anneal

CVD graphene transfer typically requires spinning a PMMA support layer over the graphene to hold it when etching away the growth substrate (typically copper)[142]. PMMA residue affect the transport properties of graphene and increase the contact resistance. To remove the PMMA residue, graphene post transfer is annealed in a forming gas at around 300 °C to remove the PMMA residuals[34], [108], [127], [139], [142], [287], [288].

Throughout this work, the preprocessing anneal was performed at a temperature of 270-300 °C, for at least 4 hours, 5% H<sub>2</sub> in Ar by volume (25 sccm H<sub>2</sub> in 475 sccm of Ar). The process was performed in a 2” quartz tube at atmospheric pressure.

## A.2. Photoresist spin coat

The spin coating parameters depended on the photoresist used. The following parameters summarizes the photoresist spin coating parameters used throughout this work:

- S1805 Photoresist:
  1. Spin coat LOR3A lift-off layer at 4000 RPM for 45 seconds.
  2. Post spin bake at 190 °C for 5 minutes.
  3. Spin coat S1805 resist at 4000 RPM for 45 seconds.
  4. Post spin bake at 115 °C bake for 5 minutes.
- AZ4110 Photoresist:
  1. Spin coat AZ4110 photoresist at 5000 RPM for 90 seconds
  2. Post spin bake at 5 minute bake at 95 °C

### A.3. Photolithography

The lithography was performed using Karl Süss MA6 contact aligner in contact mode. The light source was an i-line, 320 nm source calibrated to an intensity of 5 mW/cm<sup>2</sup>. The photolithography masks used were 4"x4"x0.090" Quartz AR with a chrome mask layer, procured from Photronics Inc.

The photolithography parameters depended on the photoresist used. The following parameters summarize the photolithography exposure and development procedure used throughout this work. Note that prior to the exposure of the sample, a dummy sample was first exposed to ensure proper source calibration:

- S1805 Photoresist:
  - Exposure Time: 18 seconds
  - Development parameters: 1 minute in CD26 with gentle agitation followed by a 30 second rinse in gently running water.
- AZ4110 Photoresist with AZ400K developer:
  - Exposure Time: 45 seconds
  - Development parameters: 1 minute in 1:4 AZ400K:DI (by volume) with gentle agitation followed by a 30 second rinse in gently running water.
- AZ4110 Photoresist with AZ developer:
  - Exposure Time: 35 seconds
  - Development parameters: 1.7 minutes in 1:1 AZ400K:DI (by volume) with gentle agitation followed by a 30 second rinse in gently running water.

Lift-off was performed in Microposit 1165 remover kept in a closed beaker on a hot plate set to 70 °C.

### A.4. Electron-Beam Lithography

PMMA A7 was used as an e-beam resist throughout this work. The following steps were used during e-beam lithography:

1. Spin coat PMMA A7 at 5000 RPM for 90 seconds.
2. Post spin bake at 180 °C or 190 °C for 90 seconds.
3. Exposure parameters:
  - a. Working distance: 6.5-7.5 mm.
  - b. Acceleration voltage: 30 kV.
  - c. Spot Size: 3.
  - d. Beam current: ~136 pA.
  - e. Magnification: Depends on pattern size. Typically 1500x.
  - f. Point-to-Point Spacing: 5 nm.
  - g. Line-to-Line Spacing: 30 nm.
  - h. Line dose: 1.6 nC/cm.
  - i. Area dose: 450-600  $\mu\text{C}/\text{cm}^2$ .
4. Development parameters:
  - a. Developer: 1:3 MIBK:IPA (by volume)
  - b. Development time: 55 seconds with gentle agitation followed by 15 seconds in IPA with gentle agitation

## A.5. Electron-Beam Evaporation

Samples were loaded over a 3” carrier wafer using 90 °C heat release tape. The samples were left to pump out in vacuum for at least 3 hours, typically overnight reaching a base pressure in the low  $10^{-7}$  Torr, in the Ultek E-Beam evaporator. The current then was increased slightly till the pressure started going down (this only occurs for the first layer after the pump down when the evaporated metal reacts with the water vapor and radicals sticking to the evaporation chamber walls), while ensuring the e-beam is properly focused and centered on the source crucible. The shutter was opened once the chamber pressure started going up.

The rate for all deposition over graphene was kept between 0.1 – 0.3 Å/sec to enhance the adhesion between the metal and the graphene. This was kept for the first 3-5 nm then the rate was increased to the values typically used with that metal in the evaporation chamber.

The typical evaporation currents were as follows:

- Cr: 20 mA
- Ti: 30-40 mA
- Pd: 40-50 mA
- Al: 40 mA
- Au: 50 mA

After the evaporation run was complete the chamber was let to cool down for 15 minutes before venting.

## A.6. Top Gate Oxide/Passivation Deposition

The top gate oxide used throughout this work was  $\text{Al}_2\text{O}_3$  due to its high reported mobility[87]. To facilitate the ALD of oxide on graphene we used a seed layer of evaporated aluminum left to oxidize in air[87]. The top gate oxide deposition parameters throughout this work was as follows:

1. Evaporate 1.5 nm of aluminum then leave it in air for at least 30 minutes.
2. Load the sample into ALD machine with the growth chamber temperature set and stable at 150 °C.
3. Grow 8.5 nm of  $\text{Al}_2\text{O}_3$  using a TMAH based precursor with  $\text{H}_2\text{O}$  as an oxygen source (thermal growth NOT plasma assisted growth). The growth rate was about 1 Å/cycle. The 8.5 nm deposition took around an hour.

The sample was removed from the chamber once the run was done.

## A.7. Graphene etching

Graphene etching was done using  $\text{O}_2$  plasma in a Reactive-Ion Etching machine (Plasma-Therm 790 RIE). We used this machine because initial experimentation with the IPC Barrel Etcher showed excessive lateral etching underneath the etch mask sacrificial layer. On the other hand, the RIE machine yielded cleaner etches with less lateral etching. The etch parameters in the Plasma-Therm 790 RIE are as follows:

- Recipe name: mdgphn1m



- Chuck used: Aluminum
- Etch time: 1 minute
- Power: 20 W
- Gases: 14:6 O<sub>2</sub>:Ar
- Pressure: 1 mT
- DC Voltage: ~ 180V (automatically controlled)

## A.8. Backside oxide etch

Commercially available graphene and thermally-grown SiO<sub>2</sub> over silicon substrates come with an oxide on the on both the top-side and back-side of the substrate, that is, the oxide is on both sides of the silicon carrier wafer. The top-side oxide is grown over the finished silicon face and acts as the back-gate oxide. The top-side oxide is the back-gate oxide that carrier the transferred graphene. The back-side oxide is a byproduct of the thermal growth process. The back-side oxide prevents electrical contact to the silicon substrate and should be removed prior to any measurements. This can be confirmed by optically inspecting the back side of the carrier wafer: if the backside is any color other than grey then it is covered with an oxide. Pictures depicting the back side of the sample (graphene facing down) are shown in Figure A.1, showing the back side before and after the removal of the back-side oxide.

Before doing any processing on the back side, the top-side oxide and graphene should be covered by spin coating PMMA or photoresist over it to prevent scratching the graphene during the etch of the back-side oxide. The back-side oxide can be removed using RIE or by floating it over BHF. We prefer the use of RIE etching because it is more safe and less prone to accidental damage to the graphene features if the sample falls into the BHF. When using an RIE oxide etch recipe, the etch time and recipe should be carefully set up to prevent, and remove, any polymer formation on the silicon surface as it would increase the contact resistance to the back gate (the silicon).

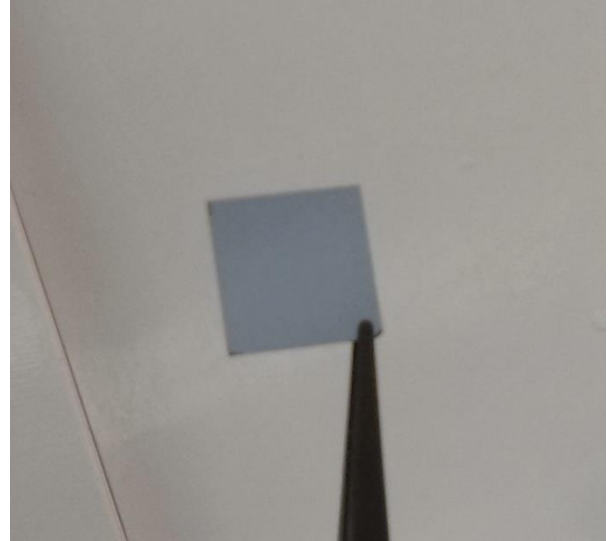
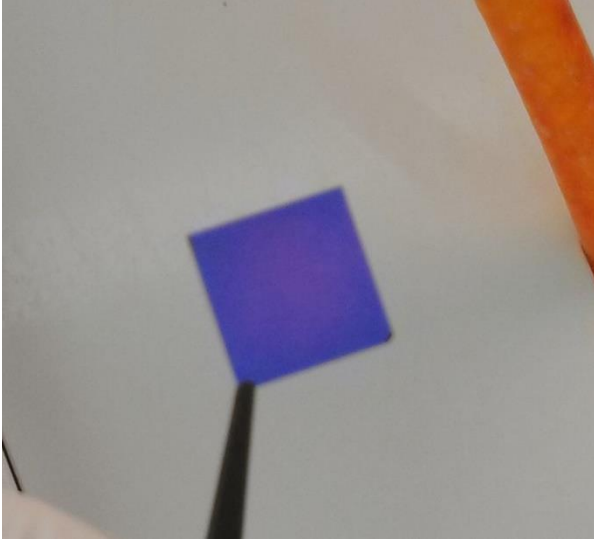


Figure A.1(a) Before, and (b) after the removal of the back-side oxide from the silicon sample. The back-gate oxide is deposited on the top-side of the sample, while the back-side oxide growth is a byproduct of the thermal oxide growth process.

# Appendix B) Fabrication of a Dual-Gated Graphene FET

We go through the details of fabricating a dual-gated graphene FET. This procedure is identical for neurons, synapses and diodes, except for the e-beam mask used to shape the top gate. The processing parameters follow the values outlines in Appendix A. The steps are numbered according to their order. Note that the devices presented in this work were all fabricated using CVD graphene over 285 nm of thermal SiO<sub>2</sub>, procured from Graphene Supermarket. The top gate oxide was 10 nm of Al<sub>2</sub>O<sub>3</sub>, and the top gate metal was 25 nm thick, e-beam evaporated aluminum. The contact stack was Ti/Pd with thicknesses 1.5/40 nm.

## A. Preprocessing Anneal

The preprocessing anneal is crucial to remove any PMMA residual from the graphene transfer step and is typically performed for at least 4 hours before any fabrication.

## B. Contact Photolithography

1. Spin coating the photoresist and contact layer lithography as shown in Figure B.1.

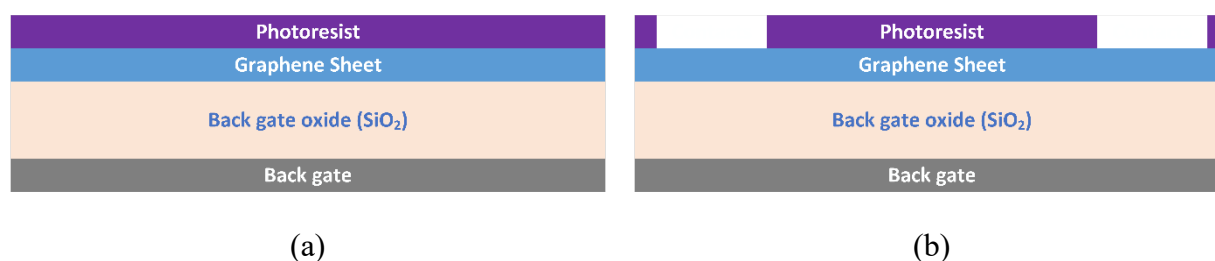
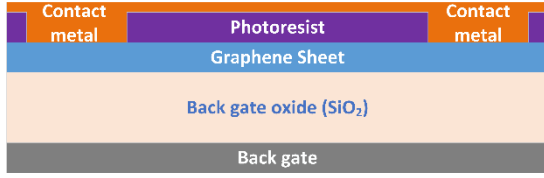
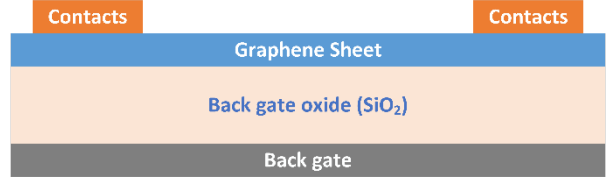


Figure B.1 Sample cross-section after (a) Spin coating, and (b) photolithography and development of contact layer.

2. Contact metal stack evaporation and lift-off as shown in Figure B.2.



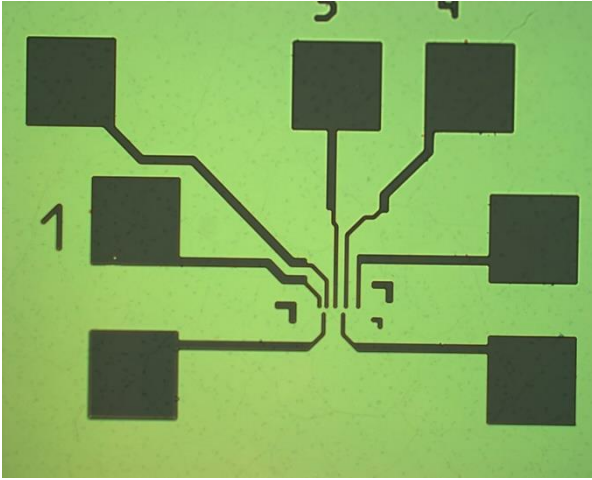
(a)



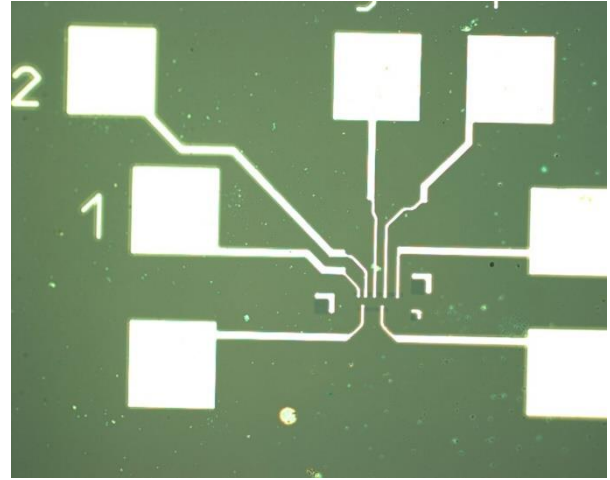
(b)

Figure B.2 Sample cross-section after (a) contact stack evaporation, and (b) contacts lift-off.

Figure B.3 shows an optical microscope image of the sample after steps (1) and (2).



(a)

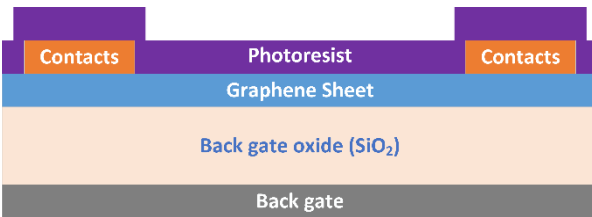


(b)

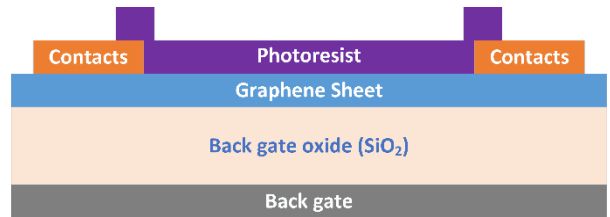
Figure B.3 Optical microscope image after (a) contact photolithography, and (b) contacts lift-off.

### C. Channel Definition

1. Spin coating the photoresist and the channel etch mask as shown Figure B.4.



(a)



(b)

Figure B.4 Sample cross-section after (a) Spin coating, and (b) photolithography and development of channel etch mask.

2.  $O_2$  plasma etching of the exposed graphene using the RIE and removal of the etch mask as shown in Figure B.5.

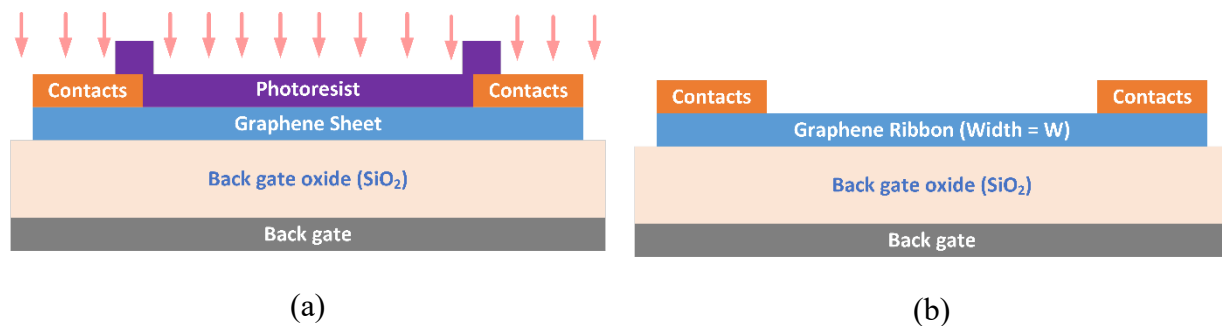


Figure B.5 Sample cross-section (a) during channel definition, and (b) after etch mask removal. The red arrows signify the  $O_2$  plasma etching the exposed graphene.

Figure B.6 shows an optical microscope image of the sample after steps (1) and (2). Figure B.6(a) shows the tears in the graphene channel prior to the etch. After the etch no graphene is visible outside the etch mask as seen in Figure B.6(b).

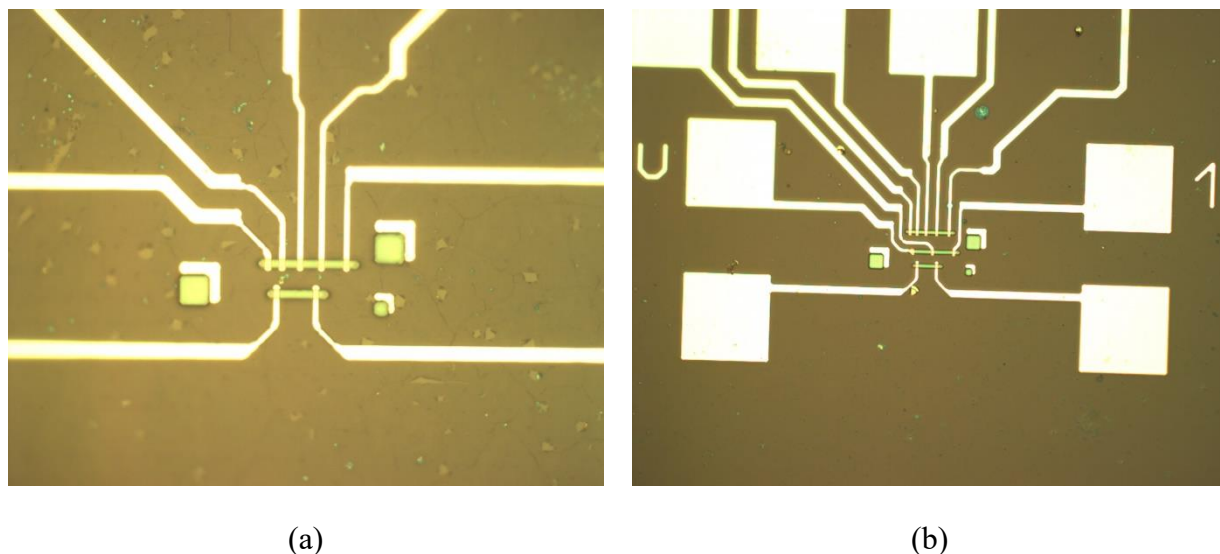


Figure B.6 Optical microscope image after (a) contact photolithography, and (b) contacts lift-off.

#### D. Top Gate Oxide/Passivation Deposition

ALD seed layer is evaporated then the ALD is performed over the seed as shown in Figure B.7. The top gate oxide also acts as a passivation to protect the channel from the environment. In our experiments, 10 nm of  $Al_2O_3$  was enough to protect the graphene from environmental dopants.

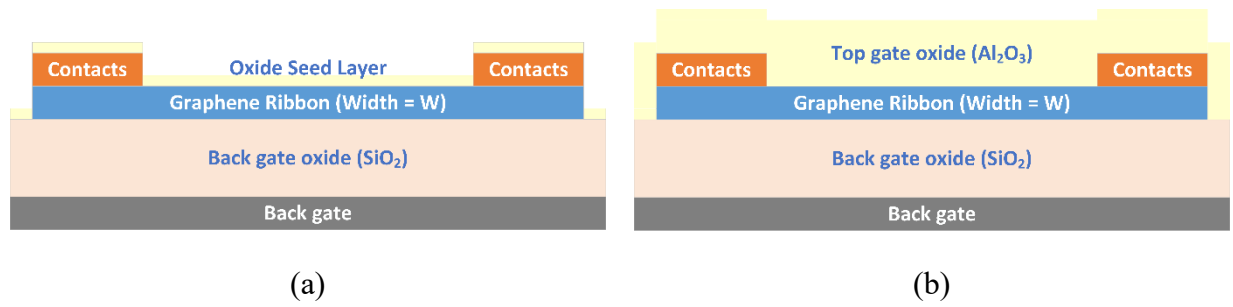


Figure B.7 Sample cross-section after (a) seed layer evaporation, and (b) top oxide ALD.

### E. Top Gate Lithography

This step is only required if a top gate is needed. The step is used for the fabrication of the neurons, synapses or diode oblique gates. The only difference is the e-beam mask used to pattern the top gate.

1. Spin coating the e-beam resist and the e-beam lithography of top gate as shown in Figure B.8.

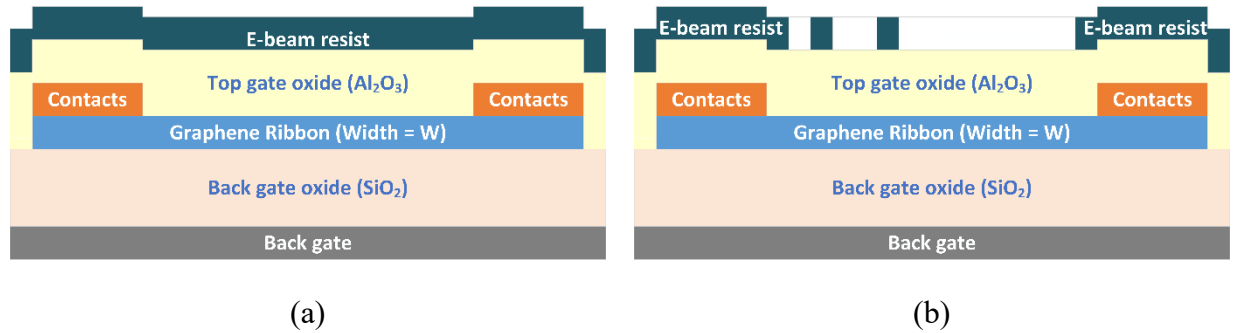


Figure B.8 Sample cross-section after (a) Spin coating, and (b) e-beam lithography and development of top gate deposition mask.

2. Evaporation of the top gate metal stack and lift-off as shown in Figure B.9.

Figure B.10 shows an optical microscope image and a false color SEM image of a graphene synapse after step (2).

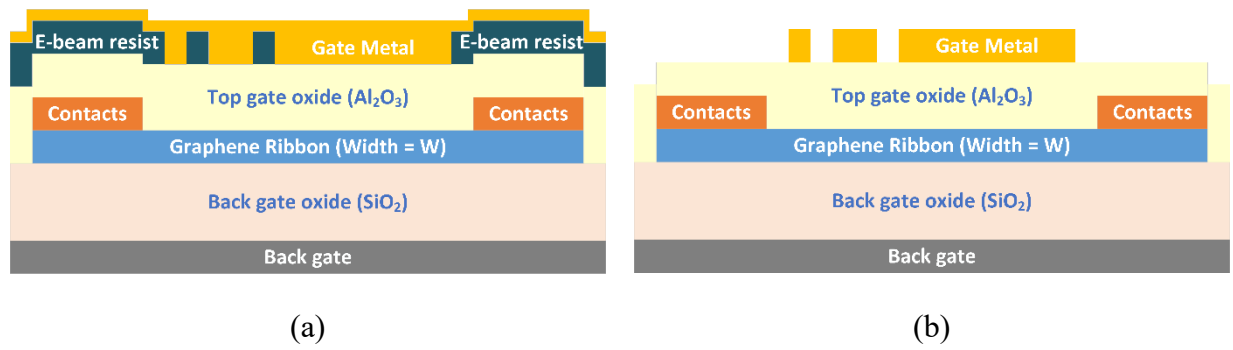


Figure B.9 Sample cross-section after (a) top gate metal stack evaporation, and (b) top gate lift-off.

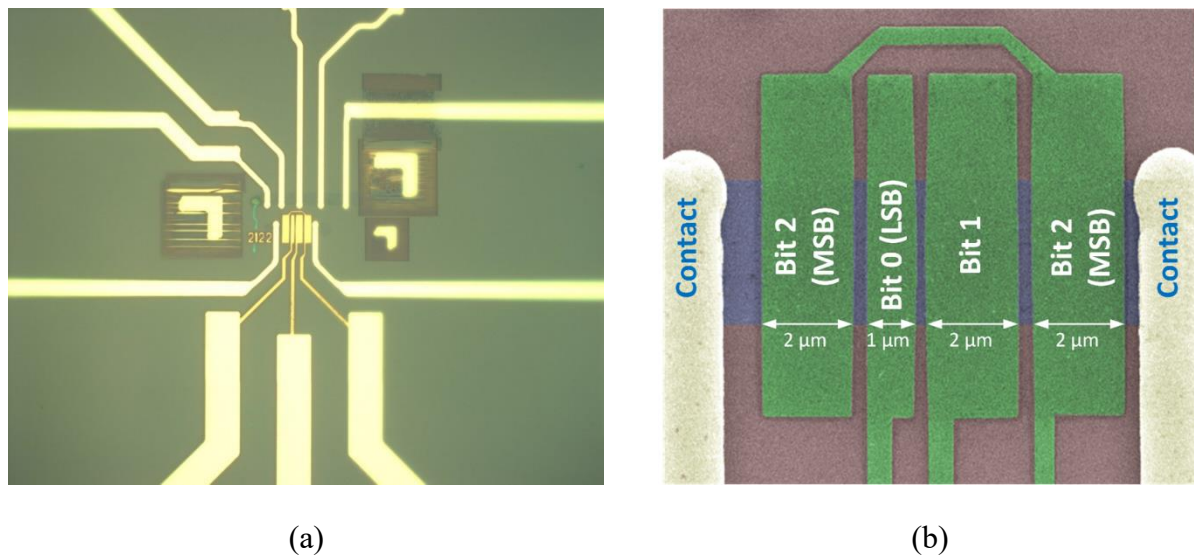


Figure B.10 (a) Optical microscope image of graphene synapse, and (b) False color SEM image of the same device.

#### F. Back-side oxide etch

1. Spin coating the top side of the sample (devices side) with photoresist or PMMA and bake it.
2. Use the RIE to etch the back side oxide, while putting protected device-side down, or put the sample gently over BHF, while keeping the protected device-side up, making sure to put it down softly so as it floats over the BHF. The BHF will etch only the back side oxide. Sometimes, the BHF vapor seeps under the protection layer damaging some of the oxide and devices near the edges and corners of the sample.

### G. Contact window opening

This step is optional and only required if the top gate oxide is too thick or too hard for the probes to punch through it, or if the devices are to be wire bonded.

1. Spin coating the photoresist and the photolithography of contact openings as shown in Figure B.11.

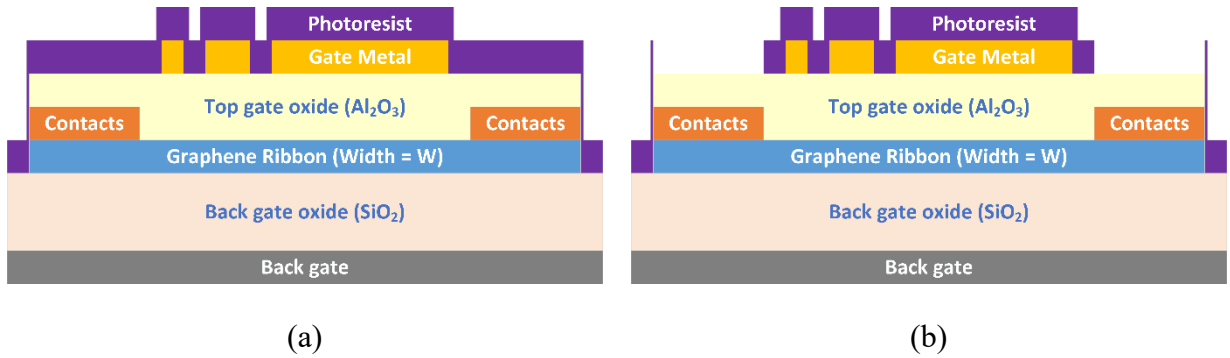


Figure B.11 Sample cross-section after (a) Spin coating, and (b) photolithography and development of oxide etch mask.

2. Ion milling or RIE etching of the exposed oxide and removal of the etch mask as shown in Figure B.12. It is recommended to use  $\text{O}_2$  plasma etching to remove any the top most crust of the photoresist prior to dissolving the etch mask as the crust is typically hardened by ion milling and removing it enhances dissolving of the etch mask.

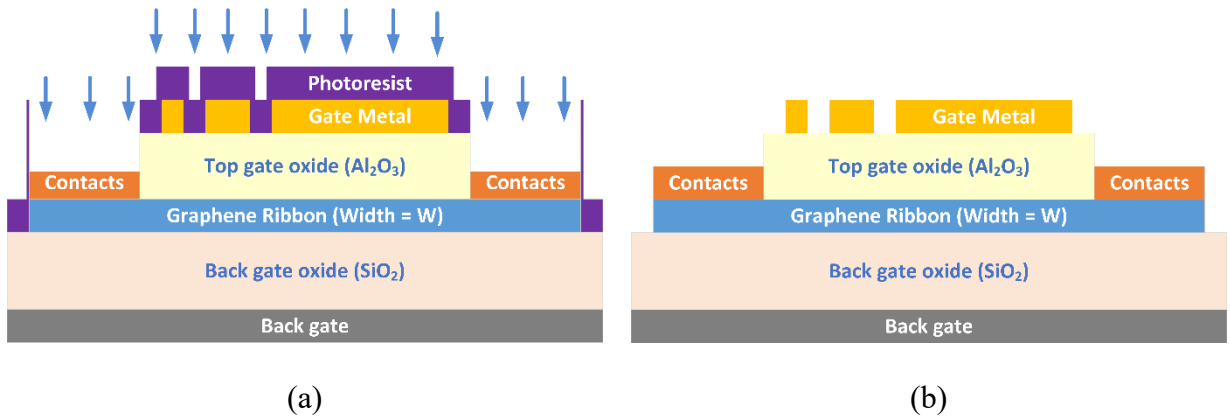


Figure B.12 Sample cross-section (a) during oxide etching, and (b) after etch mask removal. The blue arrows signify the accelerated ions used for ion milling or the reactive species if RIE is used for etching the exposed oxide.



# Appendix C) Measurement Setup for Dual-Gated Graphene FETs

The measurement setup for measuring dual-gated FETs used throughout this thesis is shown in Figure C.1. A conducting chuck is used to carry the sample alloying direct connection between the Keithley 2400 Source Meter used to control the back-gate voltage and the sample back gate. The Keithley 6487 Picoammeter is used to measure the device current/resistance and applying supplying the device measurement voltage. The NI 9264 Voltage Output module was used to set the top-gate voltage and can be omitted in measurements that do not have a top-gate.

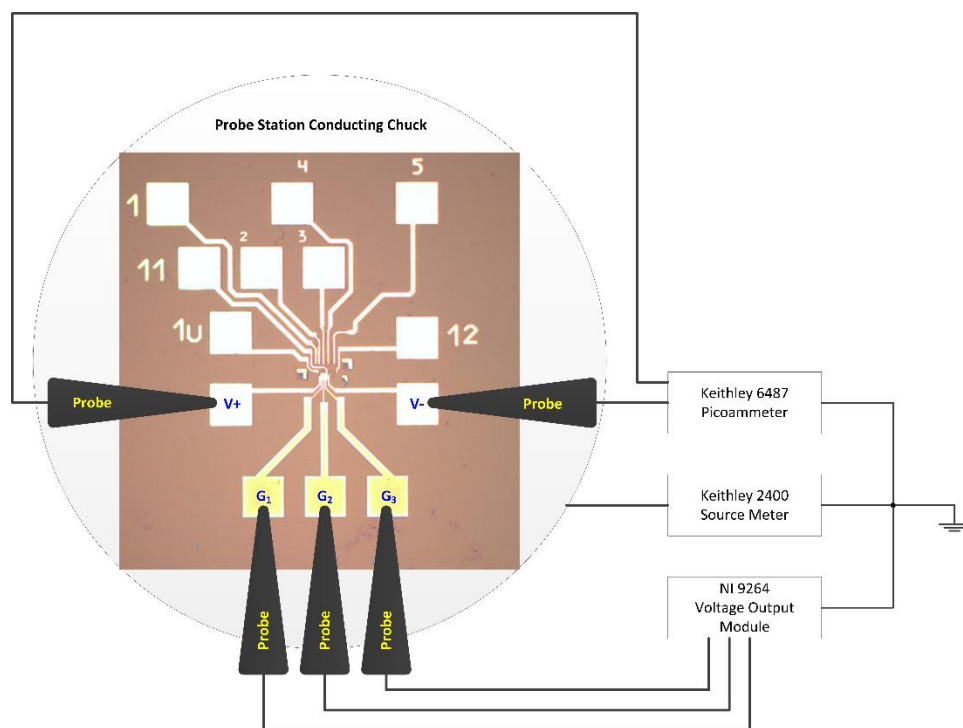


Figure C.1 Measurement setup used when measuring dual-gated FETs and devices. The use of a conducting chuck enables direct connection to the back-gate via the chuck. When no top gate is required, the NI 9264 can be omitted from the test setup.

# Appendix D) Derivation of the Current Coupling Coefficient in a Diffusive-Transport Graphene Coupler

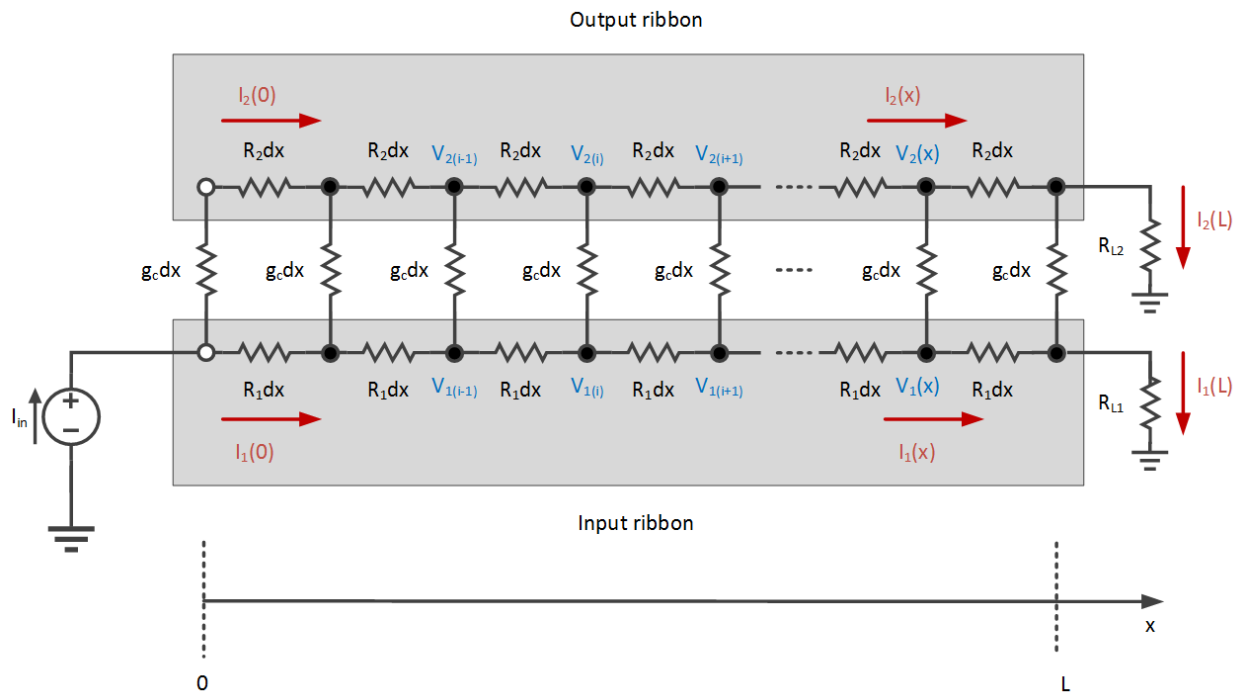


Figure D.1 Electrical model of graphene coupler. The graphene ribbons are modelled using two distributed resistors with a resistance per unit length of  $R_1$  and  $R_2$ , and the tunneling resistance coupling them is modelled using a distributed conductance with conductance per unit length  $g_c$ .

The electrical model of the device is composed of three distributed resistors: a distributed resistor for each of the graphene ribbons with a distributed tunneling conductance connecting them together, as shown in Figure D.1. We label one of the ribbons as the input ribbon, and the other as

the output ribbon. For this analysis, we apply a current stimulus at the input ribbon and calculate the current at other end (output) of each ribbon.

We start by solving the voltage differential equation for the distributed system then relating it to the current.

Applying KCL at any node the node (i), we get:

$$\frac{V_{1(i-1)} - V_{1(i)}}{R_1 dx} = \frac{V_{1(i)} - V_{1(i+1)}}{R_1 dx} + g_c dx (V_{1(i)} - V_{2(i)})$$

$$\frac{V_{2(i-1)} - V_{2(i)}}{R_2 dx} = \frac{V_{2(i)} - V_{2(i+1)}}{R_2 dx} + g_c dx (V_{2(i)} - V_{1(i)})$$

This can be rewritten as:

$$\frac{V_{1(i-1)} - 2V_{1(i)} + V_{1(i+1)}}{R_1 (dx)^2} = g_c (V_{1(i)} - V_{2(i)})$$

$$\frac{V_{2(i-1)} - 2V_{2(i)} + V_{2(i+1)}}{R_2 (dx)^2} = g_c (V_{2(i)} - V_{1(i)})$$

Taking the limit as  $dx \rightarrow 0$ , we get:

$$\frac{1}{R_1} \left( \frac{d^2 V_1(x)}{dx^2} \right) = g_c (V_1(x) - V_2(x))$$

$$\frac{1}{R_2} \left( \frac{d^2 V_2(x)}{dx^2} \right) = g_c (V_2(x) - V_1(x))$$
(D.1)

Substituting from the two equations together to decouple the equations we get:

$$V_2(x) = V_1(x) - \frac{1}{g_c R_1} \left( \frac{d^2 V_1(x)}{dx^2} \right)$$

$$V_1(x) = V_2(x) - \frac{1}{g_c R_2} \left( \frac{d^2 V_2(x)}{dx^2} \right)$$

Accordingly, the differential equation for each branch after substitution:

$$\frac{1}{R_2} \left( \frac{d^2 V_2(x)}{dx^2} \right) = \frac{1}{R_2} \left( \frac{d^2 V_1(x)}{dx^2} - \frac{1}{g_c R_1} \left( \frac{d^4 V_1(x)}{dx^4} \right) \right) = -\frac{1}{R_1} \left( \frac{d^2 V_1(x)}{dx^2} \right)$$

$$\frac{1}{R_1} \left( \frac{d^2 V_1(x)}{dx^2} \right) = \frac{1}{R_1} \left( \frac{d^2 V_2(x)}{dx^2} - \frac{1}{g_c R_2} \left( \frac{d^4 V_2(x)}{dx^4} \right) \right) = -\frac{1}{R_2} \left( \frac{d^2 V_2(x)}{dx^2} \right)$$

The resulting decoupled equations are:

$$-\left( \frac{d^4 V_1(x)}{dx^4} \right) + g_c (R_1 + R_2) \left( \frac{d^2 V_1(x)}{dx^2} \right) = 0 \quad (\text{D.2})$$

$$-\left( \frac{d^4 V_2(x)}{dx^4} \right) + g_c (R_1 + R_2) \left( \frac{d^2 V_2(x)}{dx^2} \right) = 0 \quad (\text{D.3})$$

The two differential equations are the same. The general solution is written as:

$$V_{1,2}(x) = A_{1,2} + B_{1,2}x + C_{1,2}e^{\sqrt{g_c(R_1+R_2)}x} + D_{1,2}e^{-\sqrt{g_c(R_1+R_2)}x} \quad (\text{D.4})$$

The above equation can be rewritten by setting  $L_c^{-1} = \sqrt{g_c(R_1 + R_2)}$  to be:

$$V_{1,2}(x) = A_{1,2} + B_{1,2}x + C_{1,2}e^{x/L_c} + D_{1,2}e^{-x/L_c} \quad (\text{D.5})$$

Current conservation dictates the boundary conditions on the current as:

$$I_{in} = I_1(0) + I_2(0) = I_1(L) + I_2(L) = I_1(x) + I_2(x) \quad (\text{D.6})$$

Ohm's law relates the current and voltage at any given position as:

$$I_1(x) = -\frac{1}{R_1} \left( \frac{dV_1(x)}{dx} \right), I_2(x) = -\frac{1}{R_2} \left( \frac{dV_2(x)}{dx} \right) \quad (\text{D.7})$$

In addition, Ohm's law as relates the voltage and current at the output end of each ribbon:

$$I_1(L) = V_1(L)/R_{L1}$$

$$I_2(L) = V_2(L)/R_{L2} \quad (\text{D.8})$$

The coupling coefficient between the current in the two ribbons is defined as the ratio between the output ribbon and input ribbon branch currents as:

$$C_I(x) = \frac{I_2(x)}{I_{in}} \quad (\text{D.9})$$

Equations (D.1) and (D.4) can be solved for the relation between the constant  $A - D$  to give:

$$\frac{C_1}{C_2} = \frac{D_1}{D_2} = -\frac{R_1}{R_2}, \quad A_1 = A_2 = A, \quad B_1 = B_2 = B \quad (\text{D.10})$$

Before proceeding to solve the equation, we note that the voltage and current equation present a system of two coupled second order linear equations, reducible to two fourth order decoupled ordinary differential equations. Ohm's law relates the voltage gradient to the current and hence, the current continuity equation poses a condition on the first derivative of the voltage, while Equation (D.8) serves as a Robin boundary condition relative the voltage to its derivative at the boundary. Accordingly, the current system cannot be completely solved analytically; we will not be able to obtain the values of the four constants needed to fully determine a unique solution, but it can be solved numerically. In this discussion, we provide an incomplete solution that does not determine all the unknown constants, but reveals the functional form of the solution.

By letting  $C_1 = C, D_1 = D$ , we can write the current in each branch using the left side of Equation (D.7) as:

$$\begin{aligned} I_1(x) &= -\frac{B}{R_1} - \frac{1}{R_1 L_C} \left( C e^{\frac{x}{L_C}} - D e^{\frac{-x}{L_C}} - (C - D) \right), \\ I_2(x) &= -\frac{B}{R_2} + \frac{1}{R_1 L_C} \left( C e^{\frac{x}{L_C}} - D e^{\frac{-x}{L_C}} - (C - D) \right) \end{aligned} \quad (\text{D.11})$$

From the current conservation equation (D.6) we obtain the requirement on the constant  $B = -\frac{I_{in} R_1 R_2}{R_1 + R_2}$ , allowing us to rewrite Equation (D.11) as:

$$\begin{aligned}
I_1(x) &= I_{in} \frac{R_2}{R_2 + R_1} - \frac{1}{R_1 L_C} \left( C e^{\frac{x}{L_C}} - D e^{\frac{-x}{L_C}} \right), \\
I_2(x) &= I_{in} \frac{R_1}{R_2 + R_1} + \frac{1}{R_1 L_C} \left( C e^{\frac{x}{L_C}} - D e^{\frac{-x}{L_C}} \right)
\end{aligned} \tag{D.12}$$

The voltage across each ribbon is this given as:

$$\begin{aligned}
V_1(x) &= A - I_{in} \frac{R_1 R_2}{R_2 + R_1} x + \left( C e^{\frac{x}{L_C}} - D e^{\frac{-x}{L_C}} \right), \\
V_2(x) &= A - I_{in} \frac{R_1 R_2}{R_2 + R_1} x - \frac{R_2}{R_1} \left( C e^{\frac{x}{L_C}} - D e^{\frac{-x}{L_C}} \right)
\end{aligned} \tag{D.13}$$

Although it is quite tempting to null the increasing exponential constant  $C$ , its presence is important in maintaining the consistency of the equations. This is can be seen through applying the boundary condition given by Equation (D.8):

$$\begin{aligned}
V_1(L) - V_2(L) &= \frac{R_1 + R_2}{R_1} \left( C e^{\frac{L}{L_C}} + D e^{\frac{-L}{L_C}} \right) = I_1(L) R_{L_1} - I_2(L) R_{L_2} \\
&= \frac{I_{in}}{R_1 + R_2} (R_2 R_{L_1} - R_1 R_{L_2}) \\
&\quad - \frac{1}{R_1 L_C} \left( C e^{\frac{L}{L_C}} - D e^{\frac{-L}{L_C}} \right) (R_{L_1} + R_{L_2})
\end{aligned} \tag{D.14}$$

If the constant  $C$ , is set to zero the while  $R_{L_1} = R_{L_2} = 0$ , Equation (D.14) reduces to:

$$(R_1 + R_2) L_C D e^{\frac{-L}{L_C}} = 0 \tag{D.15}$$

Equation (D.15) can only be satisfied if  $D$  is also nulled. This result is erroneous as it means that the current will not change regardless of the values of  $R_1 + R_2$  if the output of the device is shorted. In line with Equation (D.14), we can extract the value of  $C$  as:

$$C = \frac{\left( \frac{I_{in}}{R_1 + R_2} (R_2 R_{L_1} - R_1 R_{L_2}) + D e^{\frac{-L}{L_C}} \left( \frac{R_{L_1} + R_{L_2}}{R_1 L_C} - \frac{R_1 + R_2}{R_1} \right) \right) e^{\frac{-L}{L_C}}}{\frac{R_{L_1} + R_{L_2}}{R_1 L_C} + \frac{R_1 + R_2}{R_1}} = C' e^{\frac{-L}{L_C}} \tag{D.16}$$

Equation (D.16) shows that the coefficient of the exponential increasing term decays exponentially with the length of the device and will not cause an unphysical increase in the voltage or current across the device length.

To sum up, we can write the functional form of the voltage and current across the coupler as:

$$I_1(x) = I_{in} \frac{R_2}{R_2 + R_1} - \frac{1}{R_1 L_C} \left( C' e^{\frac{x-L}{L_C}} - D e^{\frac{-x}{L_C}} \right), \quad (D.17)$$

$$I_2(x) = I_{in} \frac{R_1}{R_2 + R_1} + \frac{1}{R_1 L_C} \left( C' e^{\frac{x-L}{L_C}} - D e^{\frac{-x}{L_C}} \right)$$

$$V_1(x) = A - I_{in} \frac{R_1 R_2}{R_2 + R_1} x + C' e^{\frac{x-L}{L_C}} + D e^{\frac{-x}{L_C}}, \quad (D.18)$$

$$V_2(x) = A - I_{in} \frac{R_1 R_2}{R_2 + R_1} x - \frac{R_2}{R_1} \left( C' e^{\frac{x-L}{L_C}} + D e^{\frac{-x}{L_C}} \right)$$

The solution reveals the functional form of the current to distribute between the two lines in an asymptotic fashion. The current asymptote is roughly given by the current division ratio had the two branches been connected only at the input end. The asymptotic behavior roughly follows an exponentially decaying function with a characteristic length  $L_C = (\sqrt{g_C(R_1 + R_2)})^{-1}$ .

To demonstrate the functional behavior, we study the case when the coupler branches have matched impedance with their loads, i.e. when  $\frac{R_1}{R_2} = \frac{R_{L1}}{R_{L2}}$ , which reduces Equation (D.16) to:

$$C' = \frac{D \left( \frac{R_{L1}}{R_1 L_C} - 1 \right) e^{-\frac{L}{L_C}}}{\frac{R_{L1}}{R_1 L_C} + 1} \quad (D.19)$$

For all practical purposes, the value of  $C' \ll D$  and thus the contribution of the exponentially increasing term in Equation (D.17) and Equation (D.18) can be neglected to give:

$$I_1(x) \approx I_{in} \frac{R_2}{R_2 + R_1} + \frac{1}{R_1 L_C} \left( D e^{\frac{-x}{L_C}} \right), \quad (D.20)$$

$$\begin{aligned}
I_2(x) &\approx I_{in} \frac{R_1}{R_2 + R_1} - \frac{1}{R_1 L_C} \left( D e^{\frac{-x}{L_C}} \right) \\
V_1(x) &\approx A - I_{in} \frac{R_1 R_2}{R_2 + R_1} x + D e^{\frac{-x}{L_C}}, \\
V_2(x) &\approx A - I_{in} \frac{R_1 R_2}{R_2 + R_1} x - \frac{R_2}{R_1} \left( D e^{\frac{-x}{L_C}} \right)
\end{aligned} \tag{D.21}$$

A useful approximation that simplifies the analysis considerably is to assume  $I_2(0) = 0$ . This assumption is valid especially when  $g_C^{-1} \ll R_1, R_2$ . This assumption is especially valid in our analysis, as  $g_C$  is a tunneling conductance that is considerably small relative to the conductance of the either branches of the coupler. Under this assumption,  $\frac{D}{R_1 L_C} = \frac{I_{in} R_1}{R_1 + R_2}$  and thus we can rewrite Equation (D.21) as:

$$\begin{aligned}
I_1(x) &\approx \frac{I_{in}}{R_2 + R_1} \left( R_2 + R_1 e^{\frac{-x}{L_C}} \right), \\
I_2(x) &\approx \frac{I_{in} R_1}{R_2 + R_1} \left( 1 - e^{\frac{-x}{L_C}} \right)
\end{aligned} \tag{D.22}$$

Equation (D.22) demonstrates the behavior of the coupler under the matching approximation, while neglecting  $I_2(0)$ . The current in each branch asymptotically approaches its value had the two ribbons been connected only at the input side, with an asymptotic behavior following an exponential function with a characteristic length of  $L_C = \left( \sqrt{g_C(R_1 + R_2)} \right)^{-1}$ . In this case the current coupling coefficient is given as:

$$C_I(x) = \frac{I_2(x)}{I_{in}} = \frac{R_1 \left( 1 - e^{\frac{-x}{L_C}} \right)}{R_2 + R_1} \tag{D.23}$$

In the limit when  $L \gg L_C$ , the current coupling coefficient at the output end of the coupler is:

$$C_I(L) \approx C_I(\infty) = \frac{R_1}{R_1 + R_2} \tag{D.24}$$