**Graphene Devices for Beyond-CMOS Heterogeneous Integration**

Submitted in partial fulfillment of the requirements for

the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

Mohamed Darwish

B.S., Electronics and Communications Engineering, Ain Shams University

M.S., Electronics and Communications Engineering, Ain Shams University

Carnegie Mellon University

Pittsburgh, PA

September 2017

© Mohamed Darwish, 2017

All rights reserved

# Acknowledgements

# Abstract

Semiconductor manufacturing is the workhorse for a wide range of industries. It lies at the heart of consumer electronics, telecommunication equipment and medical devices. Most semiconductor electronics are made from Silicon, and are fabricated using CMOS technology. The versatility of semiconductor electronics stems from the ever-reducing cost of integrating more computing and memory functions on chip. The small cost for adding extra functions has been maintained in the past 50 years through transistor scaling. Transistor scaling focuses on shrinking the size of transistors integrated on chip. This reduction in transistor size, while keeping the overall cost of the chip fixed allowed us to reduce the cost per function with scaling, and is what is celebrated as Moore’s law. Scaling has been working gracefully up to the last decade, where the exponential rise in manufacturing cost and diminishing gains of scaling on device performance reduce its economic benefit. To revive the cost reduction trend, different techniques were proposed such as augmenting CMOS manufacturing with new materials (Beyond CMOS), 3D integration, and integrating more non-transistor elements on-chip (More than Moore).

In this work, we focus on the efficient implementation of several circuit functions using an allotropy of carbon known as graphene. Graphene, a single layer of carbon atoms arranged in a hexagonal lattice, has unique electronic properties that has been taken the solid-state electronics community by a storm since its first experimental conception in 2004. Despite its promising electronic properties, namely the very high charge-carrier mobility and reduced scattering by impurities, graphene circuits has been held back by a plethora of nonidealities and technological roadblocks that hamper its use in traditional transistor-based circuits. In this work, we attempt to leverage the unique physical properties of graphene to implement non von-Neumann neuromorphic computing architectures, low-loss diodes and evaluate the behavior of diffusive-transport graphene couplers. We focus on the the design, fabrication and characterization of graphene devices in the presence of the current performance-limiting technological nonidealities in heterogeneous graphene-CMOS systems. We present the design, fabrication and characterization of all-graphene resistive data converters devices and diodes, discussing their performance and application as building elements of all-graphene brain-inspired computing architectures. We evaluate the performance of graphene couplers operating in the diffusive transport regime, which serve as a method to analyze the cross-coupling between adjacent graphene interconnects. We also discuss the current technological limitations hampering the performance of graphene devices, and the roles of different processing non-idealities on the characteristics of graphene devices.

# Table of Contents

# List of Tables

# List of Figures

1. Introduction

The Semiconductor Industry has evolved over the d

## Economics of Scaling and Moore’s Law

## Beyond-CMOS Materials and Devices

## Graphene as a Beyond-CMOS Material

## Overview of Document

1. The Electronic Properties of Graphene

## Electronic Band Structure of Graphene

## Klein-Tunneling and the Absence of Backscattering

## The Role of the Substrate

## Charge Transport in CVD Graphene

## Contact-Induced Doping

## Characterization of Graphene

### Raman Analysis

### Constant Mobility Model

1. All-Graphene Neuromorphic Computing Architectures

## Cellular Neural Networks (CNNs)

## All-Resistance CNNs

## Graphene Neurons and Synapses

## Measurement Results

## Conclusion

1. Graphene Low-Loss Diodes

## Geometric Graphene Diodes

## Oblique Incidence Diodes

## Performance Limitations

### Lead Resistance

### Momentum Distribution Smearing by Scattering

## Measurement Results

## Conclusion

1. Diffusive-Transport Graphene Couplers

## Modeling Diffusive-Transport Current Coupling

## Dependence Current Coupling Coefficient on Coupling Distance

## Impact of Current Coupling on Deeply Scaled Interconnects

## Conclusion

1. Current Technological Limitations on Graphene Devices and Circuits

## Contact Engineering

### Electrical Resistance

### Thermal Interface Conductance

## Interface Roughness

## Stress in dual-gated Graphene FETs during Processing

## Impact of Metal-Ion Containing Developers on the Performance of Graphene FETs

1. Conclusion and Future Work

## Alloyed Contacts for Optimized Thermal and Electrical Contact Resistance

## CVD Graphene over CVD hBN

## Mixing 2D Materials for Optimized Contacts

# References

1. Graphene Processing

## Preprocessing Anneal

## Photolithography

## Electron-Beam Lithography

## Electron-Beam Evaporation

## Top Gate Oxide/Passivation Deposition

1. Fabrication of a Dual-Gated Graphene FET
2. Measurement Setup for Dual-Gated Graphene FETs
3. Measurement Setup for Graphene Diodes