**Graphene Devices for Beyond-CMOS Heterogeneous Integration**

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# Abstract

Semiconductor manufacturing is the workhorse for a wide range of industries. It lies at the heart of consumer electronics, telecommunication equipment and medical devices. Most semiconductor electronics are made from Silicon, and are fabricated using CMOS technology. The versatility of semiconductor electronics stems from the ever-reducing cost of integrating more computing and memory functions on chip. The small cost for adding extra functions has been maintained in the past 50 years through transistor scaling. Transistor scaling focuses on shrinking the size of transistors integrated on chip. This reduction in transistor size, while keeping the overall cost of the chip fixed allowed us to reduce the cost per function with scaling, and is what is celebrated as Moore’s law. Scaling has been working gracefully up to the last decade, where the exponential rise in manufacturing cost and diminishing gains of scaling on device performance reduce its economic benefit. To revive the cost reduction trend, different techniques were proposed such as augmenting CMOS manufacturing with new materials (Beyond CMOS), 3D integration, and integrating more non-transistor elements on-chip (More than Moore).

In this work, we focus on the efficient implementation of several circuit functions using an allotropy of carbon known as graphene. Graphene, a single layer of carbon atoms arranged in a hexagonal lattice, has unique electronic properties that has been taken the solid-state electronics community by a storm since its first experimental conception in 2004. Despite its promising electronic properties, namely the very high charge-carrier mobility and reduced scattering by impurities, graphene circuits has been held back by a plethora of nonidealities and technological roadblocks that hamper its use in traditional transistor-based circuits. In this work, we attempt to leverage the unique physical properties of graphene to implement non von-Neumann neuromorphic computing architectures, low-loss diodes and evaluate the behavior of diffusive-transport graphene couplers. We focus on the the design, fabrication and characterization of graphene devices in the presence of the current performance-limiting technological nonidealities in heterogeneous graphene-CMOS systems. We present the design, fabrication and characterization of all-graphene resistive data converters devices and diodes, discussing their performance and application as building elements of all-graphene brain-inspired computing architectures. We evaluate the performance of graphene couplers operating in the diffusive transport regime, which serve as a method to analyze the cross-coupling between adjacent graphene interconnects. We also discuss the current technological limitations hampering the performance of graphene devices, and the roles of different processing non-idealities on the characteristics of graphene devices.

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The similarity between the dispersion relation of photons and charge carriers in graphene points designers to design optics-inspired electronic devices. An interesting optics-inspired analog is the electronic directional coupler. Optics directional couplers allow coupling light between two branches, where the coupling coefficient varies periodically with the coupling distance[1]. The electronic wave modes in graphene ribbons and the resistive coupling between graphene ribbons in close proximity has been analyzed for ballistic transport [2]–[4]. The problem of analyzing resistive coupling in diffusive graphene ribbons is different from that in ballistic graphene ribbons. The successive scattering events randomize the wavefunction phase information [5]–[7] prohibiting the use of the coupled-mode theory. A direct consequence of this phase randomization is losing the spatial periodicity of the coupling coefficient predicted in ballistic devices.

Modeling of resistive coupling is crucial for deeply scaled interconnects, in which transport will inadvertently be diffusive unless methods for reducing line-edge roughness induced-scattering are developed[8]–[10]. Graphene interconnects in close proximity has been studied previously to evaluate their cross-talk performance[11]–[17]. Prior work focused on analyzing the delay and energy metrics of a single graphene interconnect, or accounting only for the capacitive coupling among interconnects.

In this chapter, we study the coupling between graphene ribbons operating in the diffusive transport regime. We start by developing an analytical model for the coupling resistance between two graphene ribbons separated by a dielectric, highlighting the impact of different fabrication nonidealities on the coupling. We then evaluate the spatial dependence of such coupling coefficient, showing its monotonic saturating behavior, and assess the impact of such coupling on the performance of deeply scaled interconnects.

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