Faculty of Media Engineering and Technology
Dept. of Computer Science and Engineering
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CSEN/CSIS 402: Computer organization
Spring 2022

Project – milestone 1

Instructions

- The project should be implemented using LogiSim
- Every team should have one submission
- You are always welcome to discuss the project with the TAs during the available office hours.
- You must work with your team members only. Do not exchange information with other teams or
- individuals.
- Cheating and plagiarism will be strictly punished with a grade of 0 in the project.
- Please respect the submission deadline marked at the beginning of the document.

Submission guideline and deadlines

- The project should be submitted as a Zip file containing the Logisim files.
- The submission should sent via email to **co.spring22@gmail.com** by May 8, 2022.
- **Your file name should be your group number and the email subject should include it as well. Include your names and emails in the email body as well.**
- The evaluation will take place in the week from May 8 to May 13. Slots will be available to you by then. All group members must be present.

Description

In this milestone, you are required to implement a subset of the basic computer to do a simulation for a memory system and an arithmetic/logic unit and a group of registers. All components should be linked through a common bus that has 3 control select lines S2, S1 and S0.

- The memory (RAM) should have 128 addresses (words). Each word is 16-bits.
- Users should be able to read and write to the memory.
- The Address Register (AR) output should be linked to the address lines of the memory
- The memory's input and output lines are connected to the common bus.
- The available registers are:
  - DR
  - TR
  - AR
  - AC (Accumulator Register)

Each register has a load enable flag to control whether the data available from the bus, will update its content or not.

The functionalities and control numbers ($C_2C_1C_0$) of the arithmetic unit (ALU) which has 2 inputs A and B, coming from the DR and the AC:

- (001) Adding the numbers A+B (you can use the available adder in Logisim)
- (010) Subtracting two numbers A-B (you can use the available subtractor in Logisim)
- (011) Transferring one number (A)
- (100) ANDing (A AND B)
- (101) ORing (A OR B)
- (110) XORing (A XOR B)
- (111) Increment A

The selection of the bus should be done as follows:

S_2	S_1	S_0	Selection
0	0	0	Memory
0	0	1	AR
0	1	0	TR
0	1	1	DR
1	0	0	AC

Testing your circuit

Fill in the first 2 locations of the memory as follows:

Address	Value
0	35
1	55

And also fill in register [AR] initially with value 0.

You should try your resulting circuit with different control signals values (that you assign manually) to test the following RTLs to achieve 35+55 (or M[0]+ M[1])

```
TR ← M[AR]   // transfer  M[0]=35 to TR
DR ← AR      // move 0 to DR
AC ← DR+1    // increment 0 to 1
AR ← AC      // store it back to AR
DR ← M[AR]   // transfer M[1]=55 to DR
AC ← DR      // transfer 55 to AC
DR ← TR      // transfer 35 to DR
AC ← DR + AC // add 35 to 55
```

(the last RTL, you can try different operations other than addition, like and, or, xor, subtract between DR and AC which are supposed to contain 35 and 55)

Question: What would you do to store the result in M[2]?