ENSC 894

# LAB 3 REPORT

Team 5 : Amrutha Suresh, Mohammed Shuhad

## 1. Benchmarks

### 1.1 Non optimized - 4096 * 4096 csim

Using whole rows and whole columns as the tile. Tile size = 4096 * 4 bytes

```
+ Timing:
    * Summary:
    +--------+---------+----------+------------+
    |  Clock |  Target | Estimated| Uncertainty|
    +--------+---------+----------+------------+
    |ap_clk  |  3.00 ns|  3.212 ns|     0.81 ns|
    +--------+---------+----------+------------+

+ Latency:
    * Summary:
    +-------------+-------------+-------------+-------------+-------------+-------------+---------+
    |       Latency (cycles)    |     Latency (absolute)    |           Interval          | Pipeline|
    |      min    |      max    |     min     |     max     |      min    |      max    |   Type  |
    +-------------+-------------+-------------+-------------+-------------+-------------+---------+
    |  756316950529|  756316950529|  2.4e+03 sec|  2.4e+03 sec|  756316950530|  756316950530|     none|
    +-------------+-------------+-------------+-------------+-------------+-------------+---------+

    + Detail:
        * Instance:
        N/A

        * Loop:
        +---------------+-------------+-------------+-----------+-----------+-----------+------+----------+
        |               |      Latency (cycles)     | Iteration |  Initiation Interval  | Trip |          |
        |   Loop Name   |      min    |      max    |  Latency  |  achieved |   target  | Count| Pipelined|
        +---------------+-------------+-------------+-----------+-----------+-----------+------+----------+
        |- OUTER_LOOP   |  756316950528|  756316950528|  184647693|          -|          -|  4096|        no|
        | + COPY_LOOP   |         4097|         4097|          3|          1|          1|  4096|       yes|
        | + COPY_LOOP   |         4102|         4102|          8|          1|          1|  4096|       yes|
        | + INNER_LOOP  |    184639488|    184639488|      45078|          -|          -|  4096|        no|
        |  ++ COPY_LOOP |         4097|         4097|          3|          1|          1|  4096|       yes|
        |  ++ MULT_LOOP |        36876|        36876|         22|          9|          1|  4096|       yes|
        |  ++ COPY_LOOP |         4097|         4097|          3|          1|          1|  4096|       yes|
        +---------------+-------------+-------------+-----------+-----------+-----------+------+----------+


================================================================
== Utilization Estimates
================================================================
* Summary:
+---------------------+---------+------+---------+--------+-----+
|         Name        | BRAM_18K| DSP  |    FF   |   LUT  | URAM|
+---------------------+---------+------+---------+--------+-----+
|DSP                  |        -|     -|        -|       -|    -|
|Expression           |        -|     -|        0|     366|    -|
|FIFO                 |        -|     -|        -|       -|    -|
|Instance             |        -|     5|      506|     274|    -|
|Memory               |        0|     -|        0|       0|    -|
|Multiplexer          |        -|     -|        -|     456|    -|
|Register             |        -|     -|      812|      96|    -|
+---------------------+---------+------+---------+--------+-----+
|Total                |        0|     5|     1318|    1192|    0|
+---------------------+---------+------+---------+--------+-----+
|Available SLR        |     1344|  2976|   871680|  435840|  320|
+---------------------+---------+------+---------+--------+-----+
|Utilization SLR (%)  |        0|    ~0|       ~0|      ~0|    0|
+---------------------+---------+------+---------+--------+-----+
|Available            |     2688|  5952|  1743360|  871680|  640|
+---------------------+---------+------+---------+--------+-----+
|Utilization (%)      |        0|    ~0|       ~0|      ~0|    0|
+---------------------+---------+------+---------+--------+-----+
```

## 1.2 Non optimized - 32 * 32  csim & cosim

+ Timing:
    * Summary:

| Clock | Target | Estimated | Uncertainty |
|---|---|---|---|
| ap_clk | 3.33 ns | 2.786 ns | 0.90 ns |

+ Latency:
    * Summary:

| Latency (cycles) | | Latency (absolute) | | Interval | | Pipeline |
|---|---|---|---|---|---|---|
| min | max | min | max | min | max | Type |
| 26849 | 26849 | 89.407 us | 89.407 us | 26850 | 26850 | none |

    + Detail:
        * Instance:
        N/A

        * Loop:

| Loop Name | Latency (cycles) | | Iteration Latency | Initiation Interval | | Trip Count | Pipelined |
|---|---|---|---|---|---|---|---|
| | min | max | | achieved | target | | |
| - OUTER_LOOP | 26848 | 26848 | 839 | - | - | 32 | no |
| + COPY_LOOP | 32 | 32 | 2 | 1 | 1 | 32 | yes |
| + COPY_LOOP | 37 | 37 | 7 | 1 | 1 | 32 | yes |
| + INNER_LOOP | 743 | 743 | 248 | 16 | 1 | 32 | yes |

==== Utilization Estimates

* Summary:

| Name | BRAM_18K | DSP | FF | LUT | URAM |
|---|---|---|---|---|---|
| DSP | - | - | - | - | - |
| Expression | - | - | 0 | 574 | - |
| FIFO | - | - | - | - | - |
| Instance | - | 100 | 5212 | 2892 | - |
| Memory | 0 | - | 64 | 66 | - |
| Multiplexer | - | - | - | 1857 | - |
| Register | - | - | 6474 | 1024 | - |
| Total | 0 | 100 | 11750 | 6413 | 0 |
| Available SLR | 1344 | 2976 | 871680 | 435840 | 320 |
| Utilization SLR (%) | 0 | 3 | 1 | 1 | 0 |
| Available | 2688 | 5952 | 1743360 | 871680 | 640 |
| Utilization (%) | 0 | 1 | ~0 | ~0 | 0 |

## 2. Optimized Results

### 32 * 32  csim & cosim

```
+ Timing:
    * Summary:
    +--------+---------+----------+------------+
    |  Clock |  Target | Estimated| Uncertainty|
    +--------+---------+----------+------------+
    |ap_clk  |  3.33 ns|  2.613 ns|     0.90 ns|
    +--------+---------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-------+-------+---------+
    |  Latency (cycles) |  Latency (absolute) |    Interval   | Pipeline|
    |   min   |   max   |    min   |    max   |  min  |  max  |   Type  |
    +---------+---------+----------+----------+-------+-------+---------+
    |    67745|    67745|  0.226 ms|  0.226 ms|  67746|  67746|     none|
    +---------+---------+----------+----------+-------+-------+---------+

    + Detail:
        * Instance:
        N/A

        * Loop:
        +--------------------------------+---------+---------+----------+----------+----------+------+----------+
        |                                |  Latency (cycles) | Iteration|  Initiation Interval  | Trip |          |
        |           Loop Name            |   min   |   max   |  Latency |  achieved |   target  | Count| Pipelined|
        +--------------------------------+---------+---------+----------+----------+----------+------+----------+
        |- OUTER_LOOP                    |    67744|    67744|      2117|         -|         -|    32|        no|
        | + COPY_LOOP_A                  |       32|       32|         2|         1|         1|    32|       yes|
        | + COPY_LOOP_C                  |       37|       37|         7|         1|         1|    32|       yes|
        | + COUNT_LOOP                   |     1996|     1996|       499|         -|         -|     4|        no|
        |  ++ OUTER_LOOP_B_COPY_LOOP_B   |      257|      257|         3|         1|         1|   256|       yes|
        |  ++ INNER_LOOP                 |      237|      237|       231|         1|         1|     8|       yes|
        | + COPY_LOOP_STORE              |       32|       32|         2|         1|         1|    32|       yes|
        +--------------------------------+---------+---------+----------+----------+----------+------+----------+


================================================================
== Utilization Estimates
================================================================
* Summary:
+---------------------+---------+------+---------+--------+-----+
|         Name        | BRAM_18K|  DSP |    FF   |   LUT  | URAM|
+---------------------+---------+------+---------+--------+-----+
|DSP                  |        -|     -|        -|       -|    -|
|Expression           |        -|     -|        0|     448|    -|
|FIFO                 |        -|     -|        -|       -|    -|
|Instance             |        -|   160|    14752|    8832|    -|
|Memory               |        0|     -|      160|     229|    -|
|Multiplexer          |        -|     -|        -|    1490|    -|
|Register             |        -|     -|     7833|    1120|    -|
+---------------------+---------+------+---------+--------+-----+
|Total                |        0|   160|    22745|   12119|    0|
+---------------------+---------+------+---------+--------+-----+
|Available SLR        |     1344|  2976|   871680|  435840|  320|
+---------------------+---------+------+---------+--------+-----+
|Utilization SLR (%)  |        0|     5|        2|       2|    0|
+---------------------+---------+------+---------+--------+-----+
|Available            |     2688|  5952|  1743360|  871680|  640|
+---------------------+---------+------+---------+--------+-----+
|Utilization (%)      |        0|     2|        1|       1|    0|
+---------------------+---------+------+---------+--------+-----+
```

Input Buffer size = 32*8

Load and Store functions have been implemented with pipeline strategy of II = 1.

In the Compute function the optimizations done are as follows:

- A buffer is partitioned block wise with a factor of 2
- B buffer is partitioned cyclic with a factor of 2

estimated execution time = number of cycles / frequency =

67745/300 * 10^6 = 0.00022581666

## 4096 * 4096 csim

Input Buffer size = 4096*128

Load and Store functions have been implemented with pipeline strategy of II = 1.

In the Compute function the optimizations done are as follows:

- A buffer is partitioned block wise with a factor of 16
- B buffer is partitioned cyclic with a factor of 16