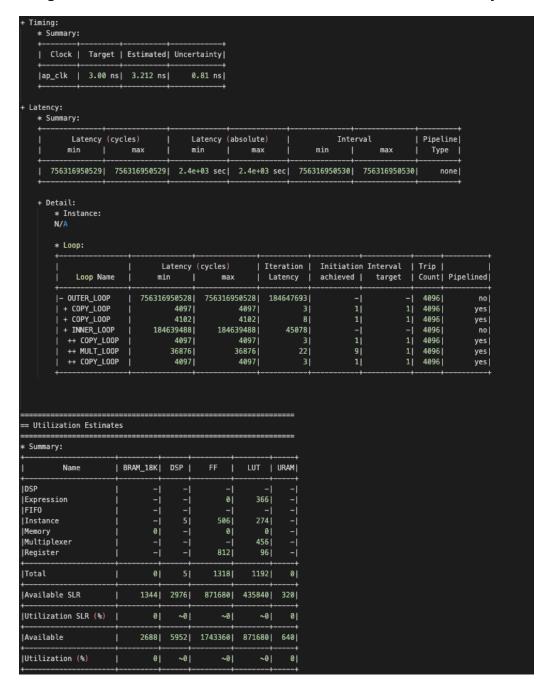
# LAB 3 REPORT

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## 1. Benchmarks

### 1.1 Non optimized - 4096 \* 4096 csim

Using whole rows and whole columns as the tile. Tile size = 4096 \* 4 bytes

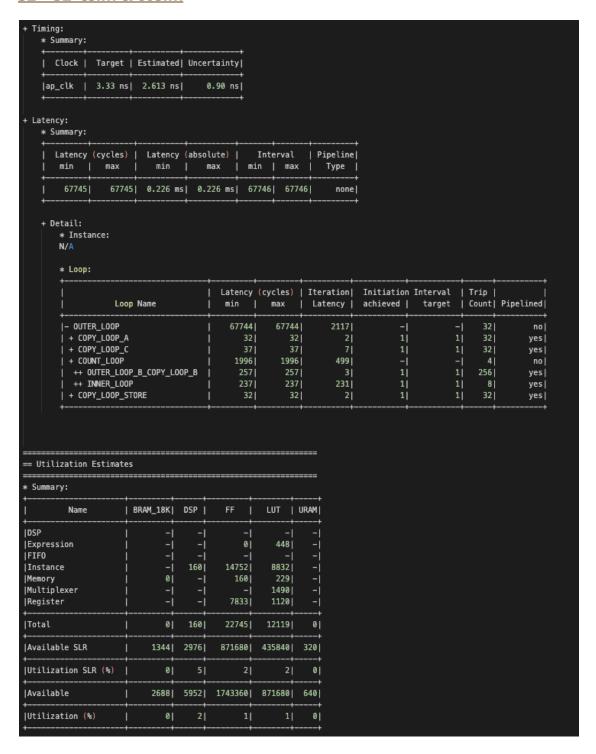


# 1.2 Non optimized - 32 \* 32 csim & cosim

Timing: * Summary:								
+	+ get   Estimate	-t	rtaintyl					
+	+3 ns  2.786 n		0.90 ns					
+	+	-+	+					
Latency: * Summary:								
+	+ les)   Laten ax   min	cy (abs	olute)   max	+ Inte min	rval   max	Pipeline Type		
26849	26849  89.407	us  8	9.407 us	26850  	26850  	none		
+ Detail:     * Instance:     N/A     * Loop:								
     Loop Na		y (cycl		+- ration  tency	Initiat achieve	ion Interv d   targ		   Pipelined
+  - OUTER_LO			<del> </del>	839		+ -	۰۱ ۱-	
+ COPY_LO   + COPY_LO		2	32	2		1	1	
+ COPT_LO   + INNER_L		7  3	37  743	7  248		1  16	1  1	
Utilization Esti	======================================							
Summary:	+			+	-++			
Name	BRAM_18K  +	DSP	FF	LUT +	URAM  -++			
SP xpression	-	-I -I			-  -  41 -			
IFO	i -i	-i	-	i	-i -i			
nstance emory	-    0				2  -  6  -			
lultiplexer								
egister 	_ ii							
otal	0	100	11750	641				
vailable SLR	1344	2976	871680	43584				
Jtilization SLR (%	)   0	3	1	İ	1  0  -+			
Available	2688	5952	1743360	87168	0  640			
	<del> </del>			<del>+</del>	-++			

# 2. Optimized Results

### 32 \* 32 csim & cosim



Input Buffer size = 32\*8

Load and Store functions have been implemented with pipeline strategy of II = 1.

In the Compute function the optimizations done are as follows:

- A buffer is partitioned block wise with a factor of 2
- B buffer is partitioned cyclic with a factor of 2

estimated execution time = number of cycles / frequency =

67745/300 \* 10^6 = 0.00022581666

### 4096 \* 4096 csim

Input Buffer size = 4096\*128

Load and Store functions have been implemented with pipeline strategy of II = 1.

In the Compute function the optimizations done are as follows:

- A buffer is partitioned block wise with a factor of 16
- B buffer is partitioned cyclic with a factor of 16