CS221 Digital Design (Dept of CSE, IIT Guwahati)

Quiz 1 Date 6th Aug 2018 Time 9.00AM to 9.35AM

Name: _____, Roll No:_____

1) [1+1+1 Marks]Convert the binary number **$(0111\ 0111\ 1101\ 1110\ 0111)_2$** to
   a) Octal number :
   b) Booth format of binary number where there can be 0, +1 and -1 to reduce the number of 1's in the number :
   c) 2's complement form assuming number of bit in the number is 20 bits:

2) [2+2 Marks] Proof the Shannon expansion equations using Boolean axioms and rules
   a) **$F(x_1, x_2, \dots, x_n) = x_1'.F(0, x_2, \dots, x_n) + x_1.F(1, x_2, \dots, x_n)$**
   b) Write dual of equation given in Question 1(a) and proof the same.

3) [3 Marks] Design a 16 inputs OR gate using minimum number of 4 inputs NOR gate and 4 inputs NAND gate. Calculate the delay for designed OR gate assuming propagation delay of 4 inputs NAND gate and 4 input NOR gate as t_{NAND} and t_{NOR} respectively.

4) [1+1 Marks] Write truth table for Boolean function **$F(x, y) = x(x'+y(x'+y'))$** and from the resultant truth table, re-write the Sum of Product form of Boolean expression of the same function.

5) [1.5+1.5 Marks] Suppose we want to design a Boolean circuit for a multi bit adder (number of bit for the considered multibit adder is 2). Inputs for the adder are A_1, A_0, B_1 and B_0. Outputs are C, S_1 and S_0. We may assume this addition hardware have 4 inputs and 3 outputs. Write truth table for all the three outputs in term of A_1, A_0, B_1 and B_0. Also write Boolean functions for all the three Outputs (may or may not be in optimized form)

[[Please do not get confuse with design of two bit adder by cascading of one Half Adder and one Full Adder]].