IIT Guwahati - Department of Computer Science & Engineering

CS 223- Computer Organization & Architecture

Practice Tutorial Sheet #1 [23.04.2020] – Solution Set

1. Given a non-pipelined architecture running at 1.5 GHz, that takes 5 cycles to finish an instruction. You want to make it pipelined with 5 stages. Due to hardware overhead the pipelined design will operate only at 1 GHz. 5% of memory instructions cause a stall of 50 cycles, 30% of branch instruction cause a stall of 2 cycles and load-ALU combinations cause a stall of 1 cycle. Assume that in a given program, there exist 20% of branch instructions and 30% of memory instructions. 10% of instructions are load-ALU combinations. What is the speedup of pipelined design over the non-pipelined design?

   up_processor :1.5Ghz →0.667 ns Vs p_processor 1 Ghz →1 ns

   (a) CPI_up = 5

   Execution Time _up= CPI x CCT = 5 x 0.667 ns = 3.335 ns / instruction

   (b) Effective CPI_p = Base CPI + stall CPI

   Category of stalls= Memory stalls+ Branch stalls+ Load –ALU stalls

   Effective CPI_p = Base CPI + Memory stalls per instruction + Branch stalls per instruction + Load –ALU stalls per instruction

   Effective CPI_p = 1 + (0.3x0.05x50) + (0.2x0.3x2) + (0.1x1)

   = 1 + 0.75 + 0.12 +0.1 = 1.97

   Execution Time _p = CPI x CCT = 1.97 x 1 ns = 1.97 ns / instruction

   Speedup = Execution Time _up/ Execution Time _p = 3.335/1.97 = 1.692 times

---

2. In a program there was a branch instruction which is iterated 6 times. The processor uses a (2,2) correlating branch predictor. The outcome of the last two branches is used to index into the BHT. Each entry of BHT is a 2-bit value that is updated by a standard 2-bit predictor automata. Let the initial entry of the BHT for NN/NT/TN/TT is 00/00/11/11, respectively. It was found that the branch predictor has an accuracy of 50% with every alternate iteration of the branch predicted correctly. The first iteration of the branch was mis-predicted. The BHT is indexed with an NN value initially.

   (A) What was the actual outcome of the 6 iterations of this branch instruction?

   (B) What is the BHT entry after predicting the 6^{th} iteration of this branch instruction?

Main conclusions from data given in the question: Given that, every alternate branch is mis-predicted. ie, the last column entries (Mis-Pred in the following table) will be always in the format of alternating N and T. The first branch was predicted.

Sl.no	Last 2 br	BHT NN/NT/TN/TT	Prediction	Actual	Miss - Pred
1.	NN	**00**/00/11/11	N	T	YES
2.	NT	01/**00**/11/11	N	N	NO
3.	TN	01/00/**11**/11	T	N	YES
4.	NN	**01**/00/10/11	N	N	NO
5.	NN	**00**/00/10/11	N	T	YES
6.	NT	01/**00**/10/11	N	N	NO
		01/00/10/11			

- The second column in the table above ie, the entry which represents the last two branches has to be interpreted in the following way. The second element in the entry represents the outcome of the latest iteration of the branch. Eg: Refer last 2 br of 2nd row. It is given as NT. This means the latest branch was T (Taken) and second last branch was N (Not Taken).
- Red color in the table shows the entry in the table that is referred to take the decision. Only that entry may change in the next row depending on whether the prediction is correct or not. The change on the entry is based on transitions and state change on 2 -bit automata used for predictor.

(a) Outcome of last 6 branches. – **T N N N T N** (last entry is the latest iteration)

(b) BHT entry after for **NN/NT/TN/TT** after 6 iterations is **01/00/10/11**