IIT Guwahati - Department of Computer Science & Engineering

CS 223- Computer Organization & Architecture

Practice Tutorial Sheet #2 [04.05.2020]

1. In a dynamically issued speculative superscalar processor the reservation station entries of two functional units (Mul and Add) at clock cycle T is as shown below. At T, none of the instructions waiting in the reservation station have started execution.

Name	Busy	Op	Vj	Vk	Qj	Qk	Dest	A
Mul	Yes	FMUL	8	5	0	#4	#5	40
Mul	Yes	FDIV	2	8	#6	0	#7	20

Name	Busy	Op	Vj	Vk	Qj	Qk	Dest	A
Add	Yes	FADD	8	5	#4	#5	#6	10

   (A) Write any possible sequence of three instructions (in the order of issue) along with their corresponding register operands that could result in the reservation station entries shown above. Only F1, F2 and F3 can be used as the operands for the instructions. Instruction syntax should be of the form: *Opcode DestReg, SrcReg1, SrcReg2*.

   (B) State other mandatory conditions (if any) that should hold at the time of issue of these instructions to ensure the correctness of the above entries.

2. Consider a dynamically scheduled single issue instruction pipeline with speculation using a branch predictor that always predicts the branch as taken. The pipeline has one FP-multiplier that takes 4 cycles for execution, one FP-adder that takes 2 cycles for execution, one integer unit that takes 1 cycle for execution and one memory address unit that takes 1 cycle to compute effective address for load and store operations. All the integer and FP units are fully pipelined and support operand forwarding. Memory access for a load operation takes place in the next cycle after the address computation. Store operation access memory only upon commit. This speculative pipeline is implemented with a 4-entry ROB. Assume that instruction issue will not be stalled due to availability of reservation stations. Consider the following code with 9 instructions (I1-I9).

   Initial values of registers are as follows: F1← a, F2← b, F3← c, R2← 200, R3← 240

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I1-lxx: L.D F4, 0(R2)          ; load X
I2-     MUL.D F5, F4, F4
I3-     MUL.D F5, F5, F1
I4-     MUL.D F4, F4, F2
I5-     ADD.D F6, F5, F4
I6-     ADD.D F6, F6, F3
I7-     S.D F6, 48(R2)         ; store Y
I8-     ADDI R2, R2, #8
I9-     BNE R2,R3, lxx         ; branch to lxx if R2!=R3
```

   Fill up the time of issue, execution, memory access, CDB write and commit for one iteration of the loop in the table given below. Answer the questions given below the table.

	Instruction	Issue	Execute	Memory Access	CDB Write	Commit
I1	L.D F4, 0(R2)	1	2	3	4	5
I2	MUL.D F5, F4, F4	2				
I3	MUL.D F5, F5, F1					
I4	MUL.D F4, F4, F2					
I5	ADD.D F6, F5, F4					
I6	ADD.D F6, F6, F3					
I7	S.D F6, 48(R2)					
I8	ADDI R2, R2, #8					
I9	BNE R2,R3, lxx					

From the duly filled table answer the following questions.

(A) In which clock cycle I4 write result to CDB?

(B) In which clock cycle I6 is issued?

(C) In which clock cycle I7 access memory?

(D) In which clock cycle I8 starts execution?

(E) What is the relation between X and Y in terms of a, b and c?

(F) How many times the loop will be iterated?