Some sample submission for “ASM Chart Multiplier”

Verilog file and Testbench

Sample format for submission:

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Verilog file:

```
module MULTPLIER(
    input  [3:0] A,
    input  [3:0] B,
    input clk,
    output [7:0] O
);
reg [3:0] a ;
reg [4:0] b ;
reg [3:0] c ;
reg [3:0] count;
always @(A or B)
begin
    a = A;
    b = 0;
    c = B;
    count = 0;
end


always @(posedge clk)
begin
    $display("output",O);
    if(!(count == 5))
    begin
```

```
        if(c[0])
        begin
            c = c >> 1;
            c[3] = b[0];
            b = b >> 1;
            b = b + a;
        end
        else
        begin
            c = c >> 1;
            c[3] = b[0];
            b = b >> 1;
        end
        count++;
    end


end


assign O[7:4] = b[3:0];
assign O[3:0] = c[3:0];
endmodule
```

Test bench

```
`timescale 1ns / 1ps
module TEST_BENCH;


reg [3:0] A;
```

```
reg [3:0] B;
wire [7:0] O;
reg clk = 0;


integer i;
initial begin
    for(i = 0;i<300;i++)
    begin
    #5 clk = ~clk;
    end
end



initial begin
A = 4;
B = 5;
#90
A = 3;
B = 3;
#90
A = 9;
B = 8;
#90
A = 15;
B = 12;
end
```

```
initial
begin
    $dumpfile("MULT.vcd");
    $dumpvars(0,TEST_BENCH);
end


MULTPLIER m(
    A,
    B,
    clk,
    O
);


endmodule
```