IIT Guwahati - Department of Computer Science & Engineering

CS 223- Computer Organization & Architecture

Practice Tutorial Sheet #1 [23.04.2020]

1. Given a non-pipelined architecture running at 1.5 GHz, that takes 5 cycles to finish an instruction. You want to make it pipelined with 5 stages. Due to hardware overhead the pipelined design will operate only at 1 GHz. 5% of memory instructions cause a stall of 50 cycles, 30% of branch instruction cause a stall of 2 cycles and load-ALU combinations cause a stall of 1 cycle. Assume that in a given program, there exist 20% of branch instructions and 30% of memory instructions. 10% of instructions are load-ALU combinations. What is the speedup of pipelined design over the non-pipelined design?
2. In a program there was a branch instruction which is iterated 6 times. The processor uses a (2,2) correlating branch predictor. The outcome of the last two branches is used to index into the BHT. Each entry of BHT is a 2-bit value that is updated by a standard 2-bit predictor automata. Let the initial entry of the BHT for NN/NT/TN/TT is 00/00/11/11, respectively. It was found that the branch predictor has an accuracy of 50% with every alternate iteration of the branch predicted correctly. The first iteration of the branch was mis-predicted. The BHT is indexed with an NN value initially.
   (A) What was the actual outcome of the 6 iterations of this branch instruction?
   (B) What is the BHT entry after predicting the 6^{th} iteration of this branch instruction?