Constraint file:

```
set_property PACKAGE_PIN W7 [get_ports {seg[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[7]}]
set_property PACKAGE_PIN W6 [get_ports {seg[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]
set_property PACKAGE_PIN U8 [get_ports {seg[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
set_property PACKAGE_PIN V8 [get_ports {seg[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
set_property PACKAGE_PIN U5 [get_ports {seg[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property PACKAGE_PIN V5 [get_ports {seg[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property PACKAGE_PIN U7 [get_ports {seg[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property PACKAGE_PIN V7 [get_ports {seg[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]
```

```
set_property PACKAGE_PIN W4 [get_ports {anoact[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anoact[3]}]
set_property PACKAGE_PIN V4 [get_ports {anoact[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anoact[2]}]
set_property PACKAGE_PIN U4 [get_ports {anoact[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anoact[1]}]
set_property PACKAGE_PIN U2 [get_ports {anoact[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anoact[0]}]
```

```
set_property PACKAGE_PIN W5 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports clk]

set_property PACKAGE_PIN R2 [get_ports B1]
set_property IOSTANDARD LVCMOS33 [get_ports B1]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B1_IBUF]

set_property PACKAGE_PIN T1 [get_ports B2]
set_property IOSTANDARD LVCMOS33 [get_ports B2]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B2_IBUF]


set_property PACKAGE_PIN U1 [get_ports B3]
set_property IOSTANDARD LVCMOS33 [get_ports B3]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B3_IBUF]

set_property PACKAGE_PIN W2 [get_ports B4]
set_property IOSTANDARD LVCMOS33 [get_ports B4]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B4_IBUF]

set_property PACKAGE_PIN R3 [get_ports B5]
set_property IOSTANDARD LVCMOS33 [get_ports B5]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B5_IBUF]

set_property PACKAGE_PIN T2 [get_ports B6]
set_property IOSTANDARD LVCMOS33 [get_ports B6]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B6_IBUF]

set_property PACKAGE_PIN T3 [get_ports B7]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports B7]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B7_IBUF]

set_property PACKAGE_PIN V2 [get_ports B8]
set_property IOSTANDARD LVCMOS33 [get_ports B8]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B8_IBUF]
set_property PACKAGE_PIN W13 [get_ports B9]
set_property IOSTANDARD LVCMOS33 [get_ports B9]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets B9_IBUF]
```