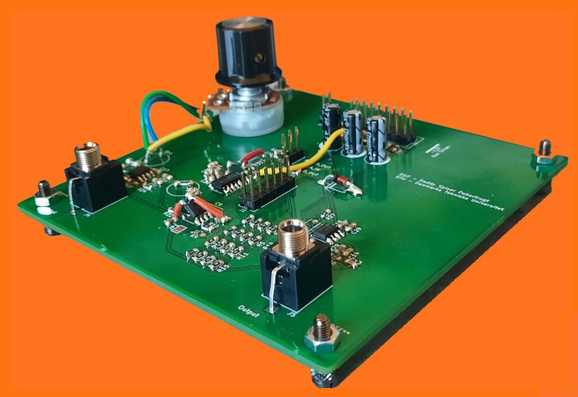
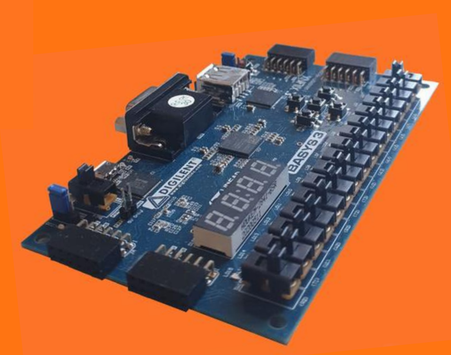
GRP 9





C.A.P.N.A

Complimentary Audio Processor Network Architecture

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Abstract:

We propose CAPNA: A Complementary Audio Processing Network Architecture which accelerate audio algorithms and enables users to program Linear and non-linear audio processors on FPGA technology using application specific hardware accelerators and ΣΔ AD- and DA conversion following the Eurorack specifications.

Problem definition

Due to chip shortages, integrated circuits has become more expensive. Yet, the demand for higher performance is growing in the audio industry. Using a reprogrammable processor could trim the amount of hardware needed, and still boost the performance.

Our goal with this project will be *to implement Audio DSP using reprogrammable FPGA tech.* To achieve this, we need to solve the following problems:

- What architecture would be advantageous for implementing a digital signal processing system through FPGA technology?
- What are the capabilities of the DSP slices available
- How can the system be made compliant with Line level signals and/or Eurorack specifications.
- What tools could we use to create an open-source platform

Testing this could offset some of the chip shortage problems related to Audio DSP components as the on-the-go reconfigurabilty would create an alternative environment for digital implementation of linear and non-linear effects.

Methods

Preliminary research on the different parts of the project was the initial step in drafting implementation ideas for the filtering, AD/DA conversion, and processor architecture

The implementation of a FIR-filter was done since the concept would be relatively simple to implement.

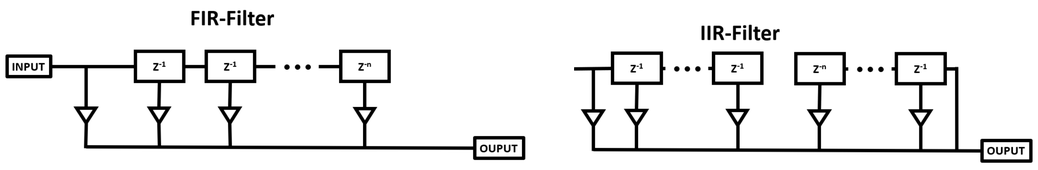

Fig. 2 The block diagrams of IIR filters (left) and FIR filters (right).

Some of the design methods used in the design workflow were group discussions, simulations of analog designs prior to testing. and generating VCD files with programs like chisel test.

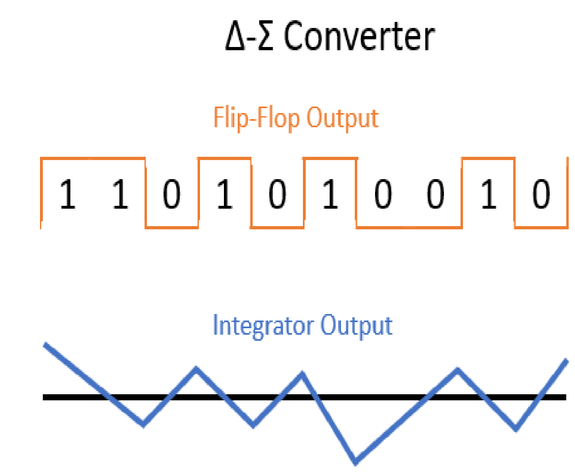

Fig. 1. Working principle of a Delta-Sigma ADC. A voltage over an integrator is compared to the last sampled bit, in order to generate the next bit.

Testing the ADDAC system was done in steps. First the DAC was tested and verified, as this made testing the ADC easier, since it was tested on an arduino nano, which has no ADC itself. The topologies were chosen due to its low cost compared to the theoretical SNR.

CAPNA is designed to be more than a computer architecture, but a framework to create application specific processor networks.

The individual processors consist of a RISC CPU and a DSP hardware accelerator for filtering, this gives us both the flexility of a general-purpose processor, as well as the speed of a hardware accelerator.

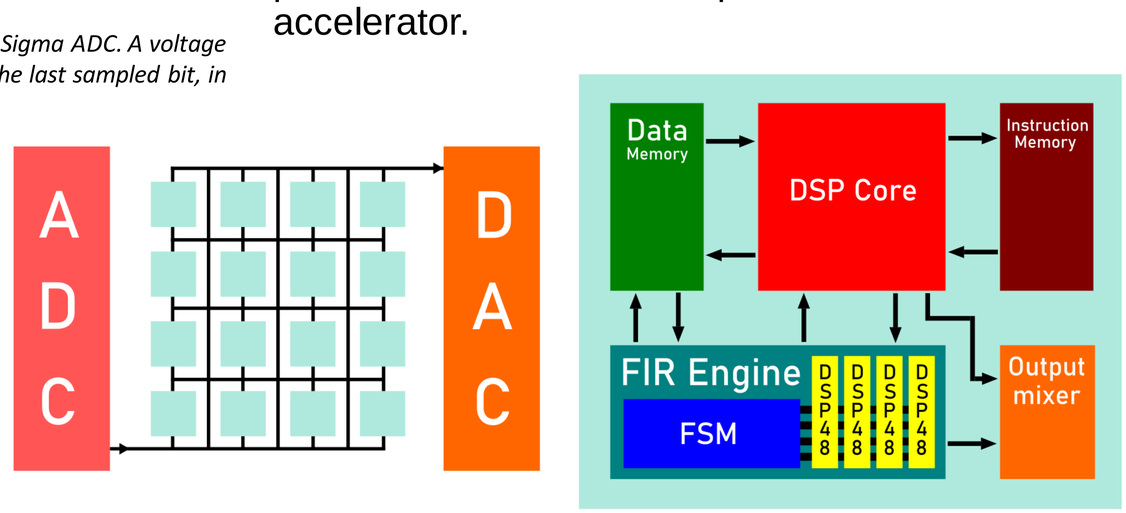

Fig. 3 The architecture of a single CAP processor (right), and the architecture of the whole design (left) .

Analysis

We found that sigma delta modulation for conversion between analog and digital signals for the FPGA is viable. We did encounter a bottleneck in the form of the switching speed of the comparator, which didn't allow for as deep a bit depth/sampling speed as desired. We were not able to filter the input or output, and we did experience a lot of noise after the conversions, but the audio was still recognizable.

We were able to make reconfigurable processors (CAPs) and configure these from XML presets. Furthermore, we were able to connect these processors in different ways

The implemented processor uses about (refer to table with resource use)

	LUT	FF	BRAM	DSP
Utilization	1666	636	1	2

Discussion

We still believe it to be possible to implement such a solution. Our current product is very much a prototype with a lot of flaws, which would have to be improved upon for it to achieve acceptable performance. We would need to find a faster comparator and debug the problems regarding the input/output filtering.