

# Lab Report for EE381A

2022-23(II)

MOHAN KRISHNA  
200590

## Section D

Department of Electrical Engineering  
30 January, 2022: 01:45 am

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# **LAB-1 and LAB-2:**

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## **Design and Implementation of a BJT Operational Amplifier**

### **Pre Lab:**

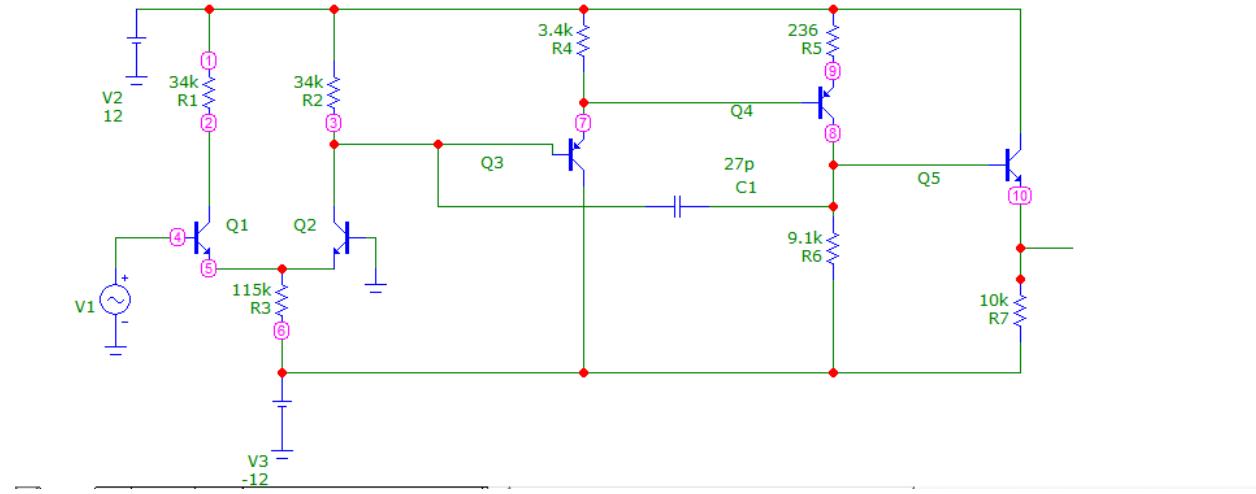
#### **Design Methodologies:**

OP-AMP required: Gain>1000. Input Resistance>10000 Ohm. Output Resistance <100 Ohm.

First stage is a differential amplifier, which provides maximum small signal gain. For a large enough input resistance, the resistor attached as a current source should be large, hence the choice of 115k resistor. Moreover, 34k resistor at the collector gives a large enough small signal gain of first stage. Second stage is a buffer, so that the input to the third stage has a large enough input resistance. Similarly the last stage is also a buffer, with base resistance of 10k so that the output resistance is low. Note that the values of 236 and 9.1k for the third stage are chosen such that the loading to stages is minimized, and gain which we get appends to the differential amplifier gain to get the required overall gain. If we want to alter the dc bias at output(in lab, in case the parameters of transistor and resistor don't match the theoretical values), we need to change the 9.1k resistor, because it feeds into the last stage ( $V_{be}$  is approx. 0.7).

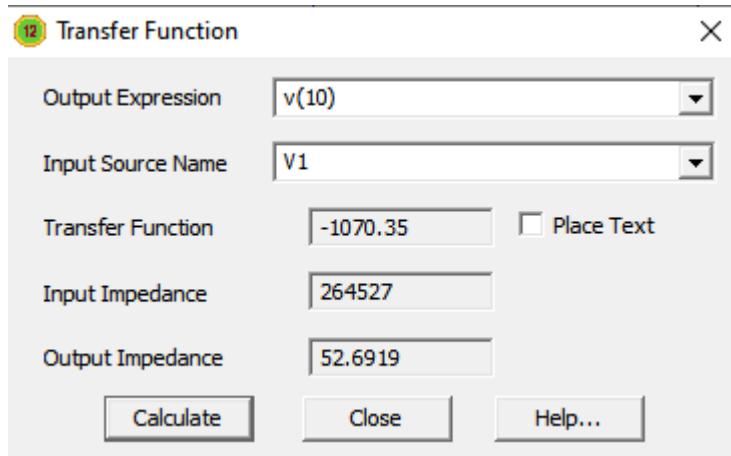
The capacitor value of 27 pF is chosen so that the pole we get is around 5kHz.

## Microcap Circuit:



## Op-Amp Characteristics:

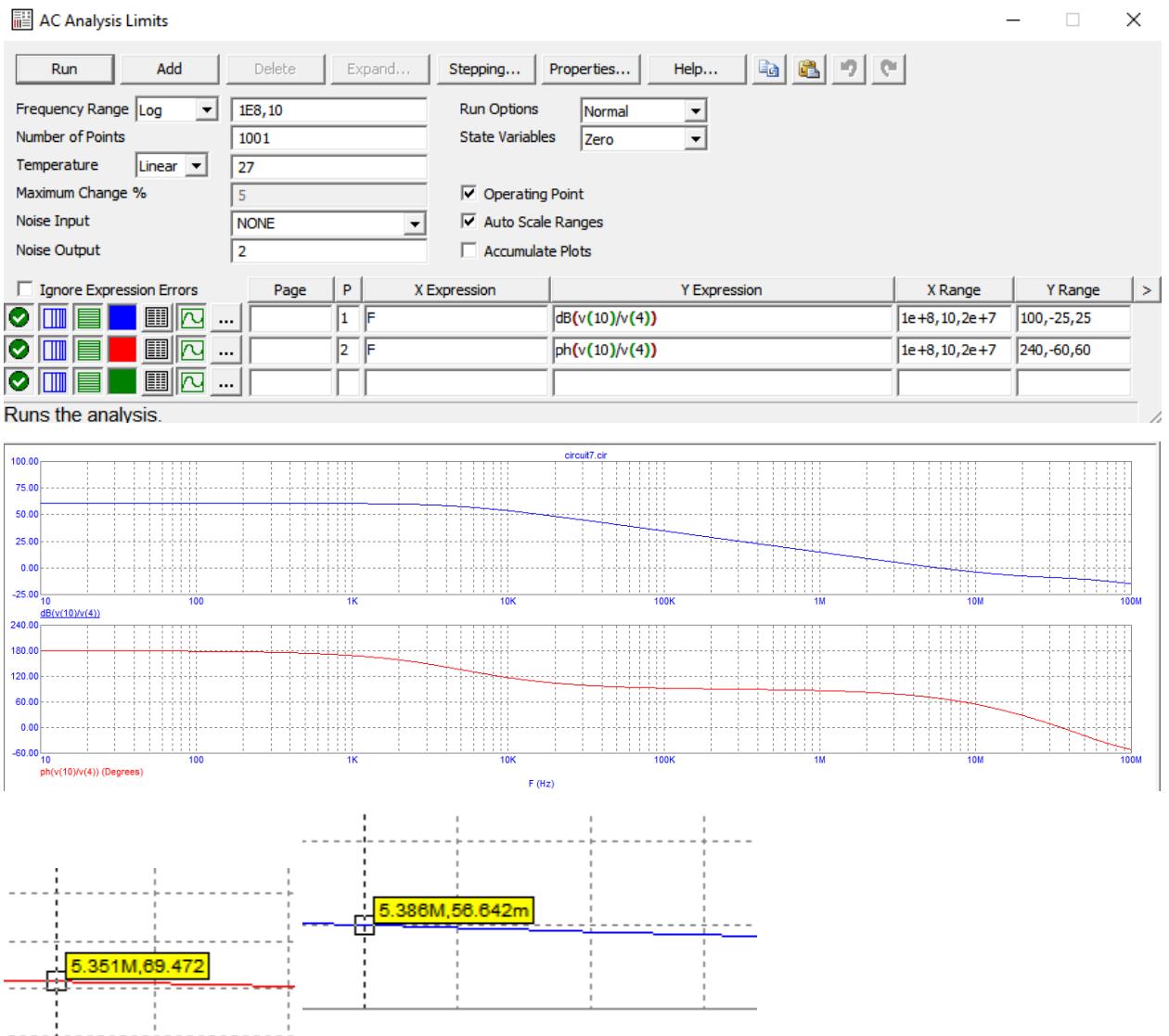
- Transfer Function: As we can see the required specifications of op-amp are met quite well, with a some margin (at least in the simulation).



- DC Bias=0 (as set in simulation).
- Small Signal Gain:  $-1070.35 = A_{V3}$ .  $R_C = 34k$ .
- Gain and Phase Plot (With capacitor):

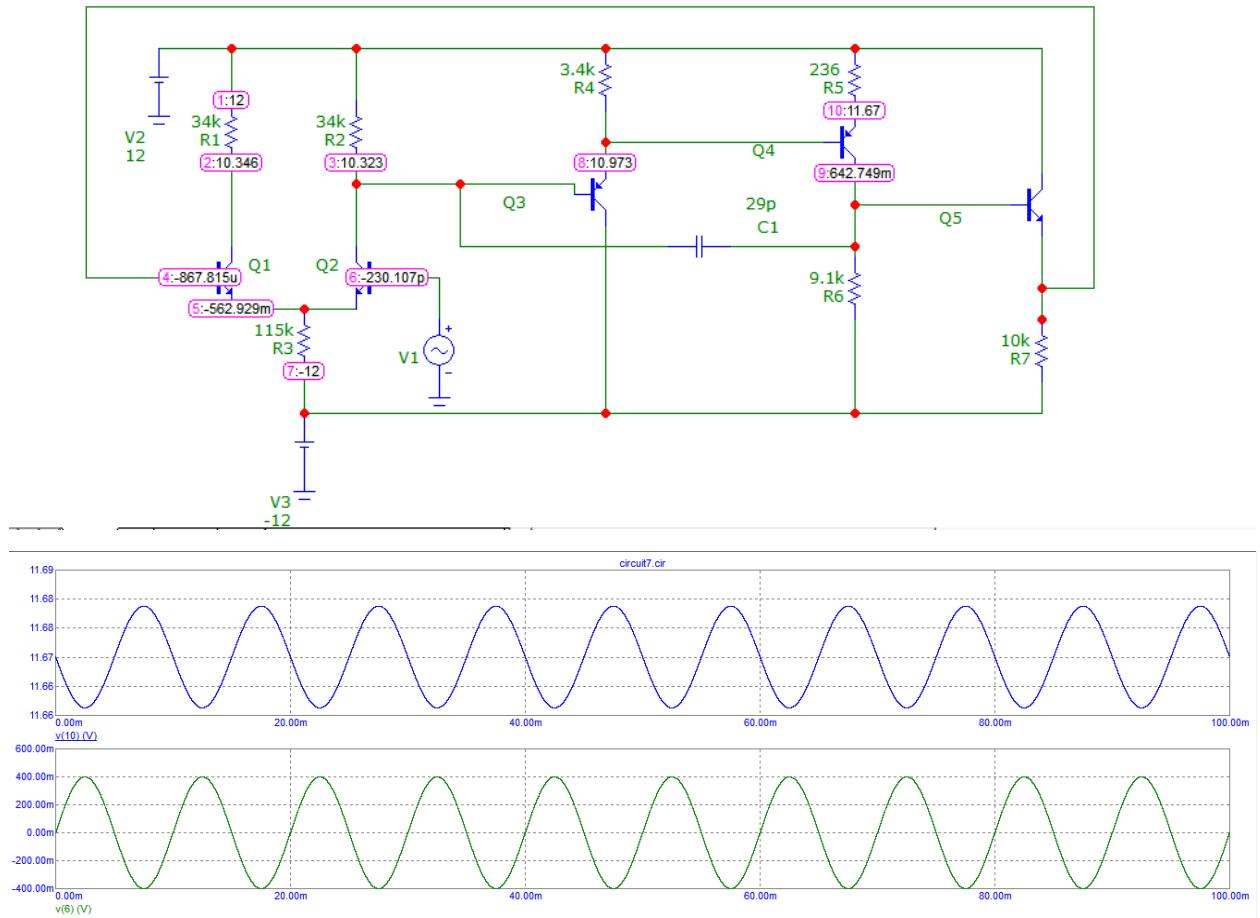
$$p = \frac{1}{2\pi R_C \times C_C \times (1 - A_{V3})} = 5\text{KHz}$$

$$C_C \cong 27\text{ pF}$$



Note that in the lab, we need to increase the phase margin, and for that, using Gain-Bandwidth product's invariant ness, we need to increase Gain.

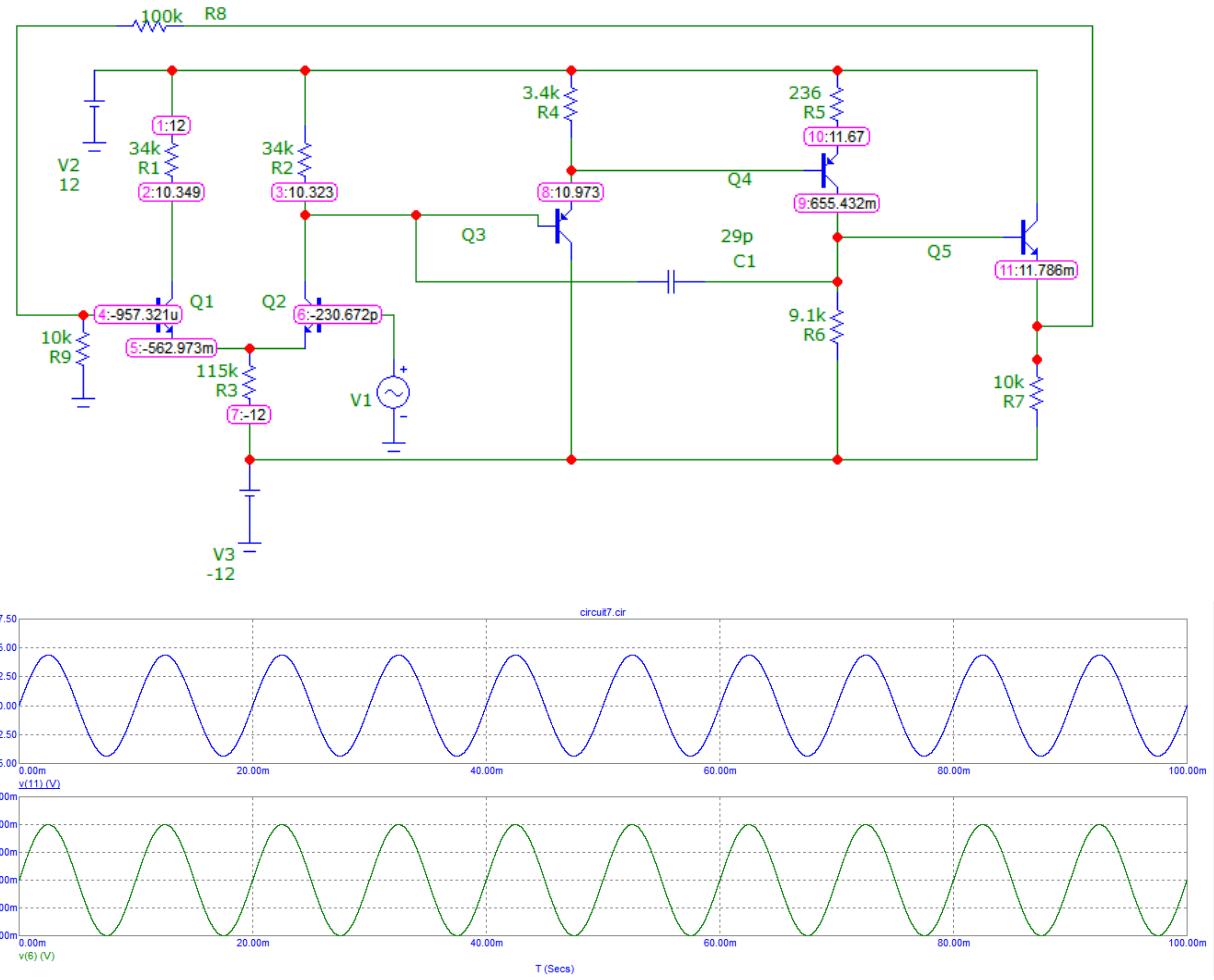
- Voltage Follower:



Blue=Input

Green=Output

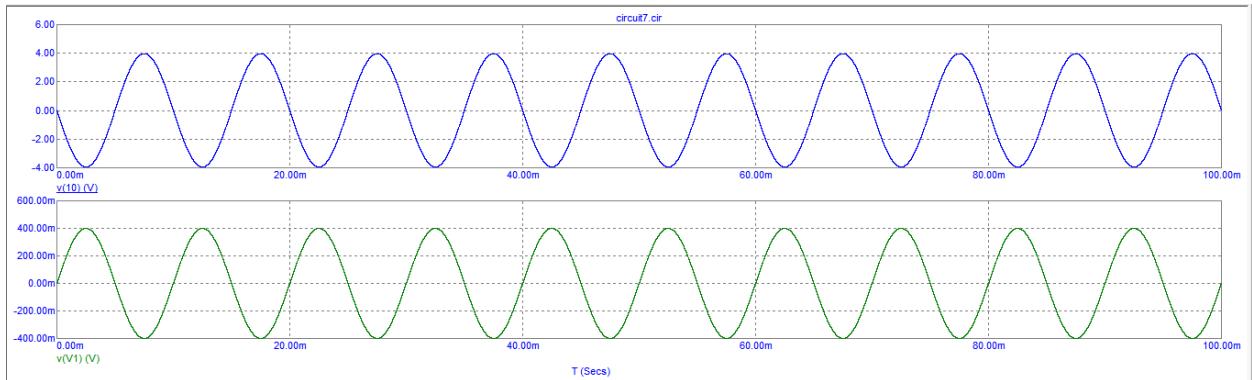
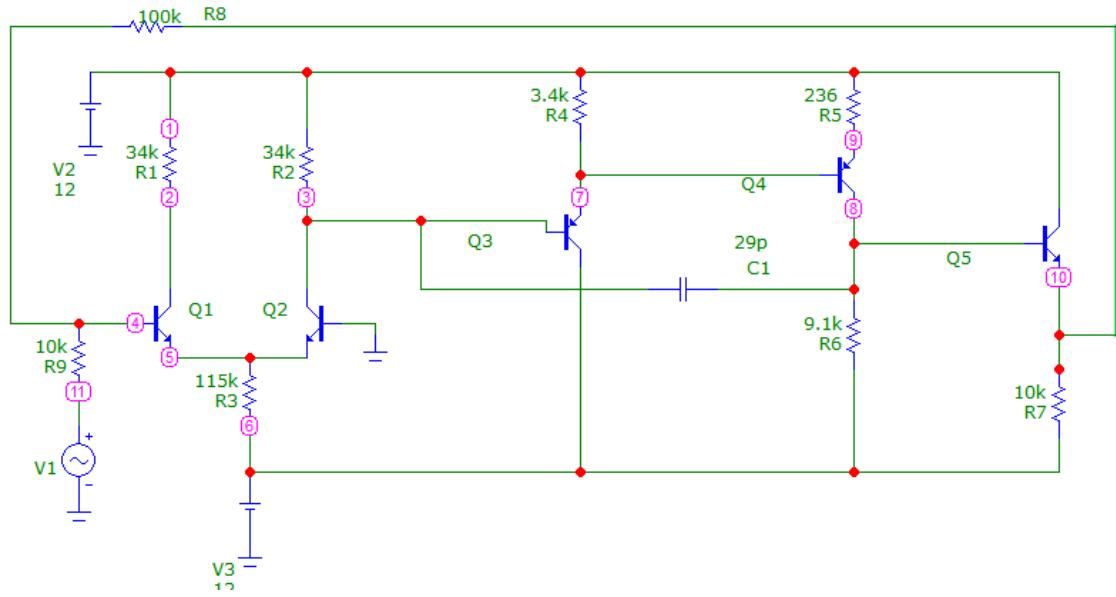
- Non-Inverting Amplifier



Blue=Output

Green=Input

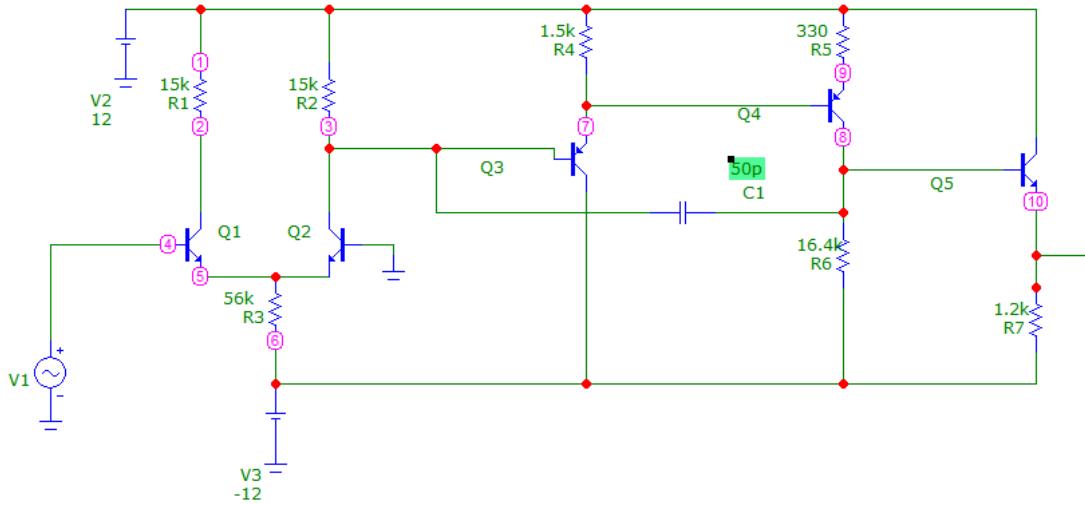
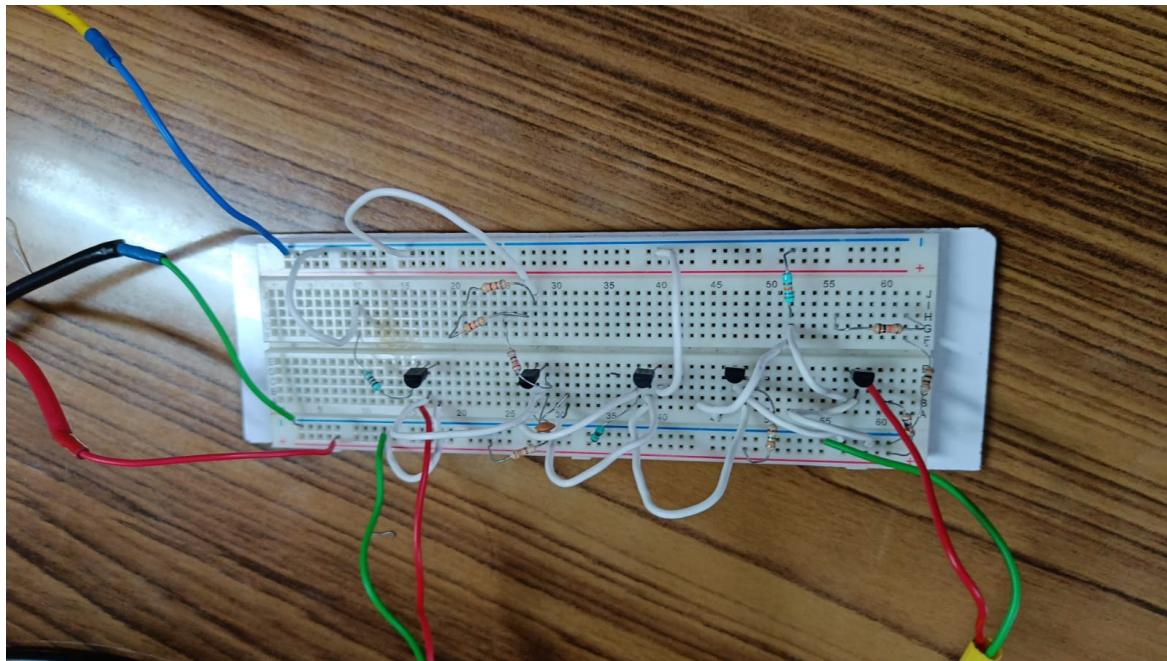
- Inverting Amplifier:



Green=Input  
Blue=Output

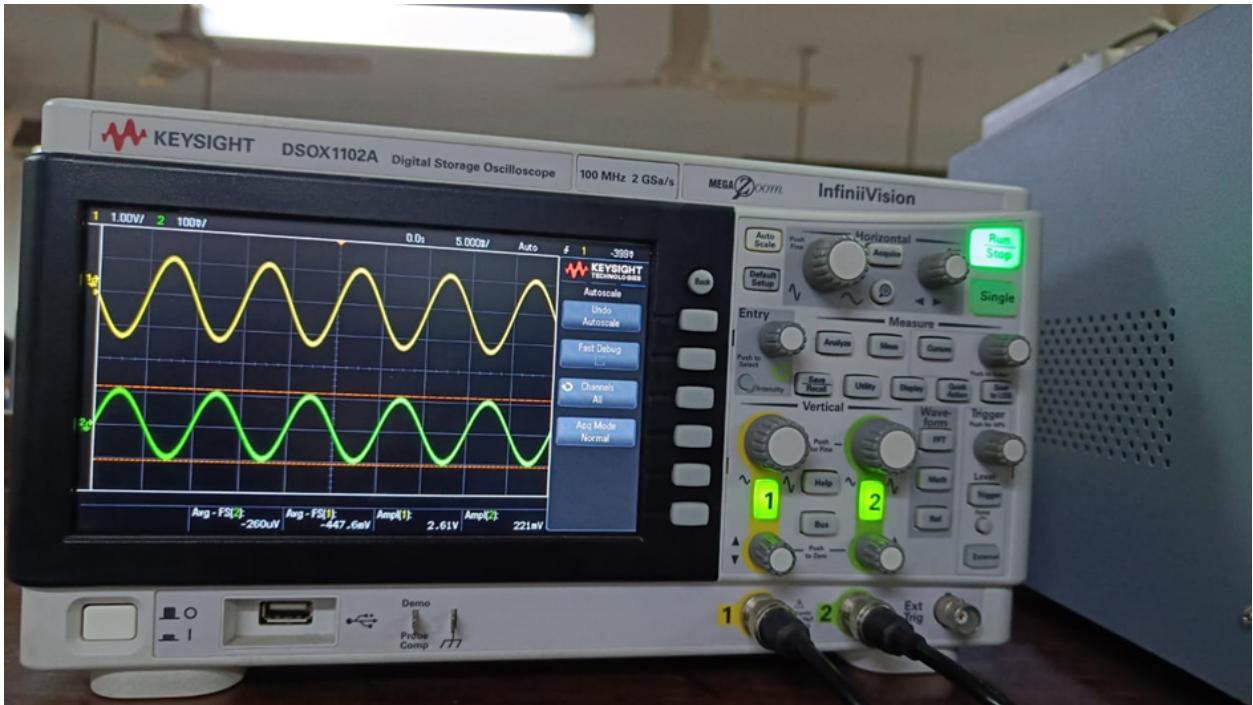
# In Lab and Post Lab:

Circuit Bread-Board:



**Note:** The values of the resistors are altered because the parameters of actual transistors (eg  $V_{fe}$ ) aren't equal to the theoretical values, due to manufacturing variations. The values are empirical, obtained by altering such that the DC bias becomes zero, and remaining values are approx. half the values of resistors used in the original circuit (done to improve the frequency response).

## Open Loop Gain:



$$V_{in} = 2.21\text{mV}$$

$$V_{out} = 2.61\text{V}$$

$$A_v = V_{in}/V_{out} = 1180.99$$

This value is in accord with the specifications which we require.

This gain wouldn't equal the simulation value of gain, because of process variations from the manufacturer's side.

**Important Note:** Since amplitude of 2 mV isn't possible from the function generator, because of cross-talk and ambient noise, we have used an input of 200 mV sine wave from the function generator, and used a resistive divider of 1 Mega Ohm and 10 kilo Ohm resistors.

## Frequency Response Without Compensation:

Note that the maximum frequency that can be given by the function generator has an upper limit, but the unity gain frequency without compensation is even higher than that. Hence, we can only approximate values of capacitor required, from estimate. The values are plotted.

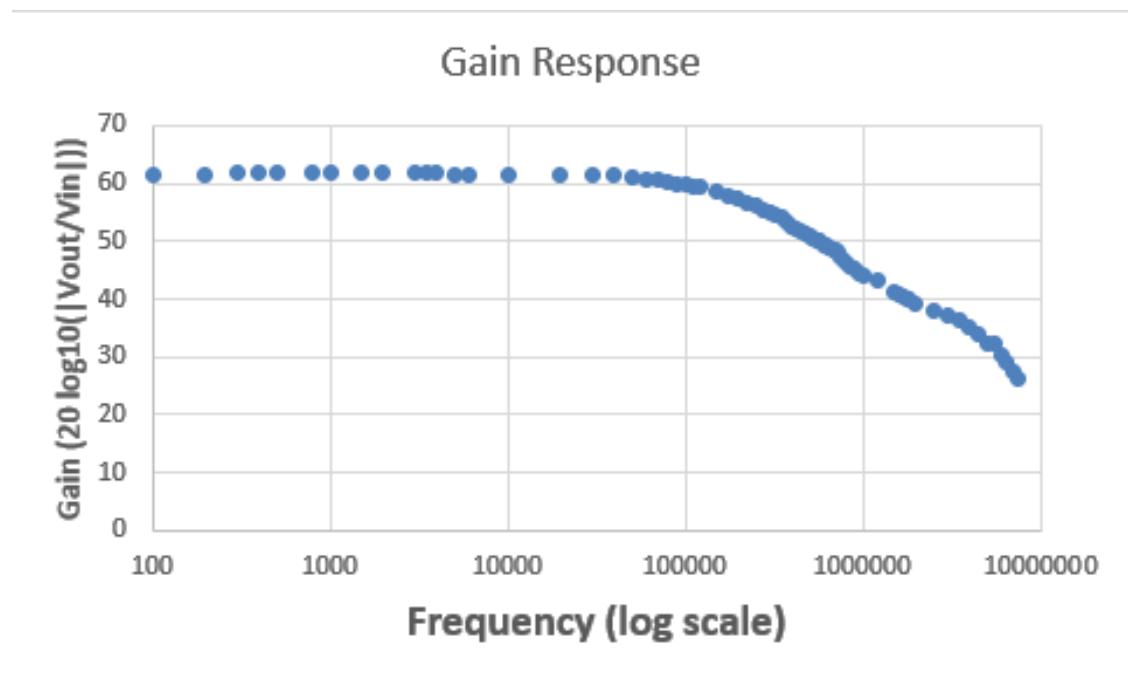
<b>Frequency</b> <b>(Hz)</b>	<b>Vin*100</b> <b>(Volts)</b>	<b>Vout</b> <b>(Volts)</b>	<b>Gain</b> <b>(dB)</b>	<b>Phase</b> <b>(degrees)</b>
100	0.221	2.65	61.57707	180
200	0.221	2.65	61.57707	180
300	0.221	2.69	61.7072	180
400	0.221	2.69	61.7072	180
500	0.221	2.7	61.73943	180
800	0.221	2.73	61.83541	180
1000	0.221	2.73	61.83541	180
1500	0.221	2.73	61.83541	180
2000	0.221	2.7	61.73943	180

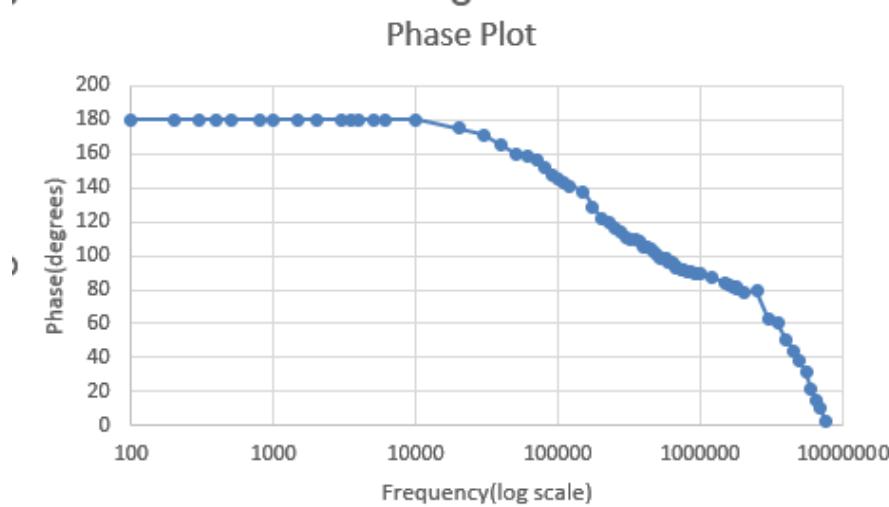
3000	0.221	2.69	61.7072	180
3500	0.221	2.69	61.7072	180
4000	0.221	2.69	61.7072	180
5000	0.221	2.65	61.57707	180
6000	0.221	2.65	61.57707	180
10000	0.221	2.65	61.57707	180
20000	0.221	2.63	61.51127	175
30000	0.221	2.6	61.41162	171
40000	0.221	2.57	61.31082	165
50000	0.221	2.49	61.03614	160
60000	0.221	2.44	60.85995	159
70000	0.221	2.37	60.60712	156
80000	0.221	2.29	60.30886	152
90000	0.221	2.21	60	148
100000	0.221	2.17	59.84135	145
110000	0.221	2.09	59.51508	143
120000	0.221	2.05	59.34723	141
150000	0.221	1.85	58.45559	138
175000	0.221	1.73	57.87308	129

200000	0.221	1.61	57.24867	122
225000	0.221	1.49	56.57588	120
250000	0.221	1.45	56.33951	116
275000	0.221	1.33	55.58919	114
300000	0.221	1.25	55.05035	111
325000	0.221	1.17	54.47587	110
350000	0.221	1.11	54.01861	110
375000	0.221	1.01	53.19858	109
400000	0.221	0.94	52.57471	105
425000	0.221	0.9	52.197	105
450000	0.221	0.85	51.70053	104
475000	0.221	0.82	51.38843	102
500000	0.221	0.78	50.95405	100
525000	0.221	0.74	50.49679	98
550000	0.221	0.72	50.2588	98
575000	0.221	0.7	50.01412	98
600000	0.221	0.66	49.50303	96
625000	0.221	0.64	49.23575	96
650000	0.221	0.62	48.95999	95

675000	0.221	0.6	48.67518	93
700000	0.221	0.58	48.38071	93
725000	0.221	0.56	48.07592	92
750000	0.221	0.51	47.26356	92
800000	0.221	0.47	46.55411	91
850000	0.221	0.43	45.78152	91
900000	0.221	0.4	45.15335	90
950000	0.221	0.37	44.47619	90
1000000	0.221	0.35	43.99352	89
1200000	0.221	0.32	43.21515	87
1500000	0.221	0.255	41.24296	84
1600000	0.221	0.24	40.71638	83
1700000	0.221	0.23	40.34671	82
1780000	0.221	0.22	39.96061	82
1800000	0.22	0.223	40.11764	81
2000000	0.223	0.205	39.26898	78.8
2500000	0.225	0.177	37.91581	79
3000000	0.202	0.146	37.18003	63
3500000	0.226	0.147	36.26418	60

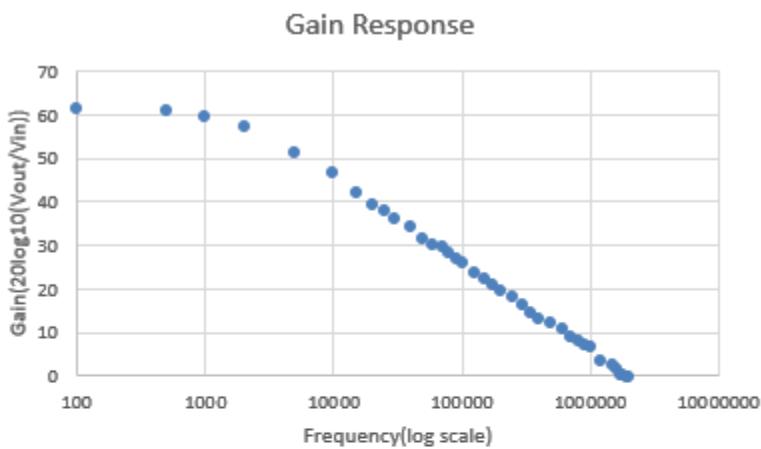
4000000	0.221	0.128	35.25635	50
4500000	0.229	0.116	34.09245	44
5000000	0.409	0.172	32.4761	38
5500000	0.4	0.163	32.20255	31
6000000	0.41	0.137	30.47873	21
6500000	2.13	0.595	28.92275	15
7000000	2.15	0.514	27.57049	10
7500000	2.16	0.452	26.41369	3

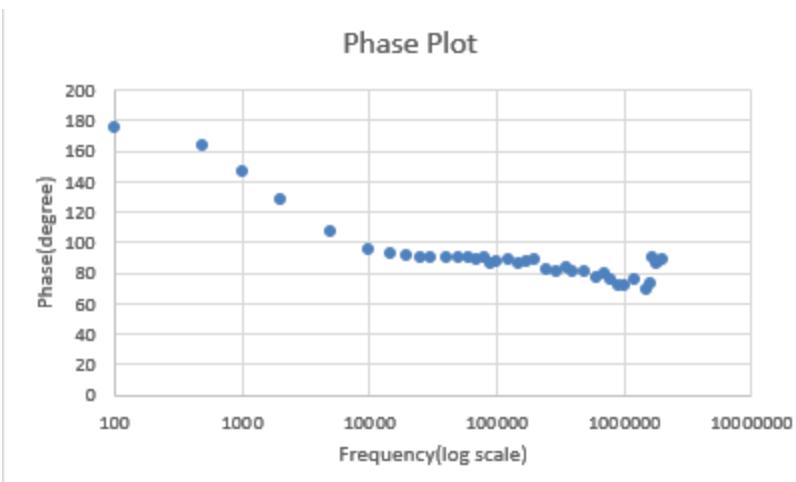




As we can see, the gain doesn't go to 0dB even at very high frequencies. Hence, we can try a 50 pF capacitance, and see how “after compensation” plot looks like(hoping to get enough phase margin):

### **Frequency Response After Compensation:**





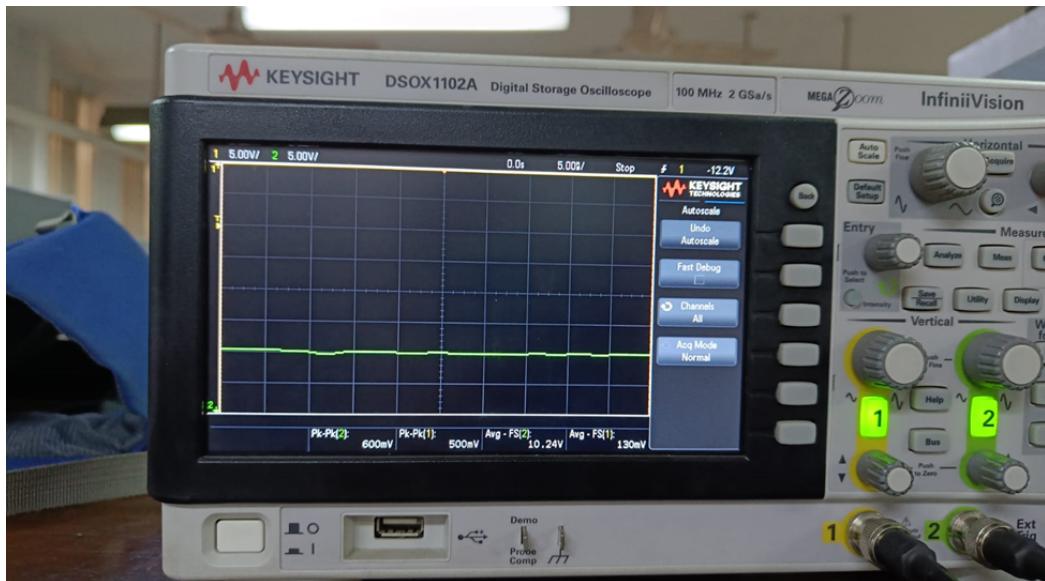
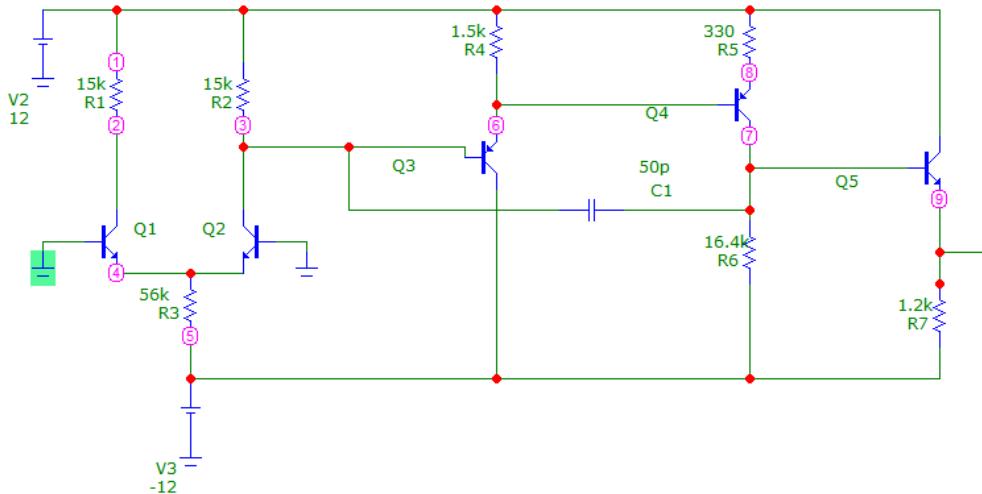
<b>Frequency</b> <b>(Hz)</b>	<b>Vin*100</b> <b>(Volts)</b>	<b>Vout</b> <b>(Volts)</b>	<b>Phase</b> <b>(degrees)</b>	<b>Gain</b> <b>(dB)</b>
100	0.225	2.57	175.81	61.15501
500	0.225	2.49	163.05	60.88034
1000	0.225	2.21	146.68	59.8442
2000	0.225	1.63	128.31	57.2001
5000	0.225	0.86	107.08	51.64632
10000	0.221	0.5	95.59	47.09155
15000	0.225	0.285	92.81	42.05325

20000	0.221	0.217	91.34	39.84135
25000	0.322	0.253	90.52	37.90529
30000	0.322	0.217	90.35	36.57208
40000	0.322	0.161	89.98	33.9794
50000	0.63	0.253	90.02	32.0756
60000	0.63	0.213	90.4	30.58078
70000	0.64	0.193	88.91	29.58755
80000	0.63	0.169	90.07	28.57092
90000	0.63	0.149	86.39	27.47691
100000	0.63	0.127	87.01	26.08926
125000	0.63	0.101	88.73	24.09962
150000	2.13	0.277	86	22.282
175000	2.13	0.245	86.97	21.21573
200000	2.09	0.209	88.14	20
250000	2.13	0.173	81.7	18.19333
300000	2.17	0.149	80.7	16.73453
350000	4.3	0.237	83.4	14.8256
400000	4.3	0.205	80.7	13.56571
500000	4.2	0.177	81.4	12.49448

600000	4.3	0.145	76.7	10.55799
700000	4.3	0.129	79.6	9.542425
800000	4.3	0.117	75	8.694348
900000	4.3	0.101	71.4	7.417058
1000000	4.3	0.096	72	6.976056
1200000	8.6	0.137	75	4.044442
1500000	8.8	0.115	69.4	2.324303
1600000	12.7	0.157	73.2	1.841919
1700000	16.7	0.185	89.8	0.889105
1800000	16.7	0.177	85.7	0.505136
1900000	16.7	0.173	87.3	0.306593
2000000	16.5	0.165	88.4	0

Phase Margin is 88.4 degrees, unity gain frequency is 2MHz, which is in accord to the capacitor value of 50pF chosen. Note: Because of the large value of capacitor chosen(hence larger phase margin than required 75 degrees), it is quite possible that the slew rate would be lower, hence the op amp won't work properly for very fast changing input.

## Offset Voltage:

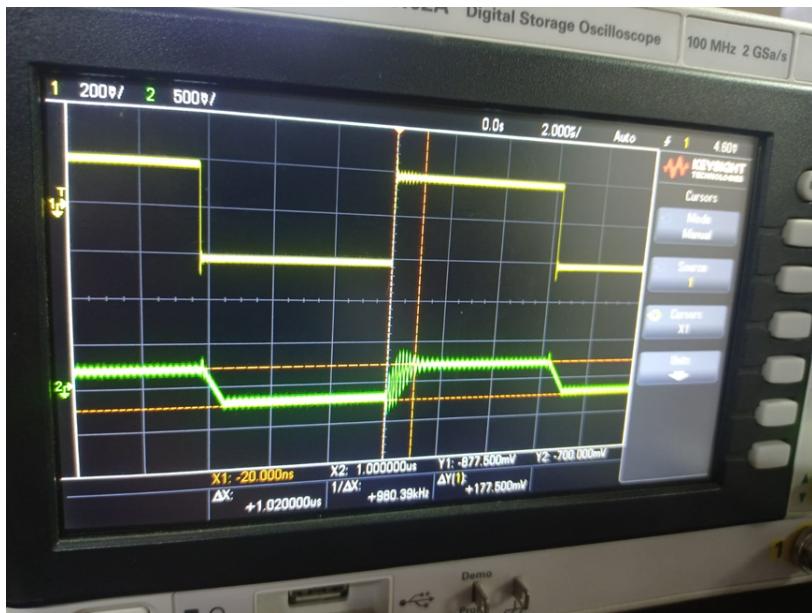


Circuit diagram is shown above, followed by output.  $V_{out}$  (Avg-FS(1) column) is approximately 0V. Hence, there is NO dc offset. This is obvious, since we had altered the resistors in 3rd stage so that there is no dc offset.

**Slew Rate:** Note: there are small oscillations in the rising edge which die out because of the large value of the capacitor used.



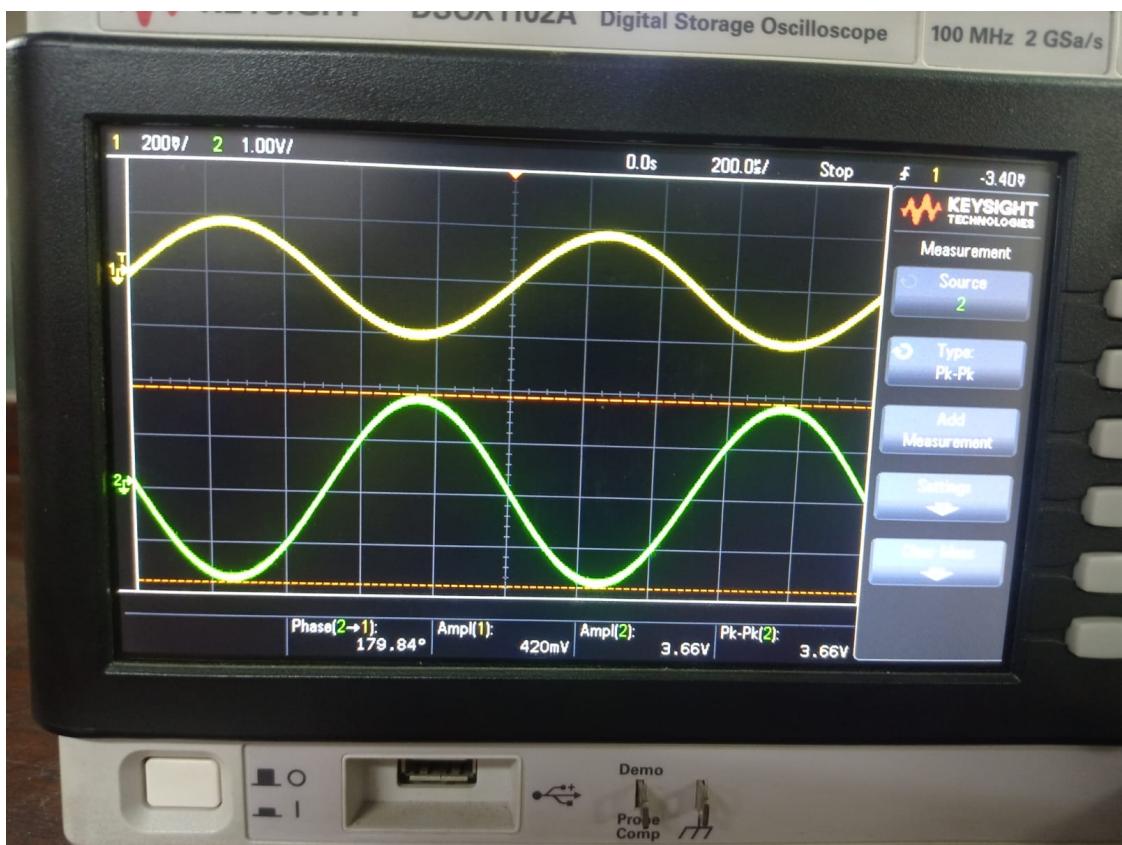
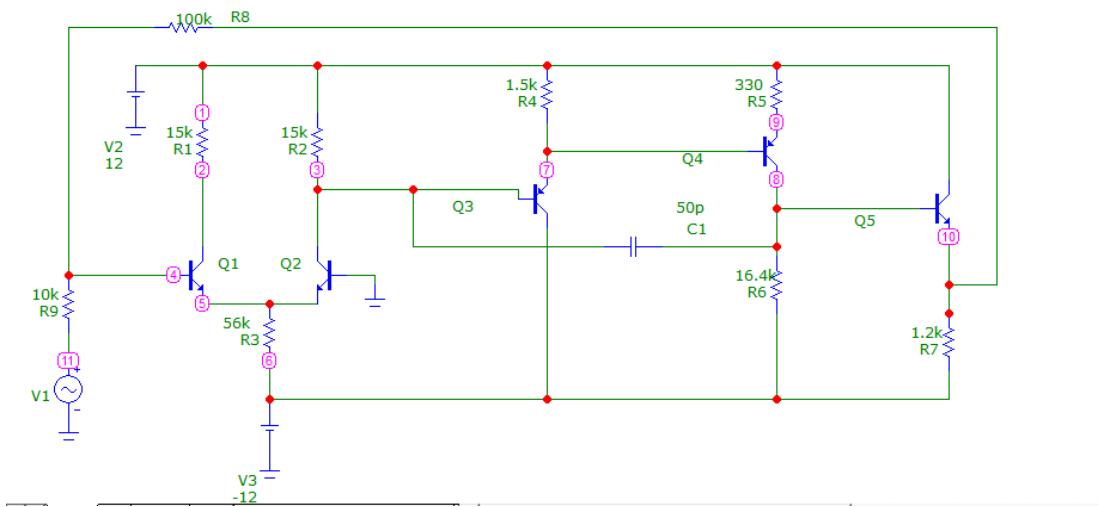
$$\Delta V/\Delta t \text{ (falling edge)} = 177.5\text{mV}/0.72\mu\text{s} = 0.246 \text{ V}/\mu\text{s}$$



$$\Delta V/\Delta t \text{ (rising edge)} = 177.5\text{mV}/1.02\mu\text{s} = 0.174 \text{ V}/\mu\text{s}$$

Hence, Slew Rate is **0.246V/μs** falling edge, and **0.174 V/μs** rising edge.

## Inverting Amplifier:



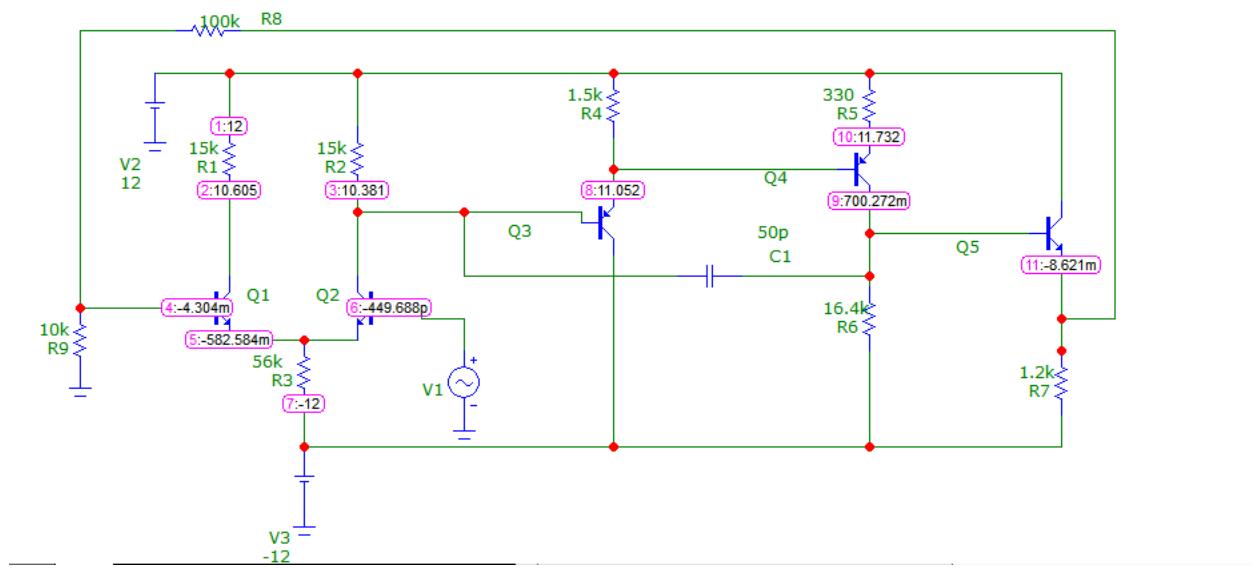
$$V_{in} = 420\text{mV}$$

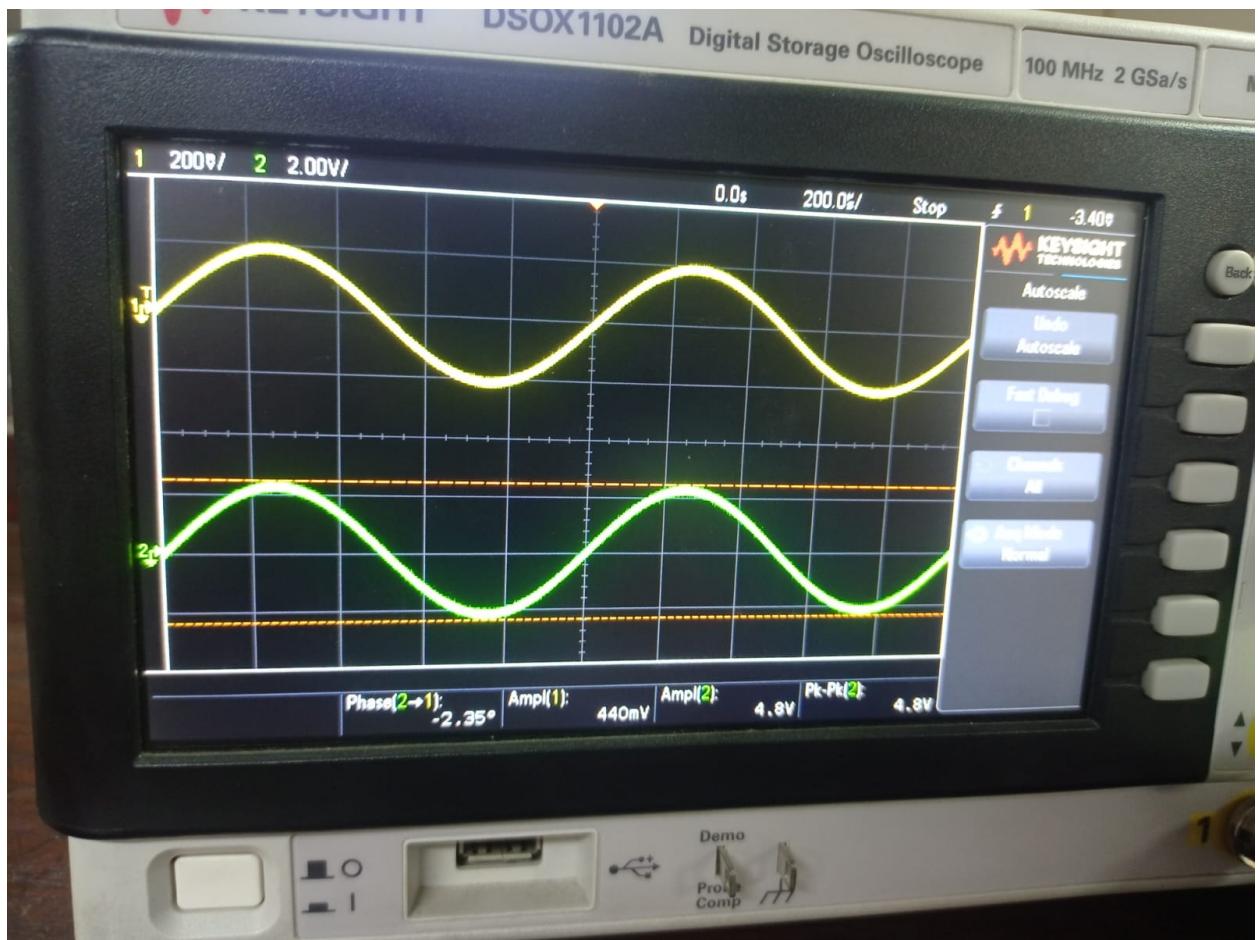
$$V_{out} = 3.66\text{V}$$

$$A_v = V_{in}/V_{out} = -8.71,$$

which is close to the theoretical value of -10. Note that the error of the resistors used are 10%, hence the error in gain is justified.

## Non-inverting Amplifier:





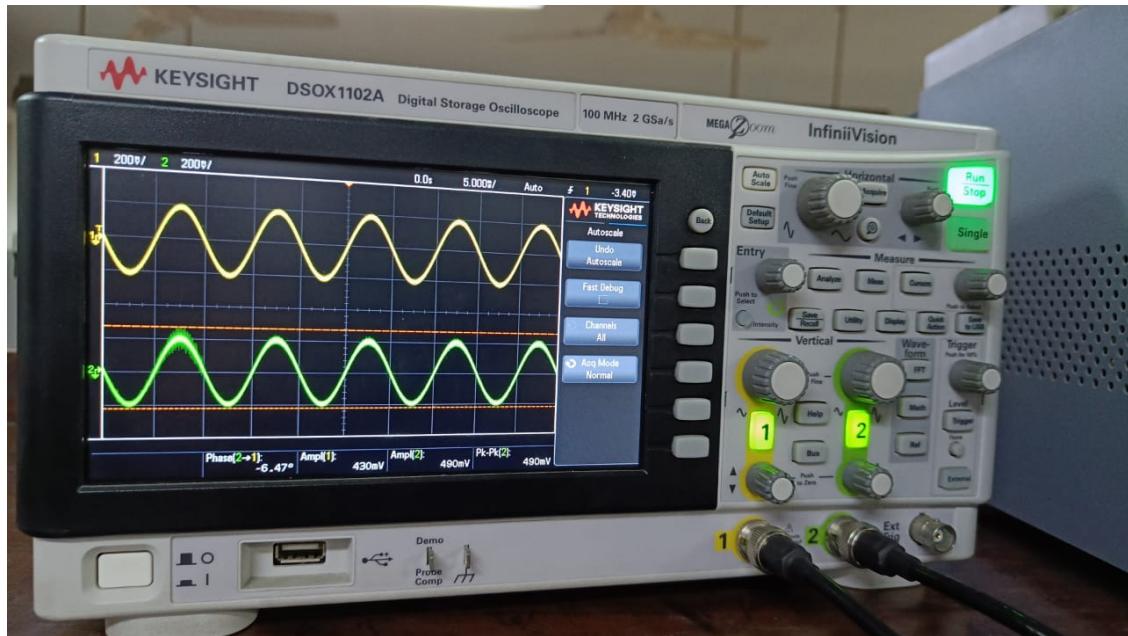
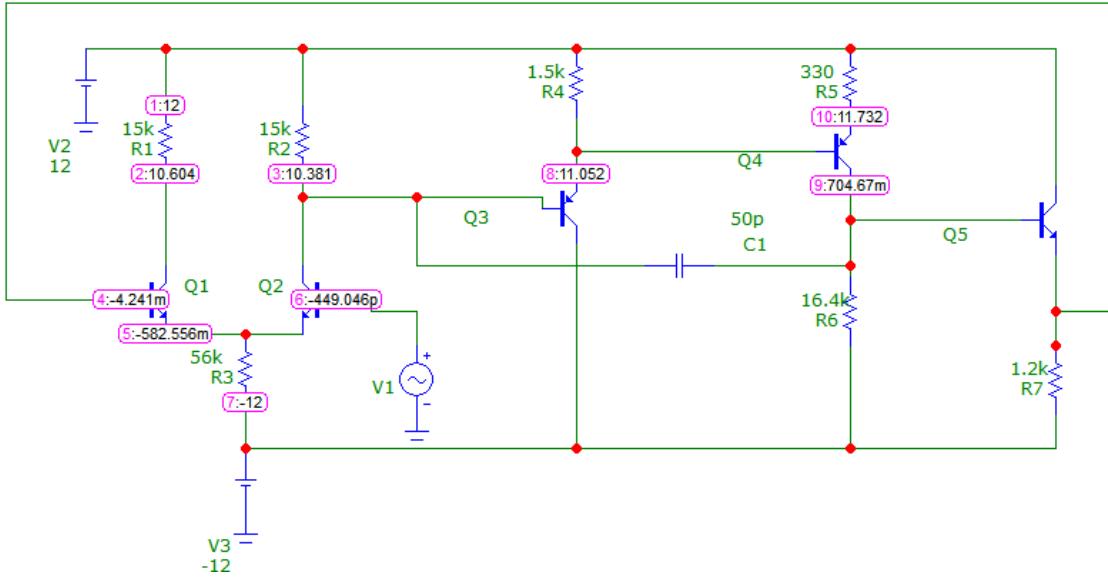
$$V_{in} = 440\text{mV}$$

$$V_{out} = 4.8\text{V}$$

$$Av = V_{in}/V_{out} = 10.9,$$

which is very close to the theoretical value of -11!

## Unity Gain Buffer/Voltage Follower:



$$V_{in} = 430\text{mV}$$

$$V_{out} = 490\text{mV}$$

$A_v = V_{in}/V_{out} = 1.14$ , which is quite close to the ideal value of 1!

## Possible Sources of Error in our experiments:

- Very high sensitivity of stage 3 resistor values.
  - Thermal variations of  $V_{fe}$  value of transistors.
  - Burning up of bread-board due to very high current.
  - Parallax error while measuring Cursors.
  - Imperfect Voltage Source(DC offset).
  - Wires not connected properly/error in bread-board
  - Capacitor value fluctuation/line capacitance.
  - Oscilloscope zero error
  - Non-linearity of resistors/non-ideal transistors.
  - Error in resistor/capacitor values.
  - Non-ideal voltage source.
  - Resistance in connecting wires.
  - Thermal variation of resistance/ $V_t$ .
  - Noise Fluctuations.
  - Harmonic Distortions
  - Not being able to get the exact resistance values due to the discretized nature of resistors.
  - Charging and discharging of capacitor.
-