ECE 506: Architecture of Parallel Computers

Report for Machine Problem 2

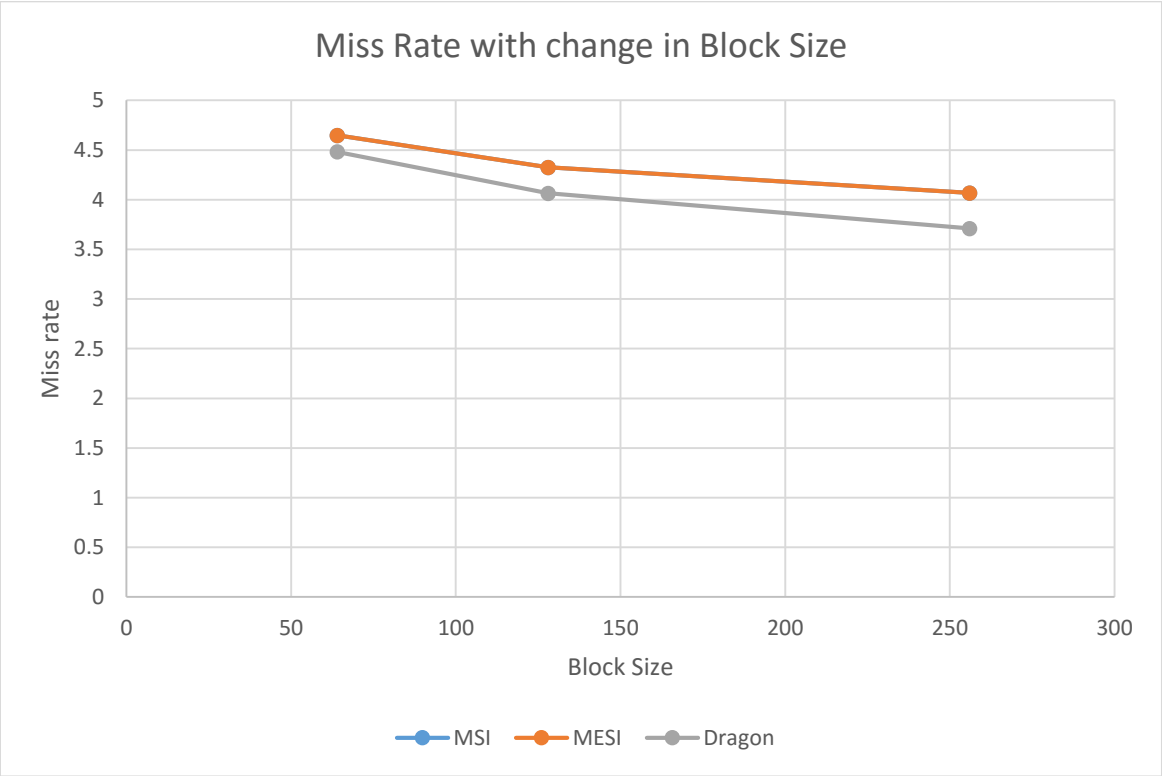
Name: Mohankumar Nekkarakalaya

ID: 200089159

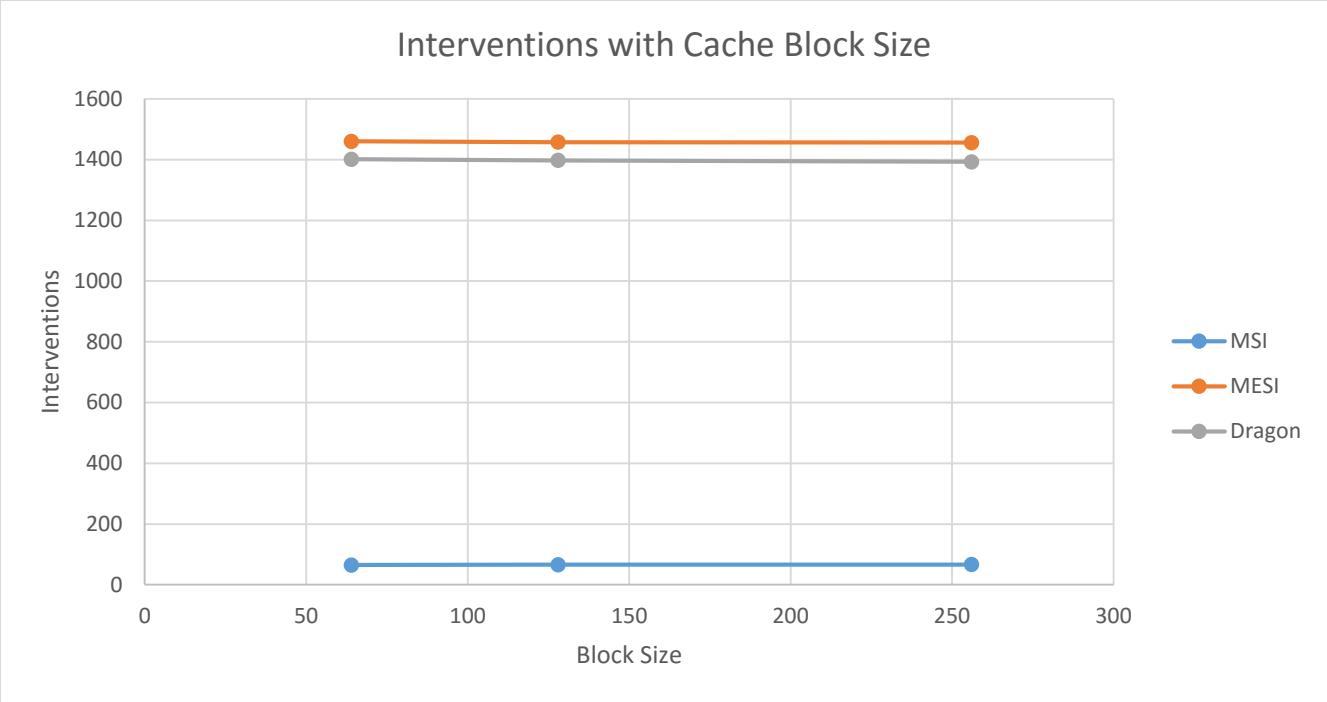
Changing Cache Block Size:

Protocol	**MSI**			**MESI**			**Dragon**		
Block Size	**64**	**128**	**256**	**64**	**128**	**256**	**64**	**128**	**256**
Reads	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25
Read Misses	5768.75	5362.75	5045.25	5768.75	5362.75	5045.25	5603.5	5078.75	4632.75
Writes	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75
Write Misses	40.25	40	40	40.25	40	40	1.75	1.5	1.5
Miss Rate	4.6475	4.325	4.0675	4.6475	4.325	4.0675	4.4825	4.065	3.71
Write Backs	167	269.25	355	167	269.25	355	111.25	149.75	194.75
C-C transfers	0	0	0	4399.75	4129.75	3930.75	0	0	0
Mem tran.	6649.5	6361.5	6152.5	1576.25	1542.25	1509.5	5716.5	5230	4829
Interventions	66.25	110	159	1457.5	1366.5	1299.25	1397.25	1266.5	1154.75
Invalidations	2019	2069	2136	2019	2069	2136	0	0	0
Flushes	104.75	148.5	197.5	104.75	148.5	197.5	6	6.75	8
BusRdXs	713.75	729.5	752.25	40.25	40	40	0	0	0

Observations:



Read Misses and Write Misses: are very less in Dragon due to no invalidation of cache blocks for cache coherency. Hence the blocks will be present longer in caches. Also as block size increases the spatial locality increases leading to lesser misses.



Interventions: This is very less in MSI as M to S is the only intervention case whereas in MESI it can have M to S, E to S as well.

Cache to Cache transfer: Decreases as block size increases due to lesser compulsory misses. There will be higher spatial locality.

Invalidations: Increases as the Block Size increases due to cache pollution.

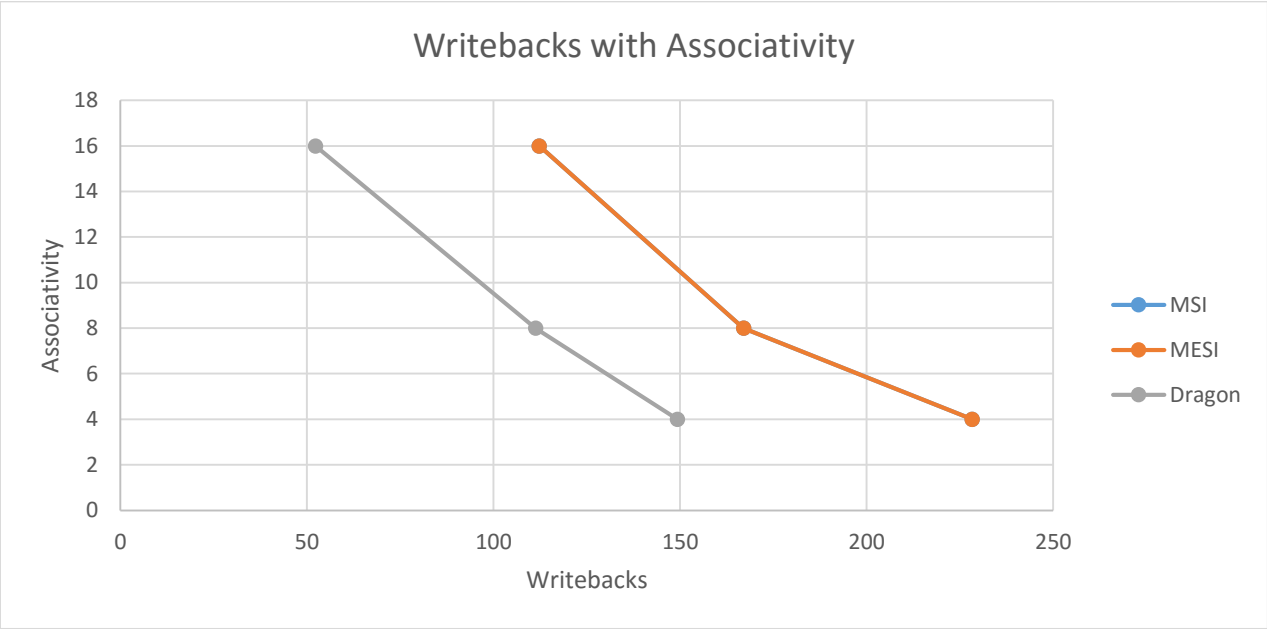
Flushes: Flushes are significantly lesser in Dragon due to dirty sharing.

BusRdX: In MESI the number of BusRdX is significantly lesser than that of MSI. In MESI Bus Rdx is generated only in one case i.e. from I to M state. In S to M it generated the BusUpgr signal. Whereas in MSI it is generated for I to M, S to I states.

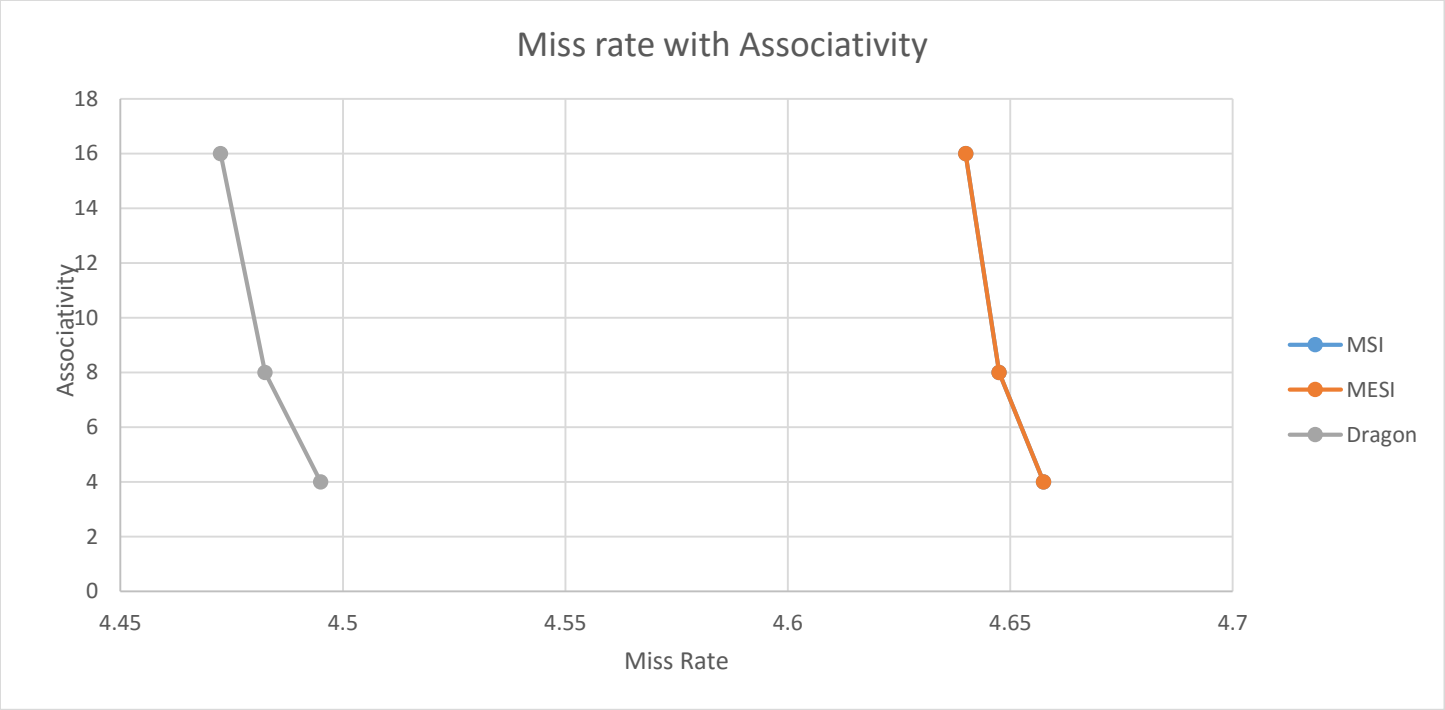
Changing Cache Associativity:

Protocol	MSI			MESI			Dragon		
Associativity	**4**	**8**	**16**	**4**	**8**	**16**	**4**	**8**	**16**
Reads	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25
Read Misses	5782.5	5768.75	5758.5	5782.5	5768.75	5758.5	5618.25	5603.5	5585.25
Writes	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75
Write Misses	40.25	40.25	40.25	40.25	40.25	40.25	1.75	1.75	1.75
Miss Rate	4.6575	4.6475	4.64	4.6575	4.6475	4.64	4.495	4.4825	4.4725
Write Backs	228.25	167	112.25	228.25	167	112.25	149.25	111.25	52.25
C-C transfers	0	0	0	4409.5	4399.75	4391.5	0	0	0
Mem tran.	6724.5	6649.5	6584.5	1641.5	1576.25	1519.5	5769.25	5716.5	5639.25
Interventions	65	66.25	66.5	1460.25	1457.5	1455.75	1401	1397.25	1392.75
Invalidations	2019	2019	2019	2019	2019	2019	0	0	0
Flushes	103.5	104.75	105	103.5	104.75	105	6	6	6
BusRdXs	713.75	713.75	713.75	40.25	40.25	40.25	0	0	0

Observations:



Write Backs: As Associativity increases the conflict misses decrease leading to lesser write backs.



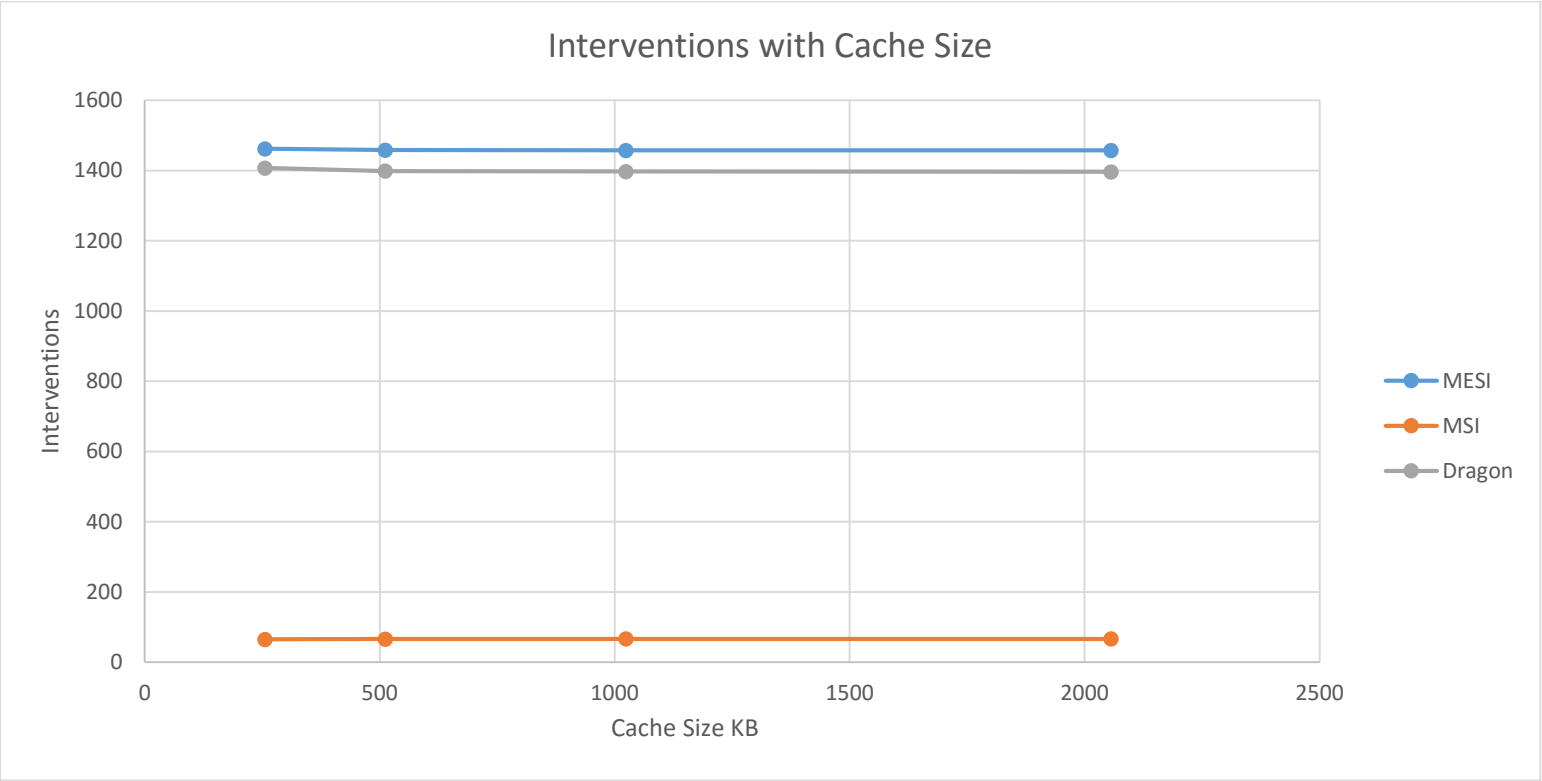
Miss rate: decreases as Associativity increases because of lesser conflict misses.

Invalidations: Does not depend on Associativity because Associativity doesn't influence bus based invalidations.

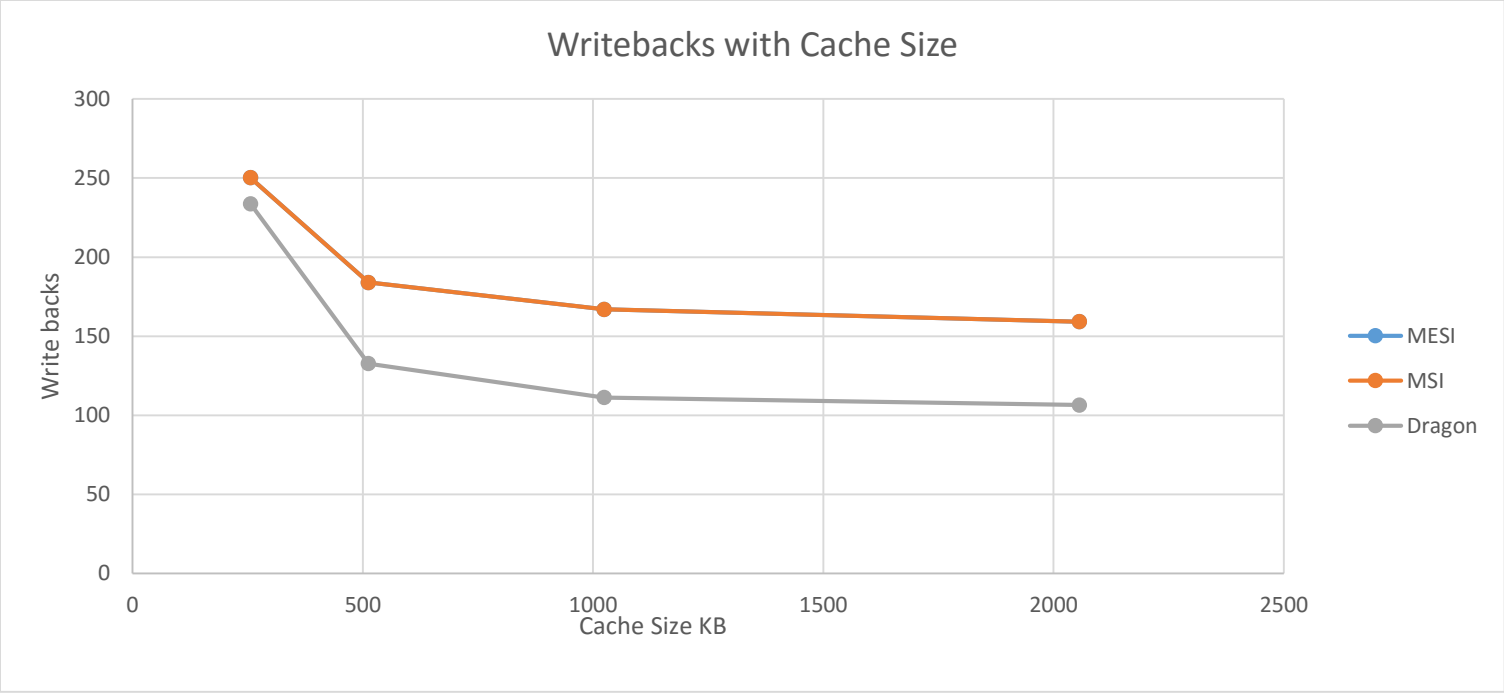
Changing Cache Size:

Protocol	MSI				MESI				Dragon			
Cache Size	**256KB**	**512KB**	**1MB**	**2MB**	**256KB**	**512KB**	**1MB**	**2MB**	**256KB**	**512KB**	**1MB**	**2MB**
Reads	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25	112964.25
Read Misses	5791	5775.25	5768.75	5767.25	5791	5775.25	5768.75	5767.25	5644.25	5609.5	5603.5	5600.75
Writes	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75	12035.75
Write Misses	40.25	40.25	40.25	40.25	40.25	40.25	40.25	40.25	1.75	1.75	1.75	1.75
Miss Rate	4.6675	4.6525	4.6475	4.6475	4.6675	4.6525	4.6475	4.6475	4.515	4.49	4.4825	4.4825
Write Backs	250.25	184	167	159.25	250.25	184	167	159.25	233.75	132.75	111.25	106.5
C-C transfers	0	0	0	0	4415.75	4404.75	4399.75	4398.25	0	0	0	0
Mem tran.	6755	6673	6649.5	6640.25	1665.75	1594.75	1576.25	1568.5	5879.75	5744	5716.5	5709
Interventions	64.75	65.75	66.25	66.25	1462	1458.5	1457.5	1457.5	1407.25	1398.75	1397.25	1396.5
Invalidations	2019	2019	2019	2019	2019	2019	2019	2019	0	0	0	0
Flushes	103.25	104.25	104.75	104.75	103.25	104.25	104.75	104.75	6.75	6	6	6
BusRdXs	713.75	713.75	713.75	713.75	40.25	40.25	40.25	40.25	0	0	0	0

Observations:



Interventions are independent of Cache Size as the Movement of block to shared state will be independent of natural misses.



Write Backs: This decreases as Cache size increases due to lesser Natural Misses.

Mem Transactions: This decreases as Cache size increases due to lesser evictions to main memory.