MOHANA RAO BERI

Patancheruvu, Hyderabad, India
9885082111 mohanaraoberi8@gmail.com

Professional Summary

Lead PCB Design Engineer with 14+ years of experience delivering **100+ multi-layer boards (up to 18 layers)** across **Intel, IoT, RF, automotive, and telecom platforms**. **IPC CID+ certified**, expert in **Cadence Allegro**, **Altium Designer**, and **OrCAD Schematic Capture** with specialization in **DDR5/LPDDR5/DDR4, PCIe Gen5/Gen4, USB 3.0, HDMI, Ethernet, CSI, and DDI**. Proven record of **first-pass success**, **EMI/EMC compliance**, and robust **post-silicon validation platforms**. Skilled in **high-speed designs** including add-on cards based on **TCP, USB3, and other interfaces** with validated performance up to **16 Gbps**. Experienced in **DFM/DFT/DFX**, **stack-up optimization**, **SI/PI analysis**, and collaborated with **cross-functional teams** to deliver advanced PCB designs for **global product platforms**.

Work Experience

Mobiveil Technologies (A GlobalLogic Company) — Client: Intel Corporation **Jun 2024 – Present**
Lead PCB Design Engineer *Bangalore, Karnataka*

- Led **design of Intel motherboards and high-speed system boards** (up to **18 layers**) using **Cadence Allegro 24.1**.
- Executed routing for **PCIe Gen5/Gen4, DDR5/LPDDR5/DDR4, USB 3.0, HDMI, Ethernet, CSI, and DDI** with strict **impedance control** and **timing closure**.
- Designed **add-on validation cards** for **TCP/USB3 interfaces**, enabling robust **post-silicon verification and debug**.
- Collaborated with **cross-functional teams** on **bring-up, validation, and prototype testing**, ensuring smooth product ramp-up.
- Mentored **junior engineers** through **design reviews** and promoted best practices in **IPC standards** and **DFM methodologies**.

Silicon Labs (SILABS INDIA Pvt Ltd) **Nov 2012 – Nov 2023**
Senior Engineer *Hyderabad, Telangana*

- Designed and delivered **RF validation kits, MCU starter kits, FPGA platforms, and power supply boards**, all aligned with **IPC** and **DFX standards**.
- Managed the complete **PCB lifecycle** – schematic validation, placement, routing, and fabrication handoff – ensuring robust and manufacturable designs.
- Applied **impedance control** and **length-matching** for **DDR, Ethernet, USB, and ADC/DAC signals**, minimizing re-spins and improving performance.
- Executed **lab bring-up and debugging** using oscilloscopes, logic analyzers, and power supplies, validating functionality prior to production release.
- Coordinated with **global engineering teams** to align with customer requirements, accelerating delivery and improving collaboration.
- Introduced **checklist-driven reviews** to improve design quality, enforce best practices, and reduce engineering queries.

Synoro Technologies **Oct 2010 – Oct 2012**
System Layout Engineer *Hyderabad, Telangana*

- Independently executed **PCB designs** for **Power Supply**, **LED Lighting**, and **Microcontroller Boards**.
- Managed complete schematic-to-**Gerber handovers** with **first-pass accuracy**, reducing dependency on external reviews.

Projects

High-Speed Validation Board for Next-Gen Processors (Intel Client)

- Executed **high-speed routing** across critical interfaces including **DDR5/LPDDR5, PCIe Gen5/Gen4, USB 3.0, HDMI, Ethernet, CSI, and DDI**.
- Optimized **stack-up design**, applied strict **impedance control**, and enforced PCB **design rules** for high-speed performance.
- Collaborated with cross-functional teams for **post-silicon validation**, enabling robust platform bring-up and compliance.

Explorer Kit (SiWx917 SoC, 6-layer, IoT)

- Built compact **RF-enabled kit** for **2.4 GHz IoT prototyping**, supporting rapid concept validation.
- Achieved **zero engineering queries** by adhering to schematic and PCB guidelines, ensuring **first-pass success**.
- Accelerated **customer prototyping cycles**, reducing design-to-deployment timelines.

FPGA XCUV 13P AFE Board (High-Speed, Altium Designer)

- Engineered PCB for **10-bit ADC/DAC high-speed signals**, applying **group-length matching** of data and CLK lines.
- Ensured **signal integrity**, minimized **skew**, and delivered stable synchronization in **FPGA systems**.
- Delivered a robust **high-speed board design** supporting demanding **mixed-signal validation**.

Technical Skills

PCB Design & Layout: Multi-Layer PCB Design (up to 16), High-Speed Interfaces, RF & Mixed-Signal, Power Supply Boards
Tools & Standards: Cadence Allegro 24.1, Altium 23/365, PADS VX2.8, Orcad 17.2, CAM350, IPC Standards, HyperLynx (Signal Integrity), Saturn Tool
Design Expertise: Schematic Capture, Librarian Creation, Stack-Up Calculations, Impedance Control, Differential Pair Routing, RF Shielding, Length Matching
Manufacturing & Validation: Gerber Generation, Panel/Stack-up Documentation, DFX Compliance, ECAD Documentation, Vendor Collaboration
Professional Skills: Problem-Solving, Attention to Detail, Team Collaboration, Customer Focus, Leadership, Time Management

Certifications

Certified Interconnect Designer – CID+ (Advanced) IPC — 2022
Certified Interconnect Designer – CID (Basic) IPC — 2022

Education

Ellenki College of Engineering, Hyderabad **Expected completion: 2026**
Bachelor of Technology (EEE)

Govt Polytechnic, Visakhapatnam, AP **2003**
AP Diploma in Electrical & Electronics Engineering