Folder: results
Date: March 31, 2014
Repository: git@git.rhrk.uni-kl.de:EIT-Wehn/finance.zynqpricer.hls.git
Revision: 3cc17b6fe870b602fdb9b1b9ff03d1ff1906d8e4
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Heston Multilevel Monte Carlo, 32bit floating point

Performance Comparison

DATE 2011 Demo	Performance [steps/s]	Energy Efficiency [Joule / step]	Process	Float Extensions	Details
FPGA, 1 instance (only IP-Core)	100.0E+6	35.0E-9	40 nm	-	Virtex 6, estimated

Source: de Schryver, Christian, et al. "A multi-level Monte Carlo FPGA accelerator for option pricing in the Heston model." Proceedings of the Conference on Design, Automation and Test in Europe. EDA Consortium, 2013.

Zync Demo	Performance [steps/s]	Energy Efficiency [Joule / step]	Process	Float Extensions	Details
Dell Laptop	137.9E+6	221.9E-9	22 nm	AVX	Intel Core i5-3320M @ 2.60 GHz, 2 cores
HyPER on Zynq	467.2E+6	6.1E-9	28 nm	-	zc702, XC7Z020-CLG484-1

Zynq 36.2 more power efficient than Intel CPU
Zynq 3.4 faster than CPU

Lines of Code Comparison

Implemetation	Heston Accelerator [lines of code]	Host Driver & Demo [lines of code]	Languages	
FPGA, Date 2013 (Pedro, Fischer)	*5280*	*7870*	AutoESL, VHDL, Java	*Demo work in progress*
ASIC (Nhan)	*9960*	-	VHDL, ROMCODE	*Only IP, no interfaces*
New Methodology: HLS + Zynq + Linux	650	1129	Vivado HLS & Zynq FPGA	
New Software C++			C++ Software	

7.4 times smaller code for the same functionality than FPGA implementation

FPGA Ressource Comparison

Target Frequency 100 MHz, Increment Generator + Path Generator + Barrier Feature

	LUTs	FFs	BRAMs	DSPs	Comments
Zynq Implementation	**6767**	**6938**	**7**	**44**	
Heston Kernel	6015	6023	3	43	
ICDF Gauss	451	592	2	1	Prec: 0.00019
Mersenne Twister	301	323	2	0	
DATE 2013	**11000**	**12630**	**68**	**69**	
Heston Kernel	10288	11949	64	68	*AXI design by Pedro (AutoESL, VHDL)*
ICDF Gauss	*300*	*450*	*1*	*1*	Prec: 0.00039, Ressources estimated
Mersenne Twister	412	231	3	0	

Source: de Schryver, Christian, et al. "A multi-level Monte Carlo FPGA accelerator for option pricing in the Heston model." Proceedings of the Conference on Design, Automation and Test in Europe. EDA Consortium, 2013.

Significantly (> 50%) better implemented than Pedro