

Folder: results
Date: September 06, 2013
Repository: git@git.rhrk.uni-kl.de:EIT-Wehn/finance.zynqpricer.hls.git
Revision: 980629241b7f4648c347902328718a244f7b511f
Author: Christian Brugger (brugger@eit.uni-kl.de)

Heston Single Level Monte Carlo, 32bit floating point

Performance Comparison

DATE 2011 Demo	Performance [steps/s]	Energy Efficiency [Joule / step]	Process	Float Extensions	Details
Laptop + FPGA (efficiency 48 %)	142.7E+6	245.5E-9	65 nm	(SSSE3)	Core 2 Duo + ML507
Server	62.1E+6	2997.0E-9	45 nm	(SSE4.2)	Intel Xeon W3550 @ 4x3.07 GHz

Source: de Schryver, Christian, et al. "An energy efficient FPGA accelerator for Monte Carlo option pricing with the Heston model." *Reconfigurable Computing and FPGAs (ReConFig), 2011 International Conference on. IEEE, 2011.*

Zync Demo	Performance [steps/s]	Energy Efficiency [Joule / step]	Process	Float Extensions	Details
Server	267.7E+6	694.8E-9	45 nm	SSE4.2	Intel Xeon W3550 @ 4x3.07 GHz
Dell Laptop	141.1E+6	216.9E-9	22 nm	AVX	Intel Core i5-3320M @ 2.60 GHz, 2 cores
Dell Desktop	214.9E+6	716.7E-9	45 nm	SSE4.2	Intel Core i7 860 @ 4x2.8 GHz
Zynq ARM only	10.8E+6	176.2E-9	28 nm	Neon	zc702, ARM Cortex-A9 @ 2 x 0.667 GHz
Zynq FPGA 6x (efficiency 99.9 %)	599.4E+6	4.6E-9	28 nm	-	zc702, XC7Z020-CLG484-1

ARM 23% more power efficient than Intel Laptop
Optimized C++ Implementation 4.3 times faster than DATE 2011 implementation (Vectorized (AVX), Cache Optimization, Ziggurat)
Zynq 4.2 times faster than DATE 2011 Demo
Zynq 53.2 more power efficient than DATE 2011 Demo
Zynq 47.0 more power efficient than Intel CPU

Lines of Code Comparison

Implemetation	Heston Accelerator [lines of code]	Host Driver & Demo [lines of code]	Languages
Heston SL, Date 2011 (Yvan, Daniel)	3705	1330	THDL, Visual Pipeline, VHDL, USB
Heston ML, Date 2013 (Pedro, Thomas)	5280	7870	AutoESL, VHDL <i>Demo work in progress</i>
New Methodology: HLS + Zynq + Linux	415	540	Vivado HLS & Zynq FPGA
New Software C++	210	150	C++ Software

9 times smaller code for the same functionality

FPGA Ressource Comparison

Target Frequency 100 MHz

	LUTs	FFs	BRAMs	DSPs	Comments
Zynq Implementation	5190	5358	5	36	
Heston Kernel	4457	4443	1	35	
ICDF Gauss	447	592	2	1	Prec: 0.00019
Box Muller	3611	3006	0	35	30 lines of code
Mersenne Twister	286	323	2	0	
DATE 2011	5681	7300	5	43	
Heston Kernel	4969	6619	1	42	
ICDF Gauss	300	450	1	1	Prec: 0.00039, Ressources estimated
Mersenne Twister	412	231	3	0	

Comparable ressources