CMPE 460 Laboratory Exercise 8

Heartrate Monitor

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By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: _____

Abstract

yeehaw

Design Methodology

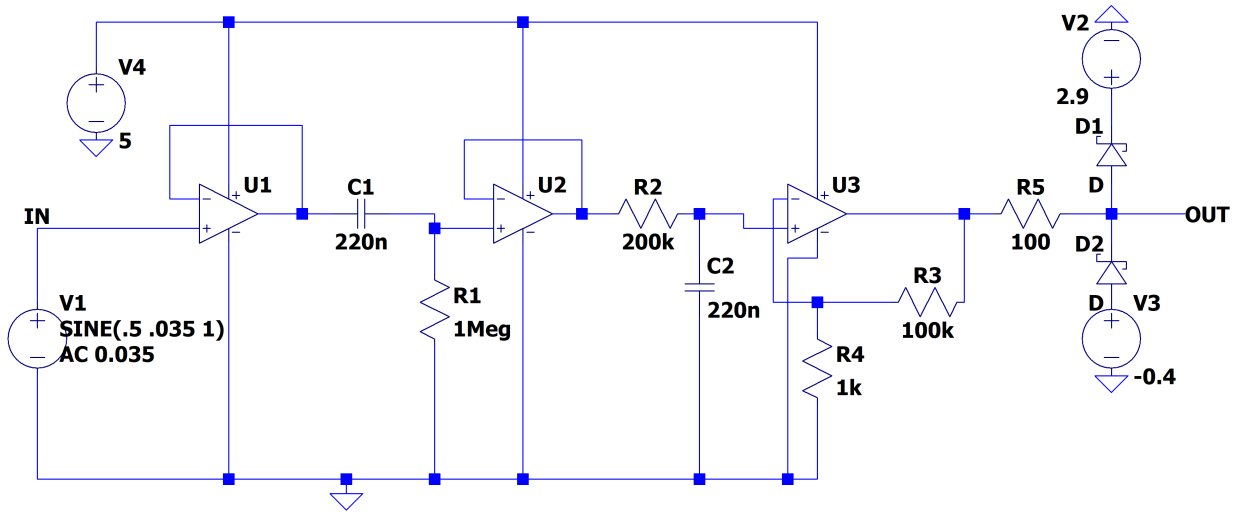

Figure 1: LTspice Schematic

Results and Analysis

The high-pass filter of the circuit was tested at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 2 shows the resulting Bode plot.

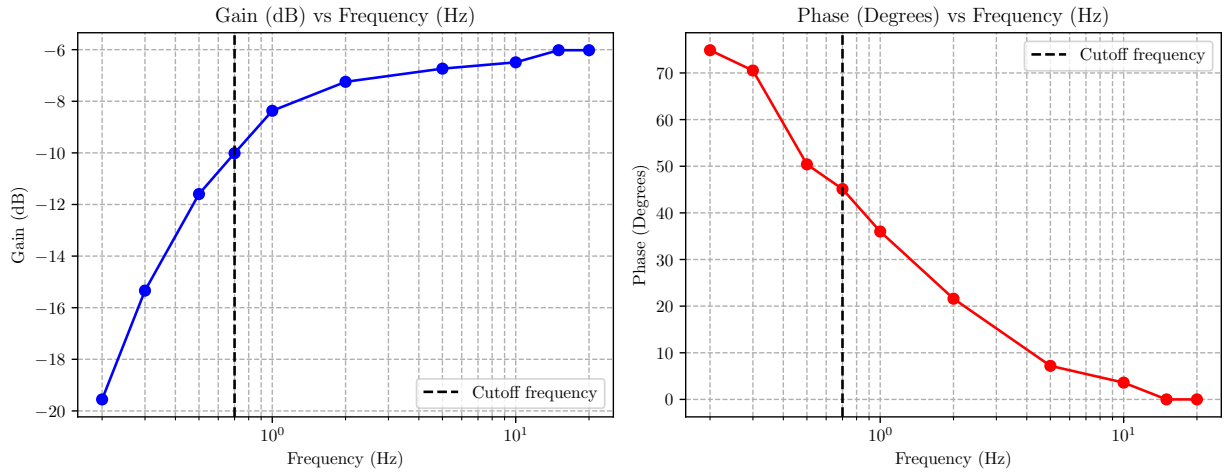

Figure 2: High-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequency of 0.7 Hz is approximately correct. The cutoff frequency on the plot is slightly higher than the calculated value, using -9 dB as the cutoff point (3 dB less than the maximum gain). The plot shows that the phase shift of the circuit is approximately 45 degrees at the cutoff frequency, decreasing to 0 degrees at higher frequencies. The phase shift has the general behavior of increasing from 75 to 0 degrees as the frequency increases.
The low-pass filter of the circuit was tested at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 3 shows the resulting Bode plot.

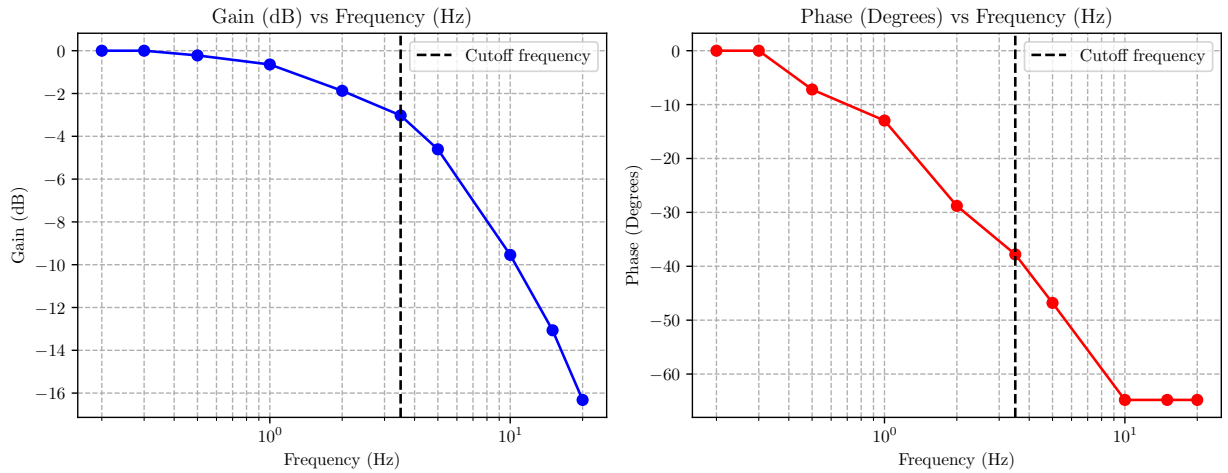

Figure 3: Low-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequency of 3.5 Hz is approximately correct. The cutoff frequency on the plot falls at the calculated value, using -3 dB as the cutoff point (3 dB less than the maximum gain). The phase shift of the circuit is approximately -38 degrees at the cutoff frequency, decreasing to -65 degrees at higher frequencies, which is the expected behavior. The phase shift has the general behavior of decreasing from 0 to -65 degrees as the frequency increases.

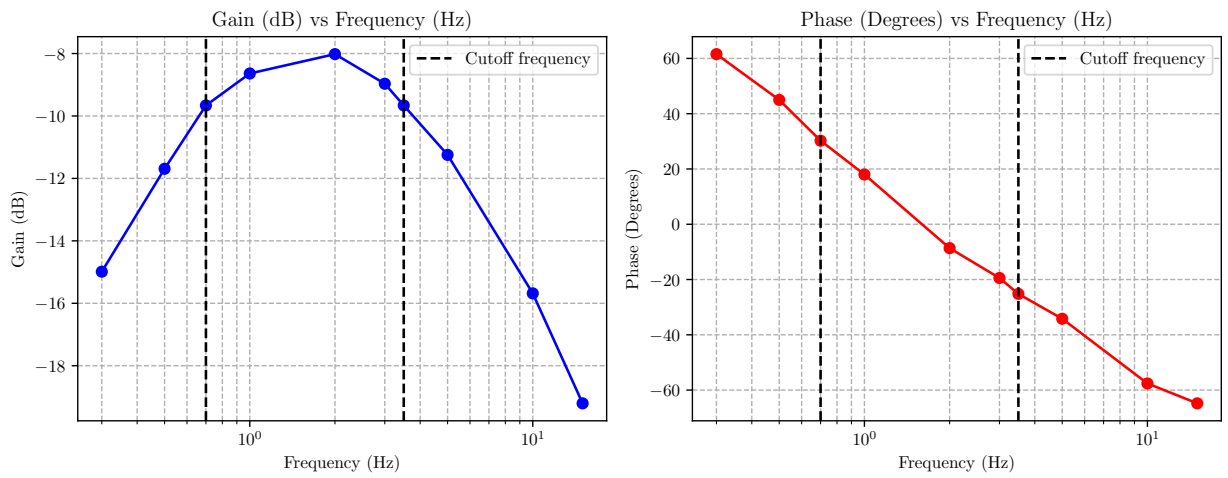

Figure 4: Band-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequencies of 0.7 Hz and 3.5 Hz are approximately correct. Using -11 dB as the cutoff point (3 dB less than the maximum gain), the lower cutoff frequency is slightly lower than the calculated value and the upper cutoff frequency is slightly higher than the calculated value. The phase shift of the circuit is approximately 30 degrees at the lower cutoff frequency, decreasing to -25 degrees at the upper cutoff frequency, which is the expected behavior. The phase shift has the general behavior of decreasing from 60 to -65 degrees as the frequency increases.

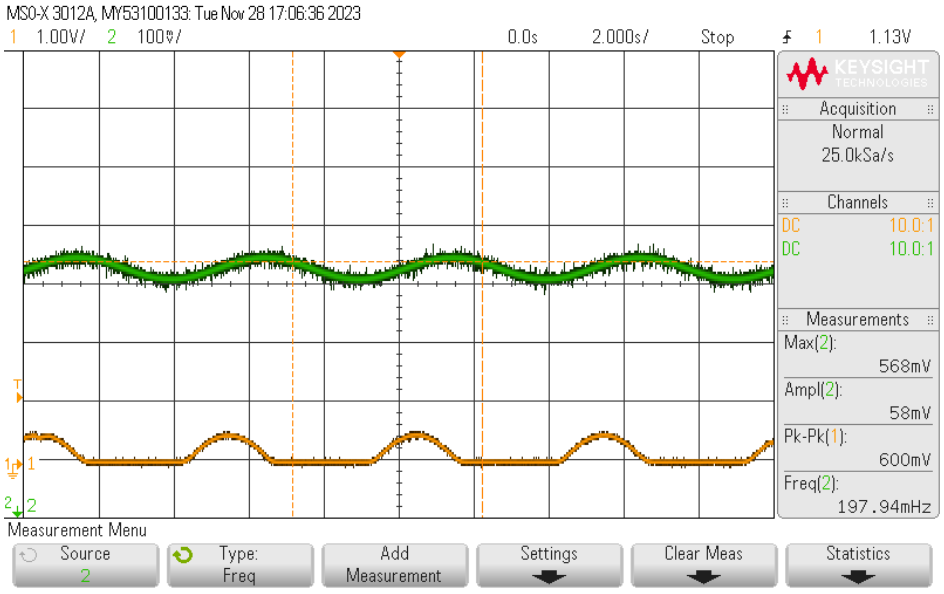

Figure 5: Oscilloscope SCHTUFF

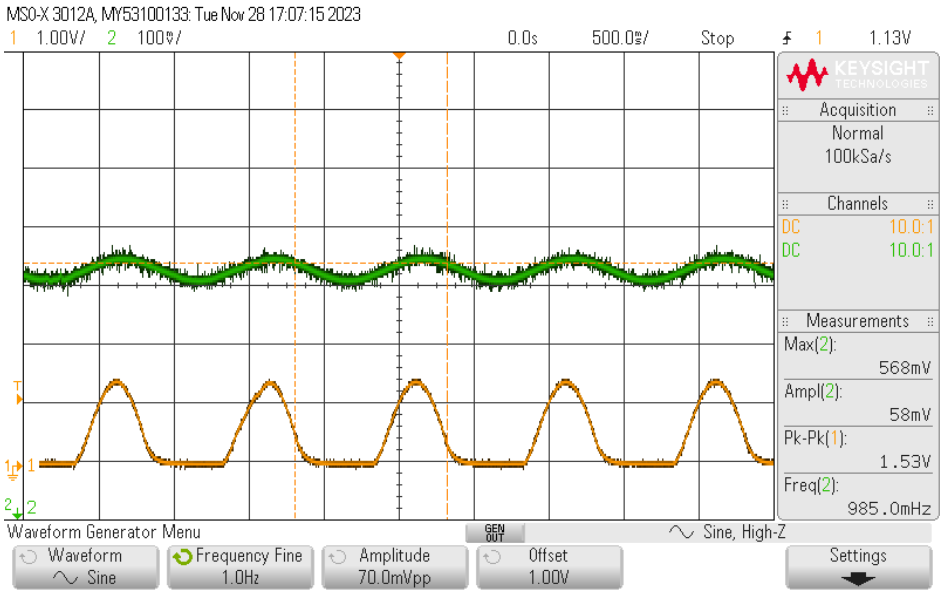

Figure 6: Oscilloscope SCHTUFF

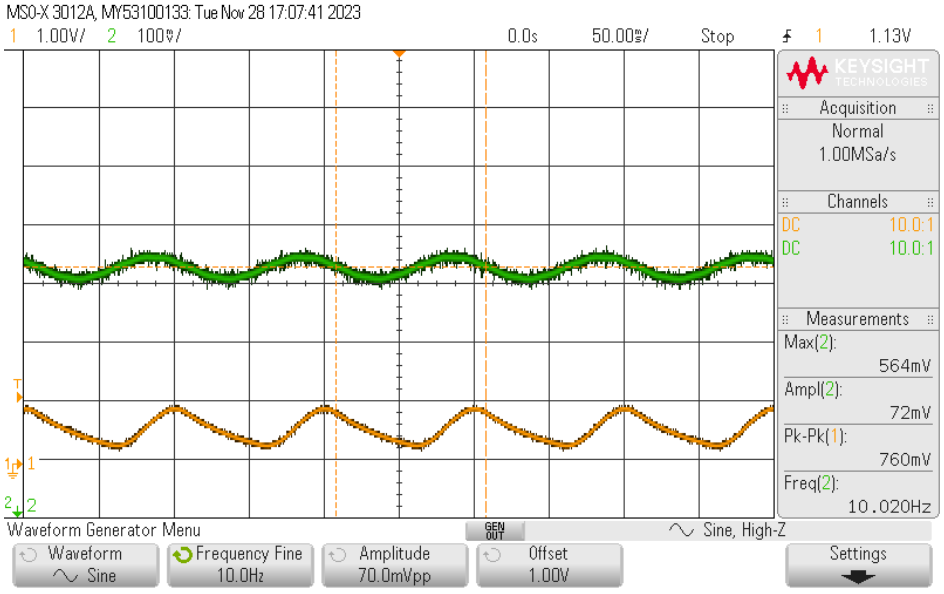

Figure 7: Oscilloscope SCHTUFF

Questions

1. *What is the ERC and DRC for?*
ERC stands for Electrical Rule Check and DRC stands for Design Rule Check. The ERC checks for electrical errors in the schematic, such as unconnected pins. The DRC checks for design errors in the schematic, such as incorrect pin types.

2. *Did your circuit cutoff frequencies match your expected/calculated values? Explain*

3. *Did the gain of the circuit match the expected/calculated values? Explain*

Conclusion