CMPE 460 Laboratory Exercise 8

Heartrate Monitor

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Abstract

This laboratory exercise involved the design and construction of a heartbeat detection circuit. For the detection of a heartbeat, an OPB745 reflective optical sensor can be used. This device will emit light through a finger and ideally measure reflected light which varies with the pulse within the arteries of a finger. The signal output is then filtered with a low pass filter and a high pass filter to exclude frequencies outside an expected range of heart rates. The resulting signal is then amplified by an op amp to get a more usable signal. This circuit was designed, simulated using LTspice, constructed on a breadboard, and measured. C code was written with an MSP432 microcontroller which would measure pulse based on the output of the constructed circuit. This exercise also includes the design of a PCB with the same heartbeat detection circuit. This exercise was partially successful since the circuit constructed behaved as expected with an oscilloscope-generated sinusoidal signal. The circuit output was accurately used by the MSP432 to detect frequency in beats per minute. The circuit constructed was unable to detect a heartbeat using the OPB745 and the PCB was not designed.

Design Methodology

A PPG is an instrument used to measure changes in blood volume under the skin. One use of this is to measure heart rate. A circuit was designed with the intent to measure the pulse within a finger using an OPB745 reflective optical sensor.
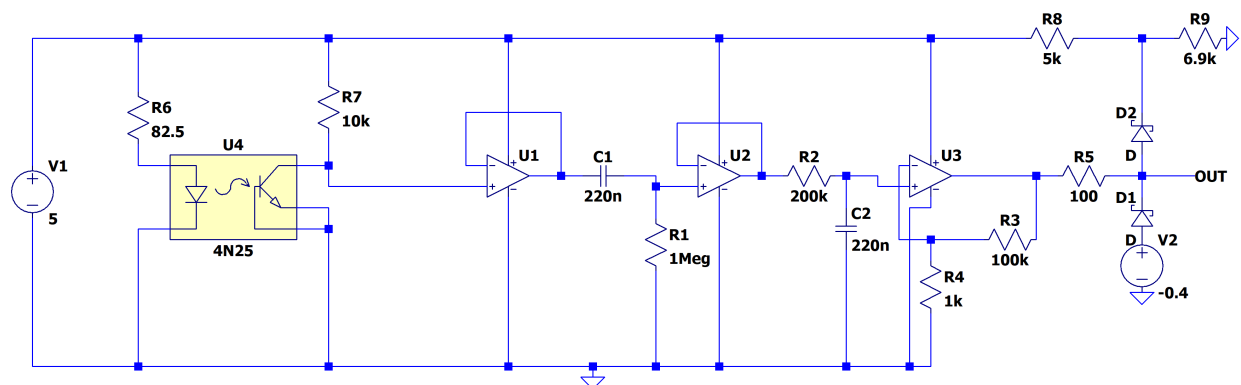

Figure 1: LTspice Schematic

Figure 1 shows the complete schematic design. The 4N25 represents the OPB745. A 5V source is used to provide power to the OPB745, op amps, and a Schottky diode. Voltage division occurs between the 10kΩ resistor and the photodetector. This signal then goes to a voltage follower op amp which isolates the signal from the next stage. The signal is then filtered by a passive high pass RC filter. This filter has a cut off frequency of 0.7Hz which is 42bpm. This ensures that a low heart rate will be detected without anything significantly lower. The equation for the high pass filter design is shown below.

$$R = \frac{1}{2 * \pi * C * f_c} = \frac{1}{2 * \pi * 220nF * 0.7Hz} = 1M\Omega \tag{1}$$

With a cut off frequency of 0.7Hz and a capacitor value of 220nF, Equation 1 shows that the appropriate resistor value is 1MΩ. Equation 2 shows the magnitude of the transfer function for the high pass filter.

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{R}{\sqrt{X_C^2 + R^2}} = \frac{R}{\sqrt{\frac{1}{\omega C}^2 + R^2}} \tag{2}$$

From this equation, it is evident that as frequency increases, the magnitude increases. This is characteristic of a high pass filter. The phase response is shown in Equation 3.

$$\angle\frac{V_{out}}{V_{in}} = -tan^{-1}(\frac{\omega RC}{1}) \tag{3}$$

This equation describes the delay that a signal will experience from the high pass filter. The signal from the high pass filter then goes through another voltage follower for isolation between stages. Next, the signal is filtered by a passive low pass RC filter. This filter has a cut off frequency of 3.5Hz which is 210bpm. The equation for the low pass filter design is shown below.

$$R = \frac{1}{2 * \pi * C * f_c} = \frac{1}{2 * \pi * 220nF * 3.5Hz} = 200k\Omega \tag{4}$$

With a cut off frequency of 3.5Hz and a capacitor value of 220nF, Equation 4 shows that the appropriate resistor value is 200kΩ. The transfer function's magnitude is shown in Equation 5.

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{X_C}{\sqrt{X_C^2 + R^2}} = \frac{\frac{1}{\omega C}}{\sqrt{\frac{1}{\omega C}^2 + R^2}} \tag{5}$$

This equation describes the magnitude response in relation to frequency for a low pass filter. According to this transfer function, as frequency increases, the magnitude decreases. The phase of the transfer function is shown in Equation 6.

$$\angle\frac{V_{out}}{V_{in}} = -tan^{-1}(\frac{1}{\omega RC}) \tag{6}$$

This equation describes the delay that a signal will experience from the low pass filter. After passing through the low pass filter, the signal is amplified by an op amp. To make the signal scale up to about 3.3V, a gain of 101 was implemented. The calculation for resistor values is shown in Figure 7.

$$Gain = 101 = 1 + \frac{R_a}{R_b} = 1 + \frac{100,000\Omega}{1,000\Omega} \tag{7}$$

After amplification and filtering, the signal goes through one last stage consisting of surge protection. A 100Ω resistor was added and two Schottky diodes were placed around the

output. The upper diode is attached to 2.9V from voltage division and the lower diode is attached to -0.4V. This ensures that voltages above 3.3V and below 0V will be pulled away from the output.

Results and Analysis

The circuit was simulated using LTspice, constructed on a breadboard, and then tested and compared to the simulation results. First, the high pass filter of the circuit was simulated using the schematic shown in Figure 2.
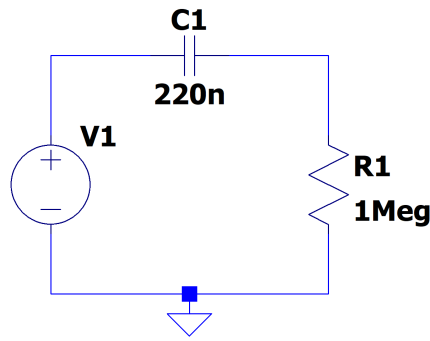

Figure 2: High-Pass Filter Schematic

The figure shows that the filter was simulated using a function generator with a 220 nF capacitor and a 1 MΩ resistor. The complete circuit was then simulated using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz.

Figure 3 shows the simulation of the high-pass filter, performed using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz.
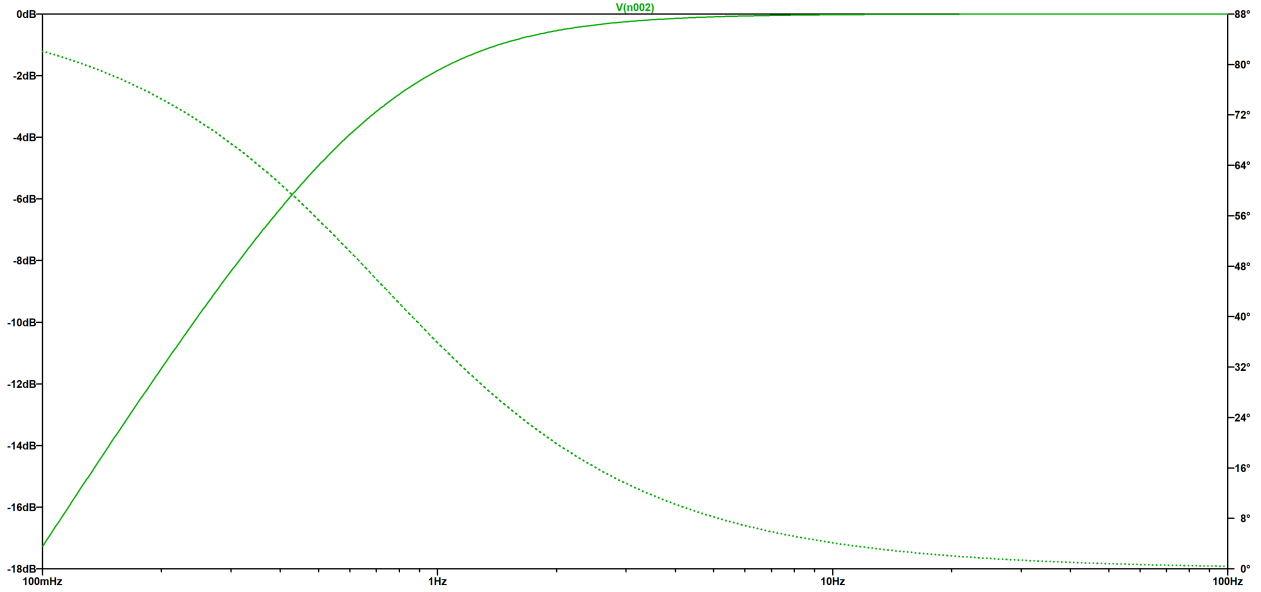
Figure 3: High-Pass Filter Bode Simulation

The figure shows that the gain of the circuit is approximately 0 dB in the pass band, decreasing as the frequency decreases. The figure also shows that the phase shift of the circuit decreases as the frequency increases. The cutoff frequency of the circuit is approximately 0.7 Hz, which is equal to the calculated value.

The high-pass filter of the circuit was constructed on a breadboard and tested using an oscilloscope and a function generator at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 4 shows the resulting Bode plot.
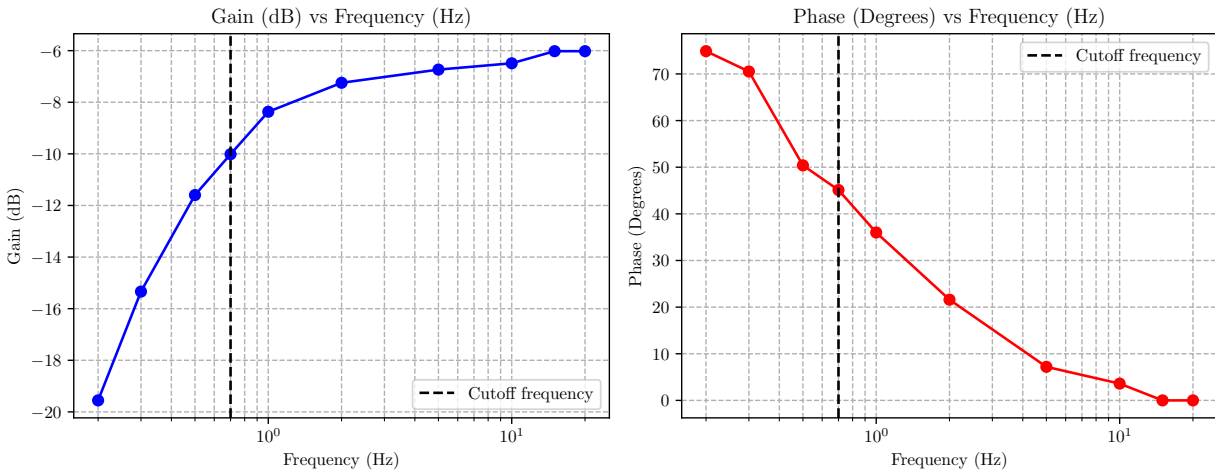

Figure 4: High-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequency of 0.7 Hz is approximately correct. The cutoff frequency on the plot is slightly higher than the calculated value, using -9 dB as

the cutoff point (3 dB less than the maximum gain). The plot shows that the phase shift of the circuit is approximately 45 degrees at the cutoff frequency, decreasing to 0 degrees at higher frequencies. The phase shift has the general behavior of decreasing from 75 to 0 degrees as the frequency increases.

The results show that the simulation and constructed circuit are similar, with the constructed circuit having a slightly higher cutoff frequency and a slightly lower phase shift at the cutoff frequency. The constructed circuit also has a lower maximum gain (-6 dB) than the simulated circuit (0 dB), which is approximately half of the simulated value. This decrease in gain propagates through the rest of the circuit.

The low pass filter of the circuit was simulated using the schematic shown in Figure 5.
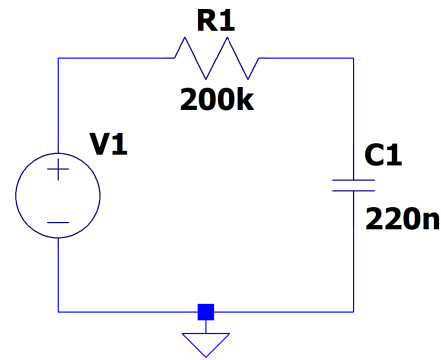

Figure 5: Low-Pass Filter Schematic

The figure shows that the filter was simulated using a function generator with a 220 nF capacitor and a 200 kΩ resistor. The complete circuit was then simulated using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz.

Figure 6 shows the simulation of the low-pass filter of the circuit, performed using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz.
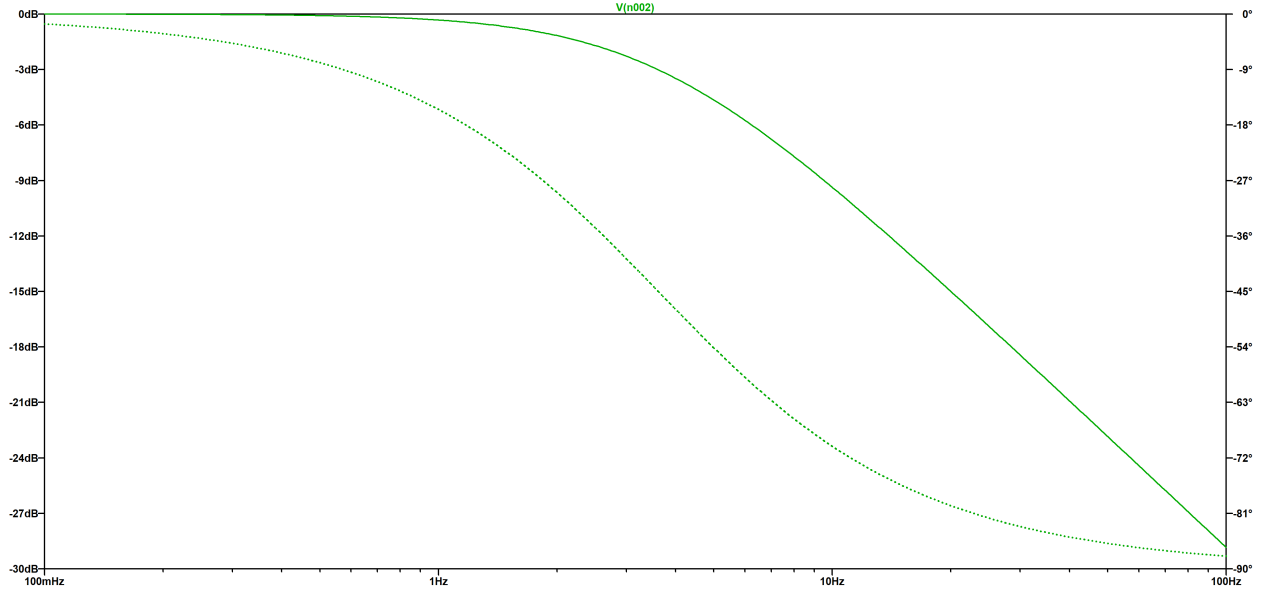
Figure 6: Low-Pass Filter Bode Simulation

The figure shows that the gain of the circuit is approximately 0 in the pass band, decreasing as the frequency increases. The figure also shows that the phase shift of the circuit is approximately 0 degrees in the pass band, decreasing to -90 degrees as the frequency increases. The cutoff frequency of the circuit is approximately 3.5 Hz, which is equal to the calculated value.

The low-pass filter of the circuit was constructed on a breadboard and tested using an oscilloscope and a function generator at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 7 shows the resulting Bode plot.
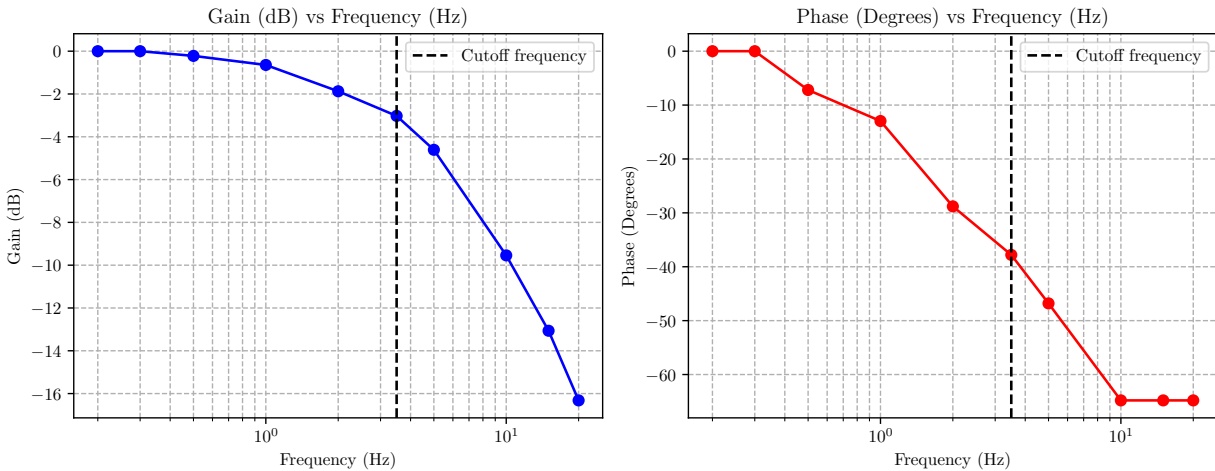

Figure 7: Low-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequency of 3.5 Hz is approximately correct. The cutoff frequency on the plot falls at the calculated value, using -3 dB as the cutoff point

(3 dB less than the maximum gain). The phase shift of the circuit is approximately -38 degrees at the cutoff frequency, decreasing to -65 degrees at higher frequencies. The phase shift has the general behavior of decreasing from 0 to -65 degrees as the frequency increases.

The results show that the simulation and constructed circuit are very similar, with no significant differences between the two.

The band pass filter of the circuit was simulated by combining the high-pass and low-pass filters. Figure 8 shows the simulation of the band-pass filter of the circuit, performed using an AC sweep with a logarithmic scale from 100 mHz to 20 Hz.
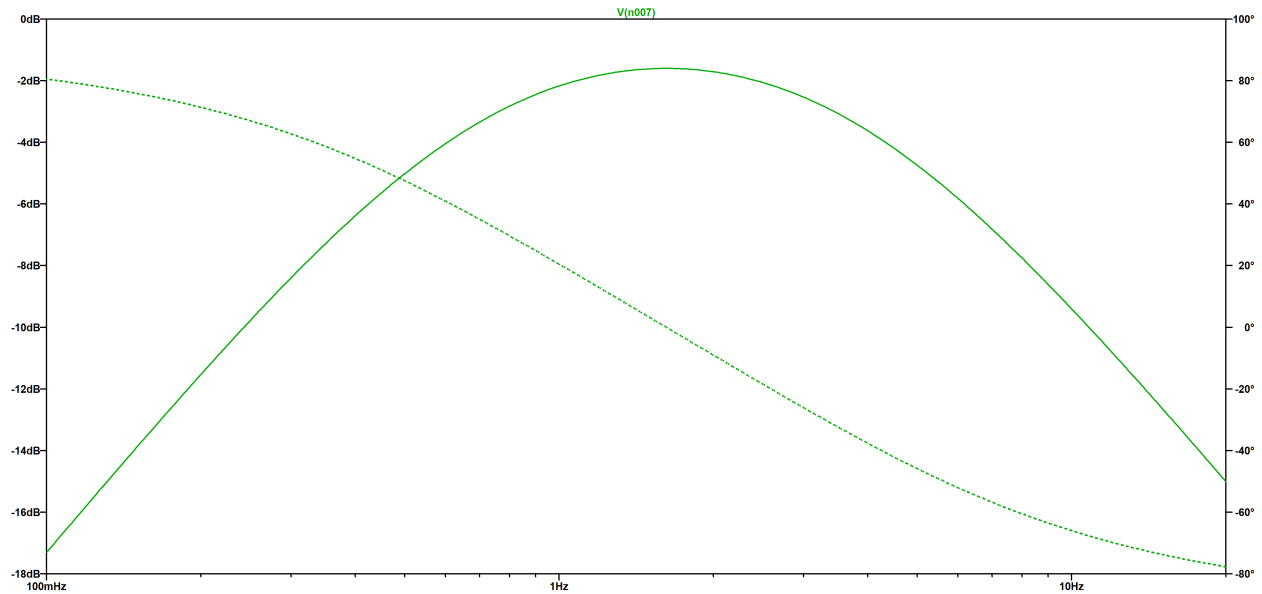

Figure 8: Band-Pass Filter Bode Simulation

The figure shows that the gain of the circuit is approximately -3 and -1 in the pass band, with cutoff frequencies of 0.7 Hz and 3.5 Hz, which matches the calculated values. The figure also shows that the phase shift of the circuit is approximately 80 degrees at low frequencies (around 100 mHz) and -80 degrees at high frequencies (around 20 Hz), which is the expected behavior. The phase shift has the general behavior of decreasing from 80 to -80 degrees as the frequency increases.

The band-pass filter of the circuit was constructed on a breadboard and tested using an oscilloscope and a function generator at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 9 shows the resulting Bode plot.
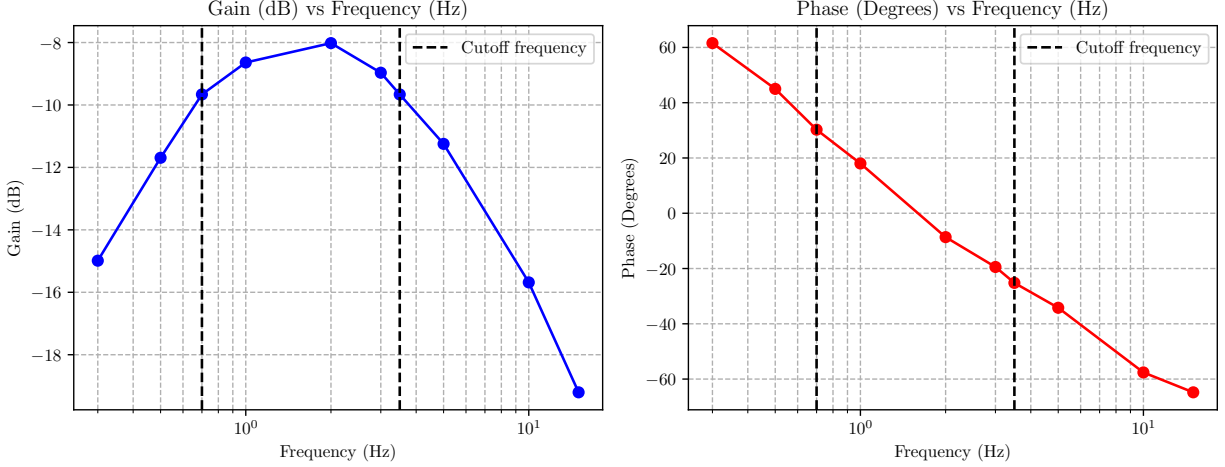
Figure 9: Band-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequencies of 0.7 Hz and 3.5 Hz are approximately correct. Using -11 dB as the cutoff point (3 dB less than the maximum gain), the lower cutoff frequency is slightly lower than the calculated value and the upper cutoff frequency is slightly higher than the calculated value. The phase shift of the circuit is approximately 30 degrees at the lower cutoff frequency, decreasing to -25 degrees at the upper cutoff frequency, which is the expected behavior. The phase shift has the general behavior of decreasing from 60 to -65 degrees as the frequency increases.

The results show that the simulation and constructed circuit are similar, with the constructed circuit having a slightly lower cutoff frequency and a slightly higher upper cutoff frequency. The constructed circuit also has a lower maximum gain (-8 dB) than the simulated circuit (-2 dB), which is attributed to the decreased gain of the high-pass filter of the circuit. The phase shift of the constructed circuit is also slightly lower than the simulated circuit at the lower cutoff frequency.

The PPG circuit was then constructed and simulated in LTspice. Figure 10 shows the schematic of the complete circuit constructed in LTspice.
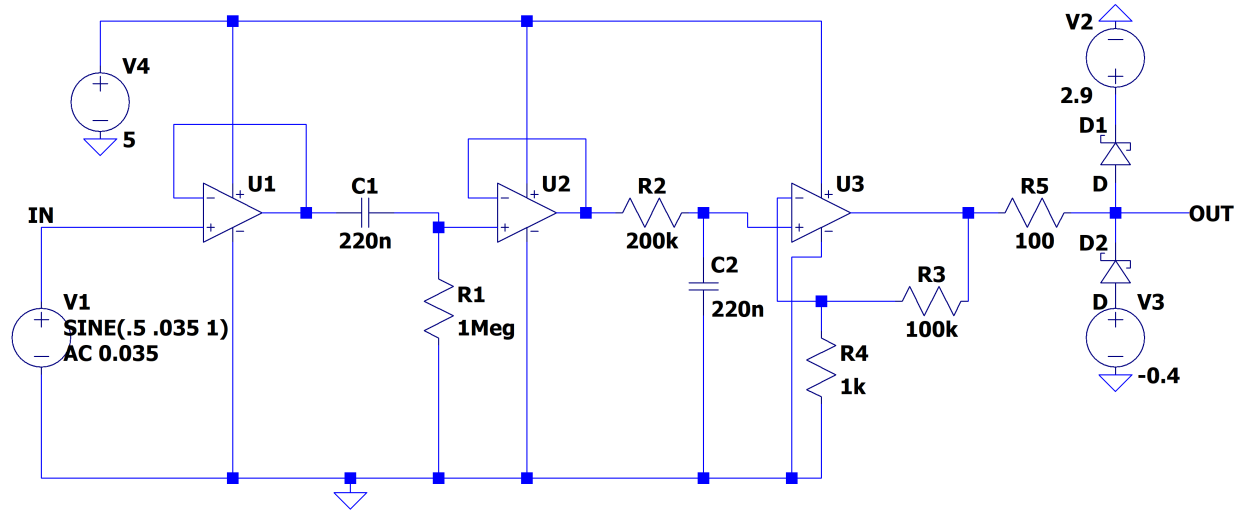
Figure 10: LTspice Schematic

The figure shows that the OPB745 is simulated using a function generator with a 35 mV amplitude and a frequency of 1 Hz, and the circuit is constructed using the appropriate components. The complete circuit was then simulated using an AC sweep with a logarithmic scale from 100 mHz to 10 Hz. Figure 11 shows the simulation of the complete circuit.
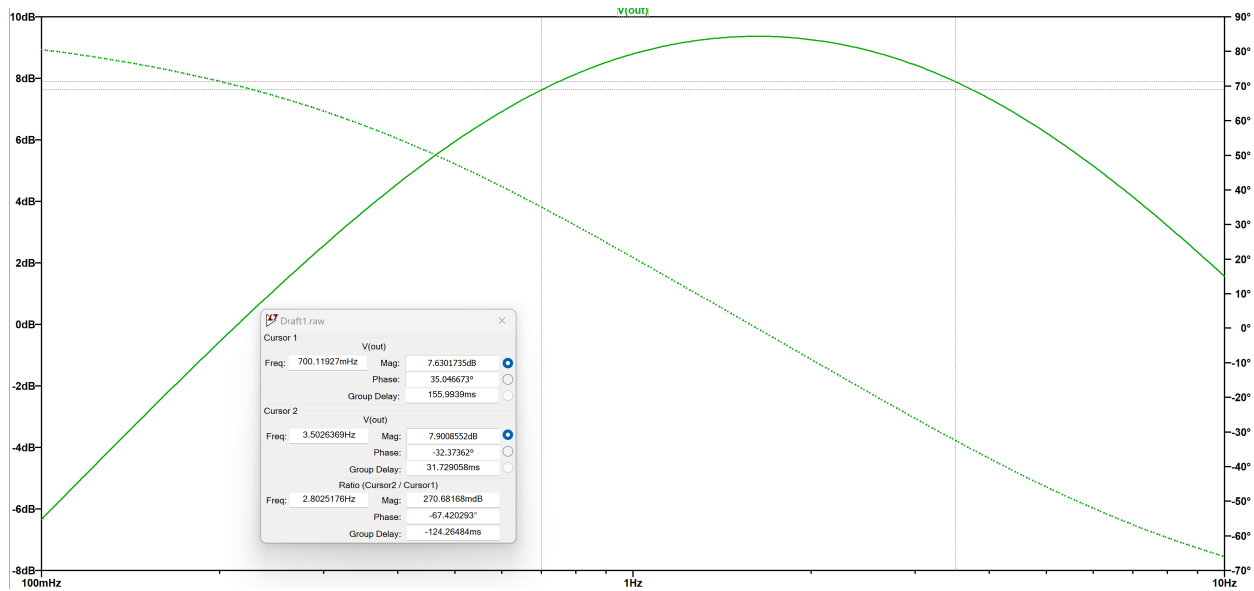

Figure 11: Complete Circuit Bode Simulation

The figure shows that the gain of the complete circuit has a maximum of around 9.5 dB at 1.5 Hz. The calculated cutoff frequencies of 0.7 Hz and 3.5 Hz are at 7.6 dB and 7.9 dB, respectively, which is approximately correct. The figure also shows that the phase shift of the circuit is approximately 80 degrees at low frequencies (around 100 mHz) and -65 degrees at high frequencies (around 10 Hz), which is close to the expected values. The phase shift

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has the general behavior of decreasing from 80 to -65 degrees as the frequency increases. The phase shift is approximately 30 degrees at the lower cutoff frequency and -30 degrees at the upper cutoff frequency, which is also close to the expected values.

The final output of the circuit was then simulated using a time domain simulation with an input of a 35 mV sinusoidal wave with a frequency of 1 Hz and offset of 0.5 V. Figure 12 shows the simulation of the complete circuit.
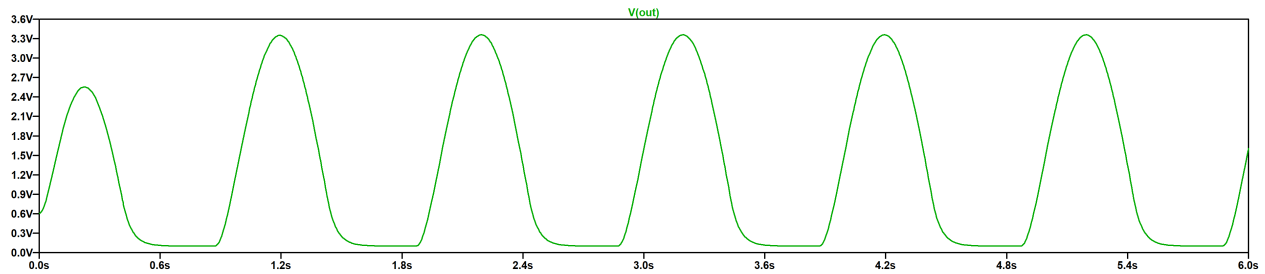

Figure 12: Complete Circuit Time Domain Simulation

The figure shows that the output of the circuit is a conditioned sinusoidal wave with a frequency of 1 Hz, which is the expected behavior. The amplitude of the wave is approximately 3.3 V, which correctly reflects an amplified signal from the OPB745 (in pass band).

The complete circuit was constructed on a breadboard and tested using an oscilloscope. A function generator was used to generate input waves at 200 mHz, 1 Hz, and 10 Hz to simulate a heartbeat at different BPM. Figure 13 shows the oscilloscope capture of the output of the circuit at 200 mHz (12 BPM).
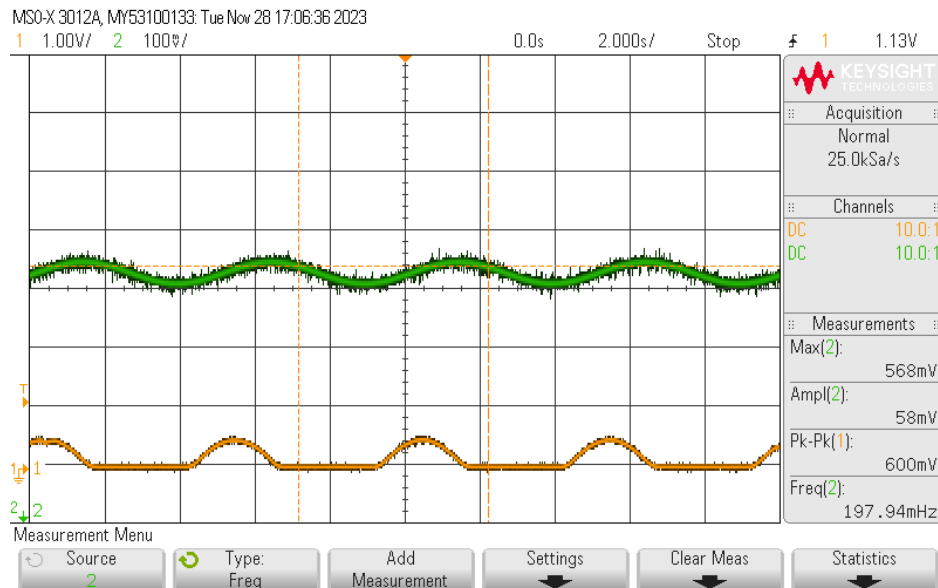

Figure 13: Oscilloscope capture at 200 mHz (stop band)

Figure 13 shows that the output of the circuit is a sinusoidal wave with a frequency of 200 mHz, which is the expected behavior. The amplitude of the wave is approximately 0.6 V, which correctly reflects a filtered signal from the OPB745 (in stop band).

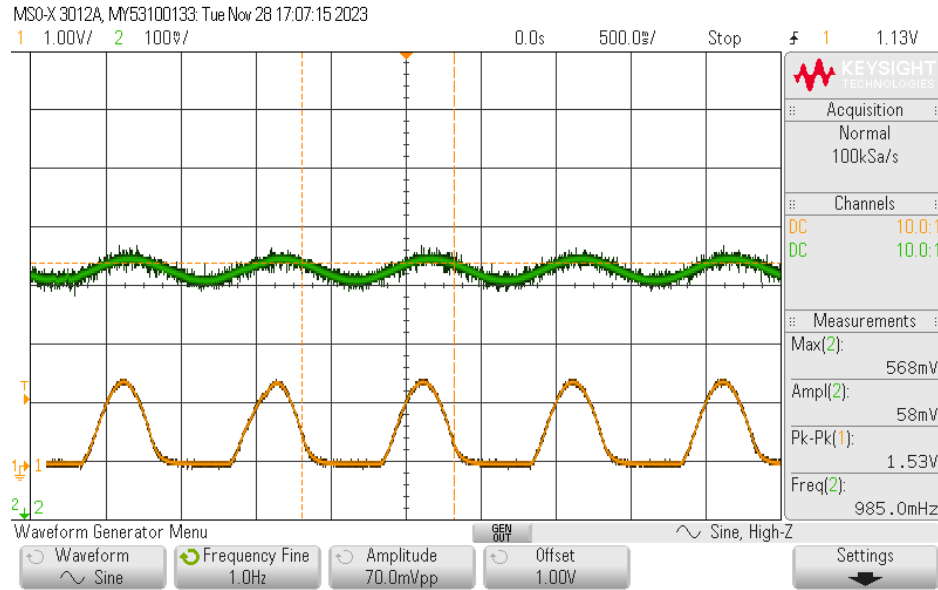Figure 14 shows the oscilloscope capture of the output of the circuit at 1 Hz (60 BPM).

Figure 14: Oscilloscope capture at 1 Hz (pass band)

Figure 14 shows that the output of the circuit is a sinusoidal wave with a frequency of 1 Hz, which is the expected behavior. The amplitude of the wave is approximately 1.53 V, which correctly reflects an amplified signal from the OPB745 (in pass band). The amplitude of the wave is also approximately half of the simulated value, which is attributed to the decreased gain of the high-pass filter of the circuit.

Figure 15 shows the oscilloscope capture of the output of the circuit at 10 Hz (600 BPM).
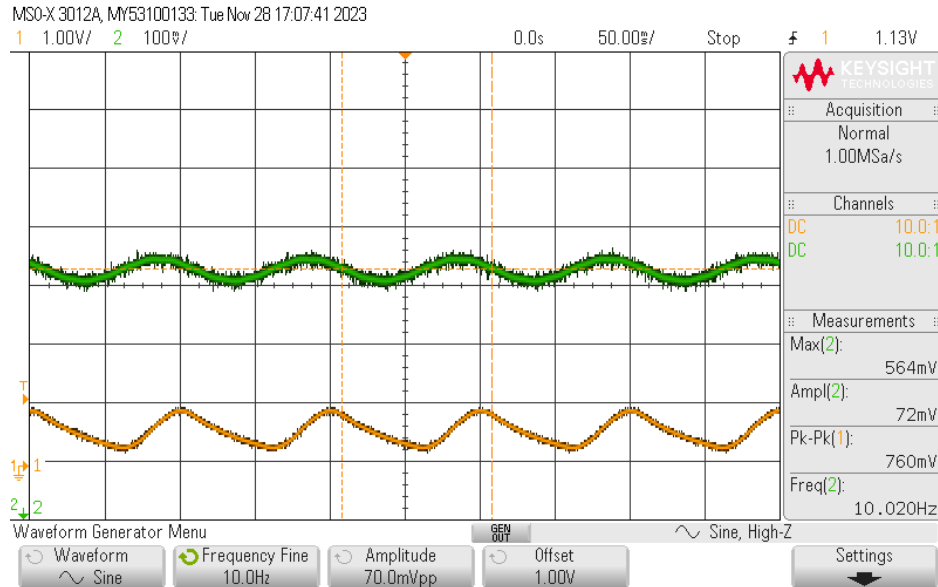
Figure 15: Oscilloscope capture at 10 Hz (stop band)

Figure 15 shows that the output of the circuit is a sinusoidal wave with a frequency of 10 Hz, which is the expected behavior. The amplitude of the wave is approximately 0.76 V, which correctly reflects a filtered signal from the OPB745 (in stop band).

The final output of the circuit was then fed into an MSP432 microcontroller to measure the frequency of the signal. The microcontroller was programmed to measure the frequency of the signal and output the frequency in beats per minute (BPM) to a serial monitor. The microcontroller was programmed to execute interrupts to capture the ADC value of the signal. The ADC value was then used to calculate BPM by measuring time between passing a constant threshold value. The following is the code used:

```
#define CAPTURE_FREQ (122)    // frequency of ADC data capture
#define VOLTAGE_CUTOFF (5000) // voltage cutoff for a heartbeat
unsigned int count = 10001;   // number of ADC values below voltage cutoff
unsigned int previous = 0;    // previous ADC value
double prev_bpm = -1;         // previous BPM
static char str[100];         // string for UART output

// Interrupt Service Routine for Timer32-1
void Timer32_1_ISR(void) {
    char str[30];
    unsigned int num = ADC_In(); // read ADC value

    // if previous ADC value was below voltage cutoff and current ADC
    // value is above voltage cutoff, calculate BPM
    if (num >= VOLTAGE_CUTOFF && previous < VOLTAGE_CUTOFF){
        // calculate BPM and difference from previous BPM
```

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```
        double bpm = (CAPTURE_FREQ * 60) / count;
        int abs = bpm - prev_bpm;
        if (abs < 0) abs = abs * -1;
        count = 0; // reset count
        // if BPM is between 40 and 220 and difference from previous BPM is
        // less than 11 (stops fluctuations), output BPM
        if (bpm > 40 && bpm < 220 && abs < 11) {
            sprintf(str, "Heart %d BPM\r\n", (int)bpm);
            uart0_put(str);
        }
        prev_bpm = bpm; // update previous BPM
    }
    else { count++; } // increment count if under voltage cutoff
    previous = num;  // update previous ADC value
}

int main(void) {
    DisableInterrupts();
    // initialize hardware
    uart0_init();
    ADC0_InitSWTriggerCh6();
    // initialize adc capture timer with capture frequency
    Timer32_1_Init(&Timer32_1_ISR, SystemCoreClock / CAPTURE_FREQ, T32DIV1);
    EnableInterrupts();
    uart0_put("Initialized\r\n");
    while (1) {}
}
```
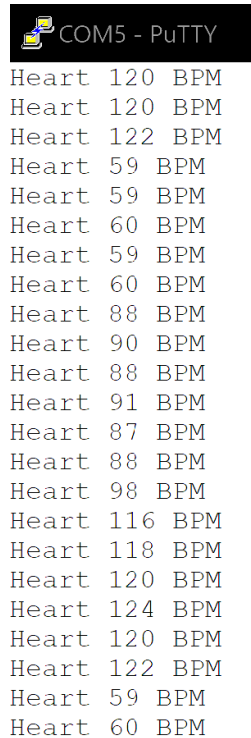
The code shows that the BPM was calculated by counting the number of ADC values that were below a certain voltage cutoff relative to all ADC values. The ADC values were captured at a frequency of 122 Hz. The BPM was then calculated using Equation 8.

$$\text{BPM} = \frac{\text{CAPTURE\_FREQ} \times 60}{\text{count}} \tag{8}$$

The code shows that the BPM was only calculated if the BPM was between 40 and 220 and the difference between the current BPM and the previous BPM was less than 11. This was done to prevent the BPM from fluctuating too much, providing a more stable reading.

The microcontroller was then connected to the circuit and the circuit was tested using a function generator to generate input wave to simulate a heartbeat at different BPM. Figure 16 shows the output of the serial monitor.

Figure 16: Serial Monitor Output

The figure shows that the output of the serial monitor is the BPM of the input wave, which was manually set to 2 Hz, 1 Hz, 1.5 Hz, 2 Hz, and then 1 Hz. The BPM is calculated to to be 120, 60, 90, 120, and 60, respectively, which matches the output shown in the figure. The output also shows slight fluctuations in the BPM of ± 1, which is attributed to noise.

Questions

1. *What is the ERC and DRC for?*
ERC stands for Electrical Rule Check and DRC stands for Design Rule Check. The ERC checks for electrical errors in the schematic, such as unconnected pins. The DRC checks for design errors in the schematic, such as incorrect pin types.

2. *Did your circuit cutoff frequencies match your expected/calculated values? Explain*
The cutoff frequency of the low-pass filter of the circuit matched the calculated values. The cutoff frequencies of the high-pass and band-pass filters were slightly different than the calculated values, but were close enough to be considered correct.

3. *Did the gain of the circuit match the expected/calculated values? Explain*
The gain of the circuit was slightly lower than the calculated values, but was close enough to be considered correct, which is attributed to the use of a real op amp instead of an ideal op amp. The gain of the high-pass filter was approximately half of the calculated value, which propagated through the rest of the circuit, causing a decreased gain in the band-pass filter, and thus, the complete circuit.

Conclusion

This report details the design, simulation, construction, and testing of a heart rate monitoring circuit. The exercise achieved partial success, demonstrated by the effective performance of the constructed circuit with an oscilloscope-generated sinusoidal signal and its compatibility with the MSP432 microcontroller for heartbeat frequency detection. However, problems and limitations were encountered, such as the inability of the OPB745 sensor in the constructed circuit to detect an actual heartbeat and the gain drop in the high-pass filter stage of the circuit. The experimental results were generally consistent with the simulations, showing slight deviations in cutoff frequencies and gain values, which can be attributed to the practical limitations of real-world components versus idealized simulation models and calculations.

Exercise 8: Heartrate Monitor

Student's Name: **Trent Wesley**   Section: **L1**

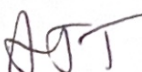|	Demo	Point Value	Points Earned	Date
Demo	Pre-Lab (Individual)	10	10	ATT 11/8
	LTspice and Plots for HRM	10	10	ATT 11/20
	Completed HRM	20	20	
	PCB Design and Layout (Individual)	10		

Bonus: Working HRM with OPB745 (10 pts) _____

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 8: Heartrate Monitor

Student's Name: Mohammed Fareed   Section: 1

Demo		Point Value	Points Earned	Date
Demo	Pre-Lab (Individual)	10		
	LTspice and Plots for HRM	10	10	AJJ 11/2e
	Completed HRM	20	20	
	PCB Design and Layout (Individual)	10		

Bonus: Working HRM with OPB745 (10 pts) _____

To receive any grading credit students must earn points for both the demonstration and the report.