CMPE 460 Laboratory Exercise 8

Heartrate Monitor

Mohammed Fareed
Trent Wesley
Performed: November 8, 2023
Submitted: November 29, 2023

Lab Section: 1
Instructor: Prof. Hussin Ketout
TA: Andrew Tevebaugh
Colin Vo

Lecture Section: 1
Professor: Prof. Hussin Ketout

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: _____

Abstract

This laboratory exercise involved the design and construction of a heartbeat detection circuit. For the detection of a heartbeat, a OPB745 reflective optical sensor can be used. This device will emit light through a finger and ideally measure reflected light which varies with the pulse within the arteries of a finger. The signal output is then filtered with a low pass filter and a high pass filter to exclude frequencies outside an expected range of heart rates. The resulting signal is then amplified by an op amp to get a more useable signal. This circuit was designed, simulated using LTspice, constructed on a breadboard, and measured. C code was written with an MSP432 microcontroller which would measure pulse based on the output of the constructed circuit. This exercise also includes the design of a PCB with the same heartbeat detection circuit. This exercise was partially successful since the circuit constructed behaved as expected with an oscilloscope generated sinusoidal signal. The circuit output was accurately used by the MSP432 to detect frequency in beats per minute. The circuit constructed was unable to detect a heartbeat using the OPB745 and the PCB was not designed.

Design Methodology

A PPG is an instrument used to measure changes in blood volume under the skin. One use of this is to measure heart rate. A circuit was designed with the intent to measure pulse within a finger using a OPB745 reflective optical sensor.

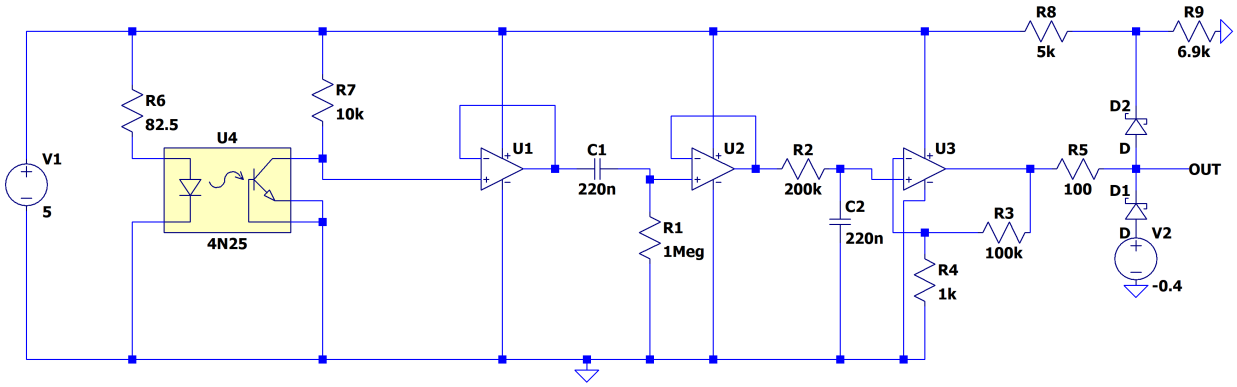

Figure 1: LTspice Schematic

Figure 1 shows the complete schematic designed. The 4N25 represents the OPB745. A 5V source is used to provide power to the OPB745, op amps, and a Schottky diode. Voltage division occurs between the 10kΩ rseistor and the photodetector. This signal then goes to voltage follower op amp which isolates the signal from the next stage. The signal is then filtered by a passive high pass RC filter. This filter has a cut off frequency of 0.7Hz which is 40bpm. The equation to for the high pass filter design is shown below.

$$R = \frac{1}{2 * \pi * C * \mathrm{f_c}} = \frac{1}{2 * \pi * 220nF * 0.7Hz} = 1M\Omega \tag{1}$$

With a cut off frequency of 0.7Hz and a capacitor value of 220nF, 1 shows that the appropriate resistor value is 1MΩ. The signal from the high pass filter then goes through another voltage follower for isolation between stages. Next, the signal is filtered by a passive low pass RC filter. This filter has a cut off frequency of 3.5Hz which is 210bpm. The equation to for the low pass filter design is shown below.

$$R = \frac{1}{2 * \pi * C * \mathrm{f_c}} = \frac{1}{2 * \pi * 220nF * 3.5Hz} = 200k\Omega \tag{2}$$

With a cut off frequency of 3.5Hz and a capacitor value of 220nF, 2 shows that the appropriate resistor value is 200kΩ.

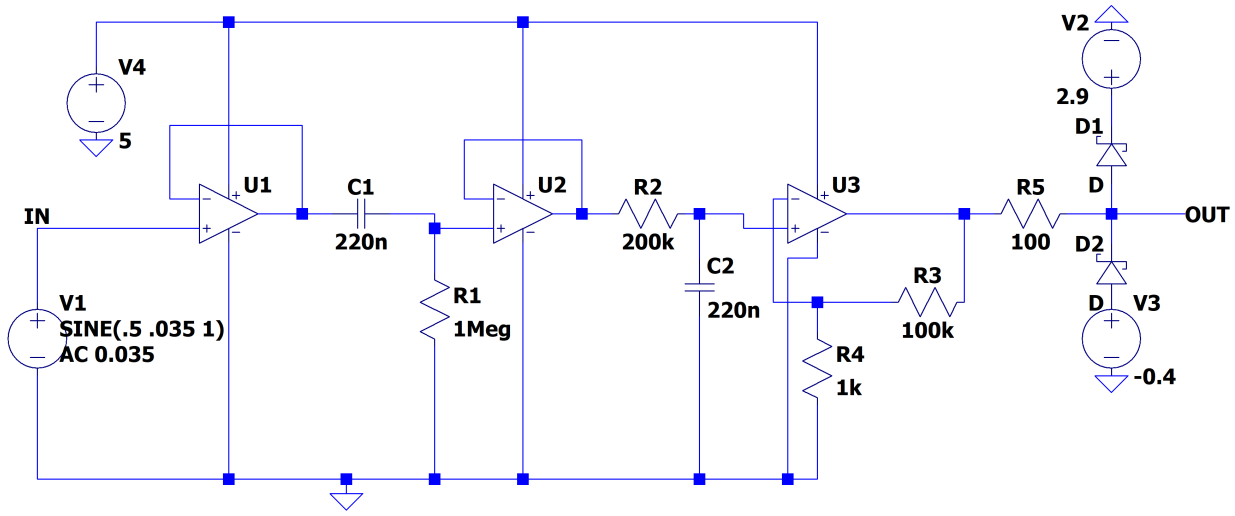

Figure 2: LTspice Schematic

Results and Analysis

The circuit was both simulated and constructed on a breadboard, with each stage of the circuit tested and compared. Figure 3 shows the simulation of the high-pass filter of the circuit, performed using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz.

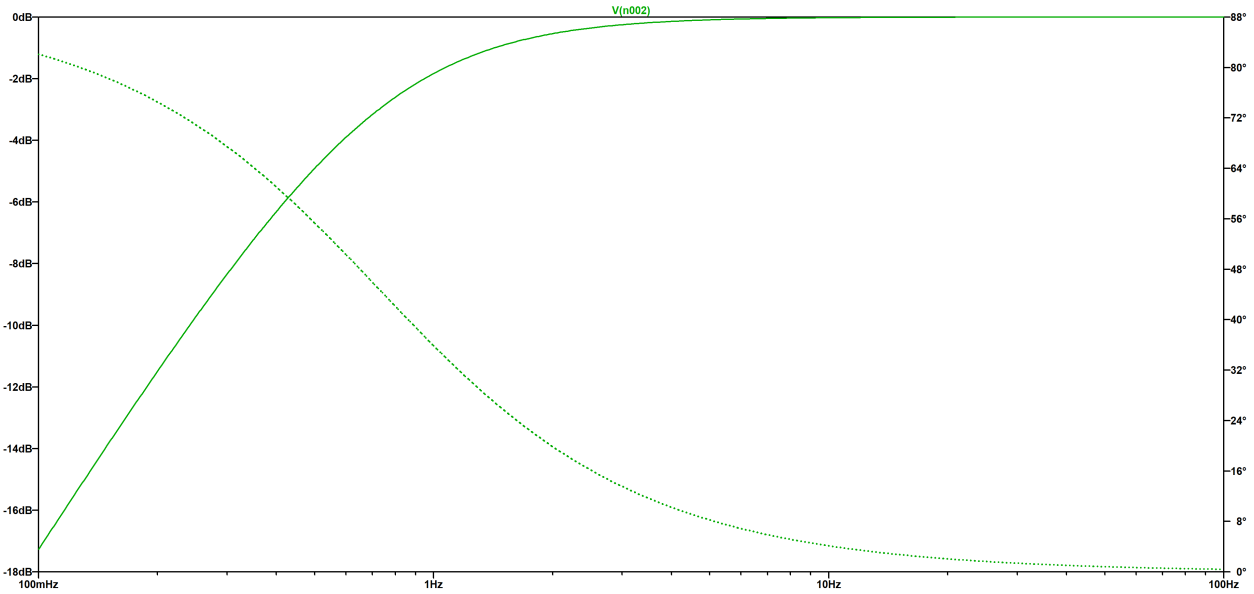

Figure 3: High-Pass Filter Bode Simulation

The figure shows that the gain of the circuit is approximately 0 in the pass band, decreasing as the frequency decreases. The figure also shows that the phase shift of the circuit is approximately 90 degrees in the pass band, decreasing to 0 as the frequency decreases. The cutoff frequency of the circuit is approximately 0.7 Hz, which is equal to the calculated value. The high-pass filter of the circuit was constructed on a breadboard and tested using an oscilloscope and a function generator at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 4 shows the resulting Bode plot.

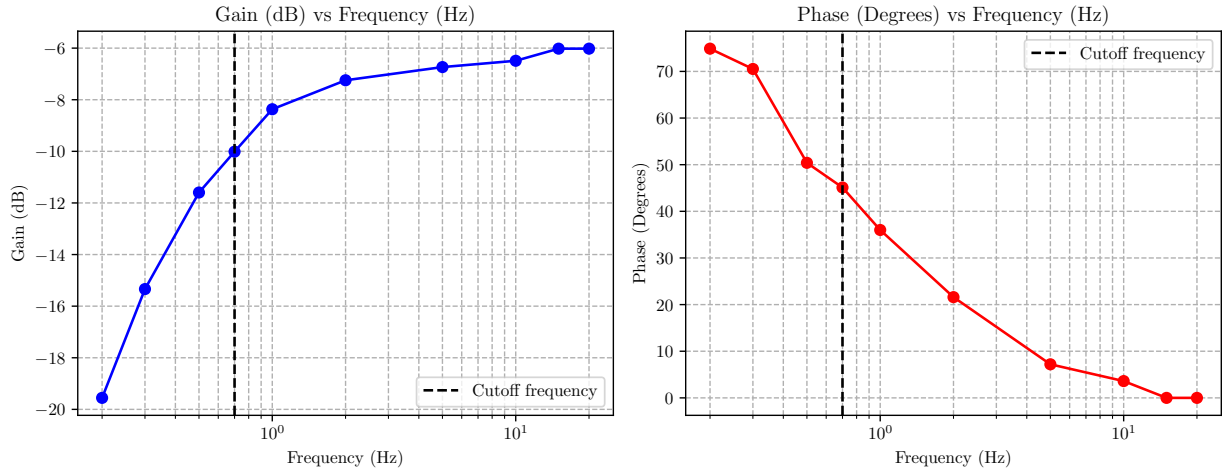

Figure 4: High-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequency of 0.7 Hz is approximately correct. The cutoff frequency on the plot is slightly higher than the calculated value, using -9 dB as the cutoff point (3 dB less than the maximum gain). The plot shows that the phase shift

of the circuit is approximately 45 degrees at the cutoff frequency, decreasing to 0 degrees at higher frequencies. The phase shift has the general behavior of increasing from 75 to 0 degrees as the frequency increases.
The results show that the simulation and constructed circuit are similar, with the constructed circuit having a slightly higher cutoff frequency and a slightly lower phase shift at the cutoff frequency. The constructed circuit also has a lower maximum gain (-6 dB) than the simulated circuit (0 dB), which is likely due to the use of a real op amp instead of an ideal op amp.

The low-pass filter of the circuit was simulated using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz. Figure 5 shows the simulation of the low-pass filter of the circuit.

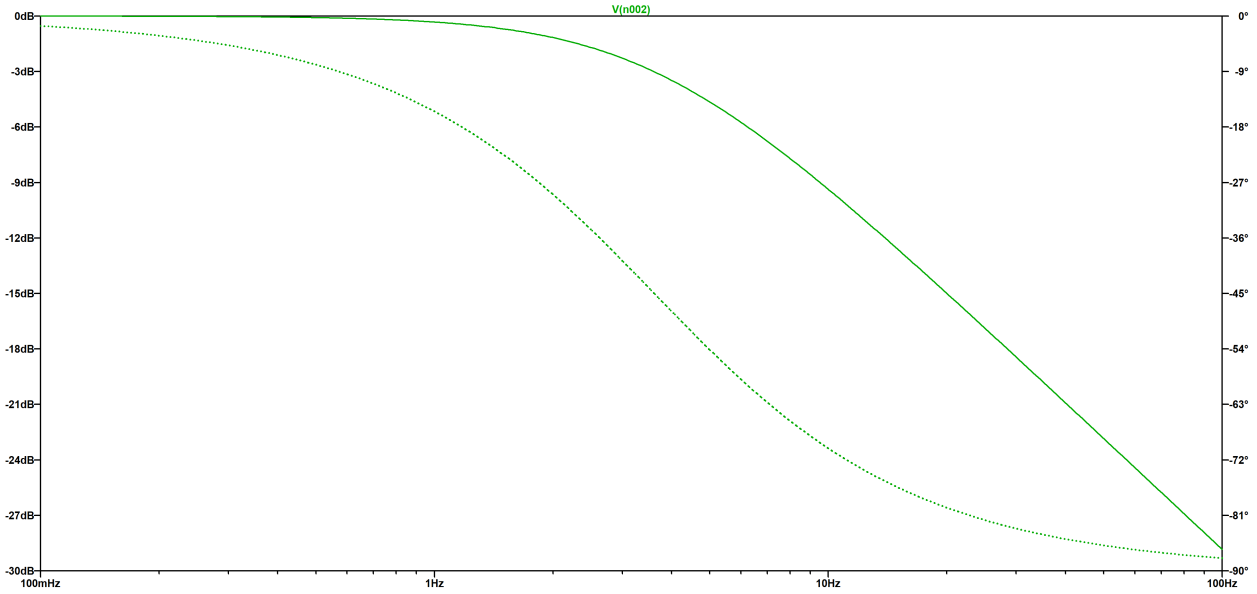

Figure 5: Low-Pass Filter Bode Simulation

The figure shows that the gain of the circuit is approximately 0 in the pass band, increasing as the frequency increases. The figure also shows that the phase shift of the circuit is approximately 0 degrees in the pass band, decreasing to -90 degrees as the frequency increases. The cutoff frequency of the circuit is approximately 3.5 Hz, which is equal to the calculated value.
The low-pass filter of the circuit was constructed on a breadboard and tested using an oscilloscope and a function generator at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 6 shows the resulting Bode plot.

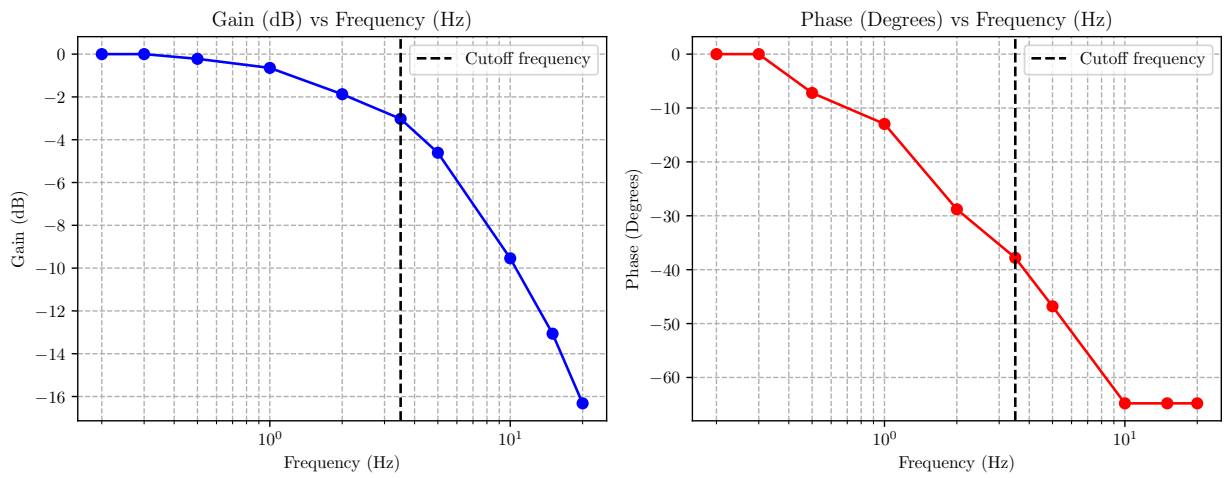

Figure 6: Low-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequency of 3.5 Hz is approximately correct. The cutoff frequency on the plot falls at the calculated value, using -3 dB as the cutoff point (3 dB less than the maximum gain). The phase shift of the circuit is approximately -38 degrees at the cutoff frequency, decreasing to -65 degrees at higher frequencies, which is the expected behavior. The phase shift has the general behavior of decreasing from 0 to -65 degrees as the frequency increases.
The results show that the simulation and constructed circuit are very similar, with no significant differences between the two.

The band-pass filter of the circuit was simulated using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz. Figure 7 shows the simulation of the band-pass filter of the circuit.

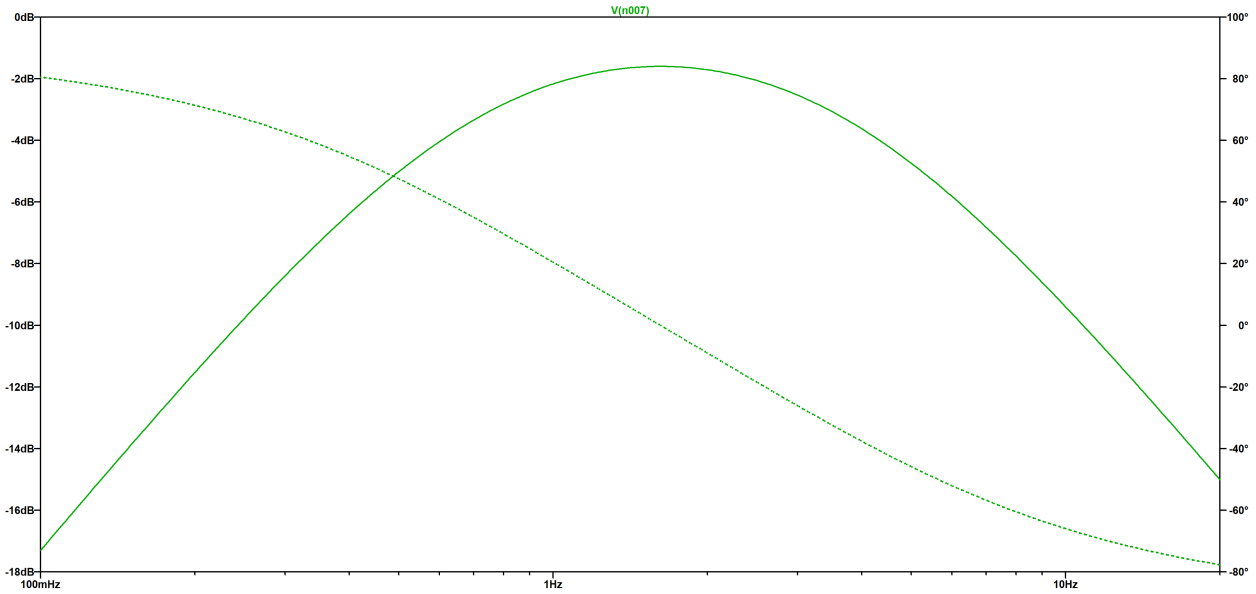

Figure 7: Band-Pass Filter Bode Simulation

The figure shows that the gain of the circuit is approximately -3 and -1 in the pass band, with cutoff frequencies of 0.7 Hz and 3.5 Hz, which matches the calculated values. The figure also shows that the phase shift of the circuit is approximately 80 degrees at low frequencies (around 100 mHz) and -80 degrees at high frequencies (around 100 Hz), which is the expected behavior. The phase shift has the general behavior of decreasing from 80 to -80 degrees as the frequency increases. The phase shift is approximately 50 degrees at the lower cutoff frequency and -25 degrees at the upper cutoff frequency, which is the expected behavior.
The band-pass filter of the circuit was constructed on a breadboard and tested using an oscilloscope and a function generator at different input frequencies and the resulting voltage gain and phase shift were plotted. Figure 8 shows the resulting Bode plot.

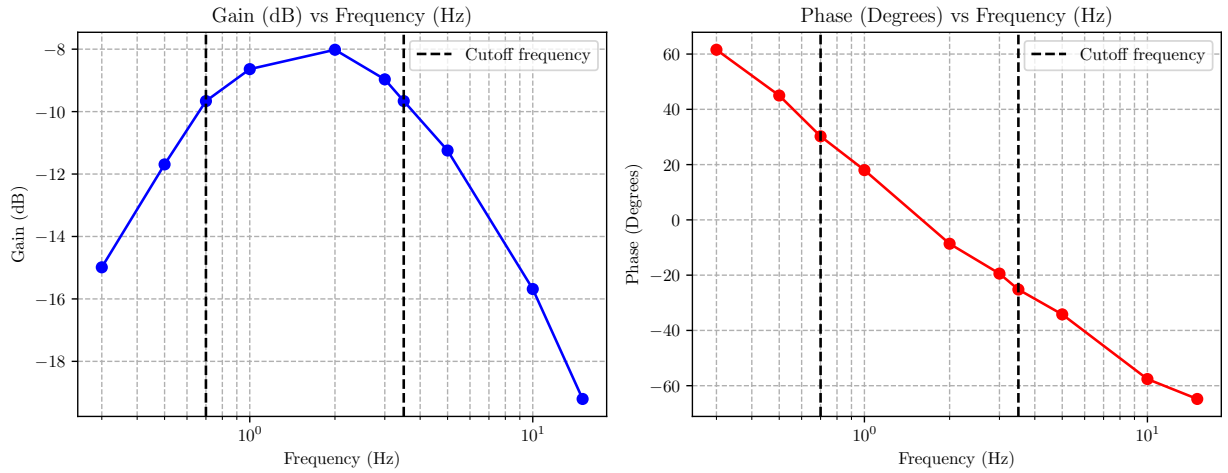

Figure 8: Band-Pass Filter Bode Plot

The figure shows that the calculated cutoff frequencies of 0.7 Hz and 3.5 Hz are approximately correct. Using -11 dB as the cutoff point (3 dB less than the maximum gain), the lower cutoff frequency is slightly lower than the calculated value and the upper cutoff frequency is slightly higher than the calculated value. The phase shift of the circuit is approximately 30 degrees at the lower cutoff frequency, decreasing to -25 degrees at the upper cutoff frequency, which is the expected behavior. The phase shift has the general behavior of decreasing from 60 to -65 degrees as the frequency increases.
The results show that the simulation and constructed circuit are similar, with the constructed circuit having a slightly lower lower cutoff frequency and a slightly higher upper cutoff frequency. The constructed circuit also has a lower maximum gain (-8 dB) than the simulated circuit (-2 dB), which is likely due to the use of a real op amp instead of an ideal op amp. The phase shift of the constructed circuit is also slightly lower than the simulated circuit at the lower cutoff frequency.

The complete circuit was then simulated using an AC sweep with a logarithmic scale from 100 mHz to 100 Hz. Figure 9 shows the simulation of the complete circuit.

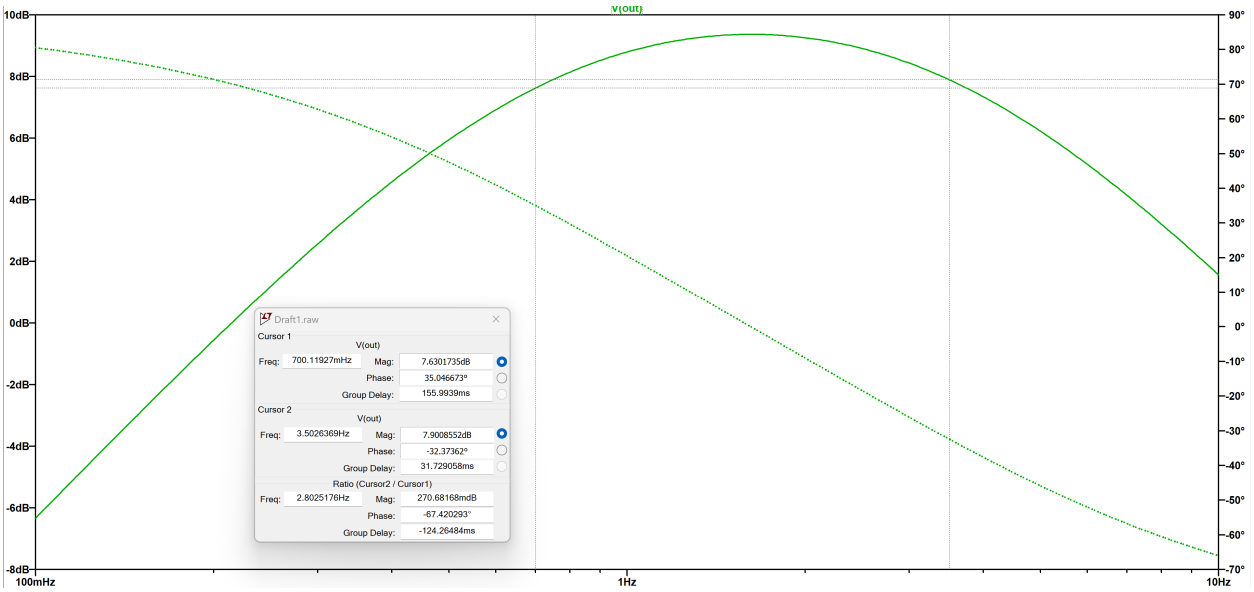

Figure 9: Complete Circuit Bode Simulation

The figure shows that the gain of the complete circuit has a maximum of around 9.5 dB at 1.5 Hz. The calculated cutoff frequencies of 0.7 Hz and 3.5 Hz are at 7.6 dB and 7.9 dB, respectively, which is approximately correct. The figure also shows that the phase shift of the circuit is approximately 80 degrees at low frequencies (around 100 mHz) and -65 degrees at high frequencies (around 100 Hz), which is close to the expected values. The phase shift has the general behavior of decreasing from 80 to -65 degrees as the frequency increases. The phase shift is approximately 30 degrees at the lower cutoff frequency and -30 degrees at the upper cutoff frequency, which is also close to the expected values.
The final output of the circuit was then simulated using a time domain simulation with an input of a 1 V sinusoidal wave with a frequency of 1 Hz. Figure 10 shows the simulation of the complete circuit.

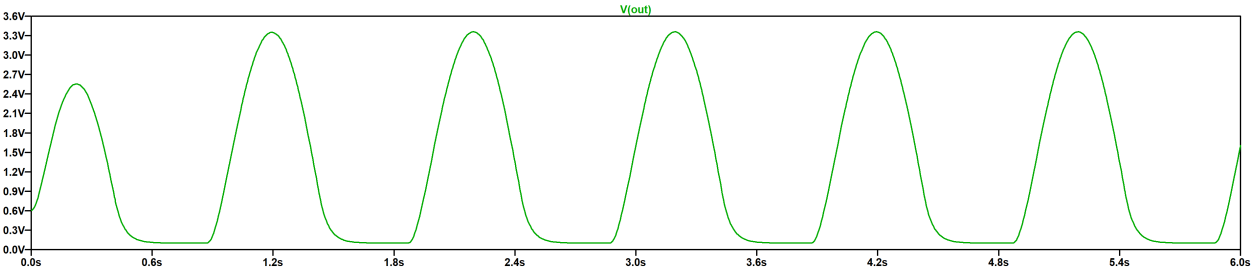

Figure 10: Complete Circuit Time Domain Simulation

The figure shows that the output of the circuit is a conditioned sinusoidal wave with a frequency of 1 Hz, which is the expected behavior. The amplitude of the wave is approximately 3.3 V, which correctly reflects an amplified signal from the OPB745 (in pass band).
The complete circuit was constructed on a breadboard and tested using an oscilloscope. A function generator was used to generate input waves at 200 mHz, 1 Hz, and 10 Hz to simulate

a heartbeat at different BPM. Figure 11 shows the oscilloscope capture of the output of the circuit at 200 mHz (12 BPM).

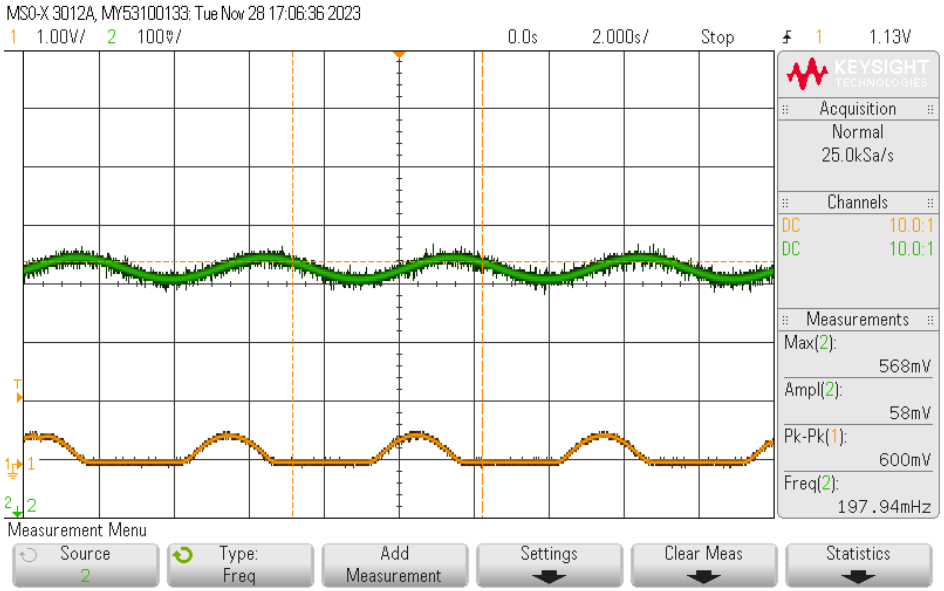

Figure 11: Oscilloscope SCHTUFF

Figure 11 shows that the output of the circuit is a sinusoidal wave with a frequency of 200 mHz, which is the expected behavior. The amplitude of the wave is approximately 0.6 V, which correctly reflects a filtered signal from the OPB745 (in stop band).
Figure 12 shows the oscilloscope capture of the output of the circuit at 1 Hz (60 BPM).

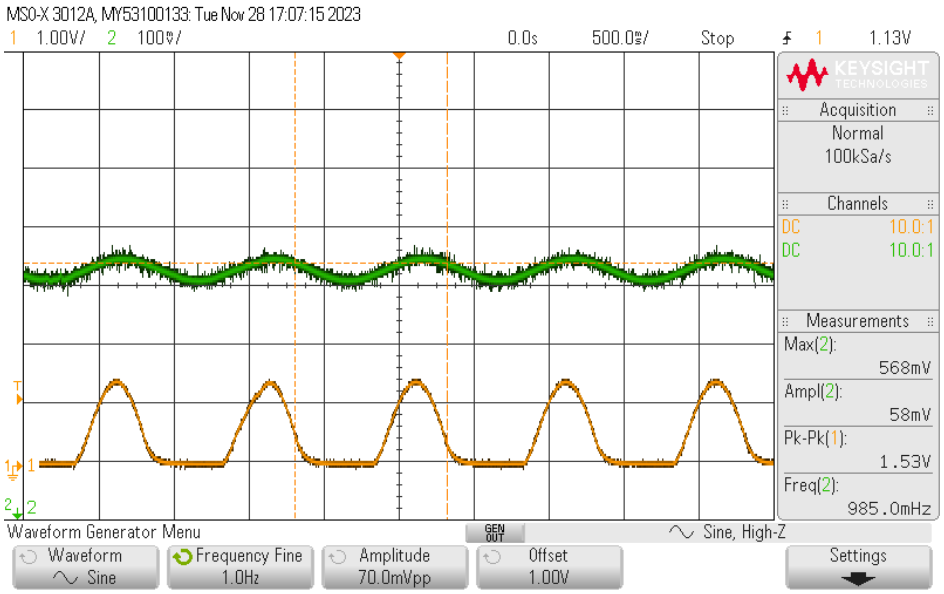

Figure 12: Oscilloscope SCHTUFF

Figure 12 shows that the output of the circuit is a sinusoidal wave with a frequency of 1 Hz,

which is the expected behavior. The amplitude of the wave is approximately 1.53 V, which correctly reflects an amplified signal from the OPB745 (in pass band).
Figure 13 shows the oscilloscope capture of the output of the circuit at 10 Hz (600 BPM).

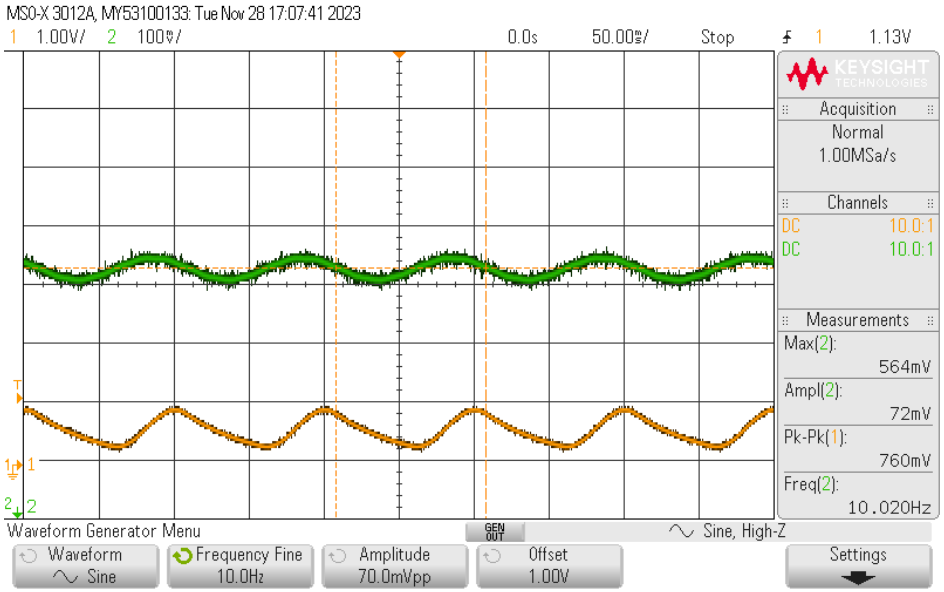

Figure 13: Oscilloscope SCHTUFF

Figure 13 shows that the output of the circuit is a sinusoidal wave with a frequency of 10 Hz, which is the expected behavior. The amplitude of the wave is approximately 0.76 V, which correctly reflects a filtered signal from the OPB745 (in stop band).

Questions

1. *What is the ERC and DRC for?*
ERC stands for Electrical Rule Check and DRC stands for Design Rule Check. The ERC checks for electrical errors in the schematic, such as unconnected pins. The DRC checks for design errors in the schematic, such as incorrect pin types.

2. *Did your circuit cutoff frequencies match your expected/calculated values? Explain*

3. *Did the gain of the circuit match the expected/calculated values? Explain*

Conclusion