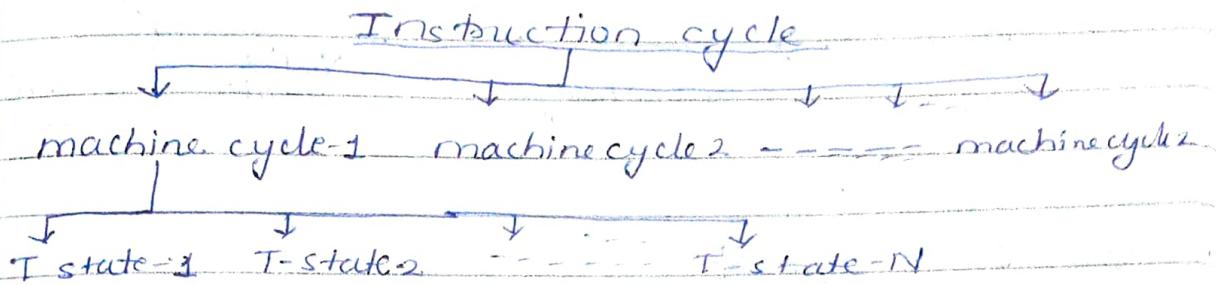


## Unit - 3<sup>rd</sup>

### → Timing operation:-



### Instruction cycle:-

Instruction cycle is defined at the time required to complete the execution of an instruction.

### Machine cycle:-

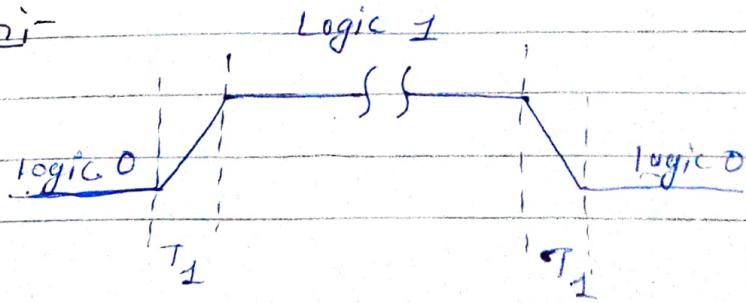
It is defined as the time required to complete one operation, the operation can be accessing memory, input output or acknowledging and external request.

### T-state:-

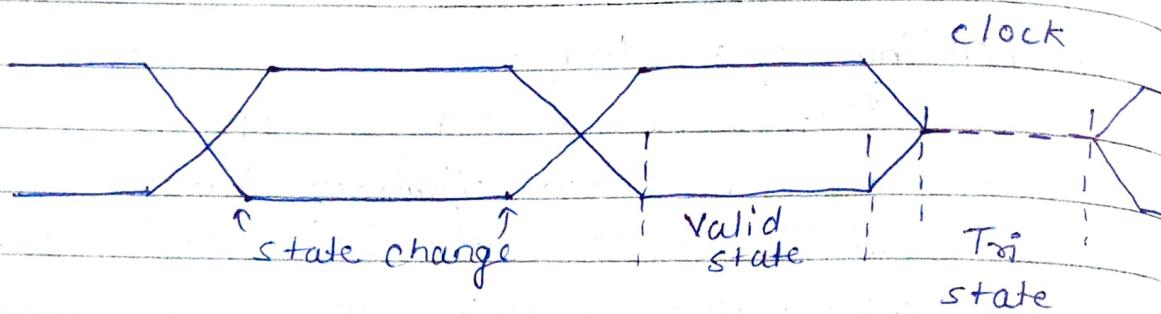
T-state is defined as one sub-division of the operation performed in one clock period, this is the unit in which time of any operation is measured.

### → Timing diagrams:-

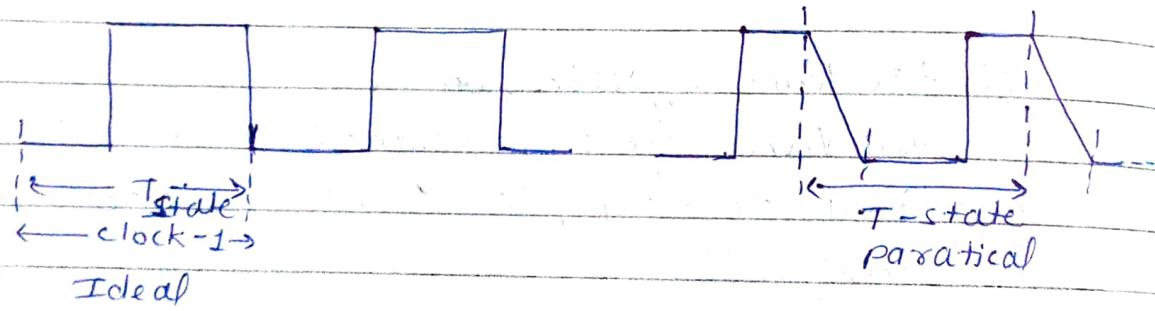
#### ① single signal:-



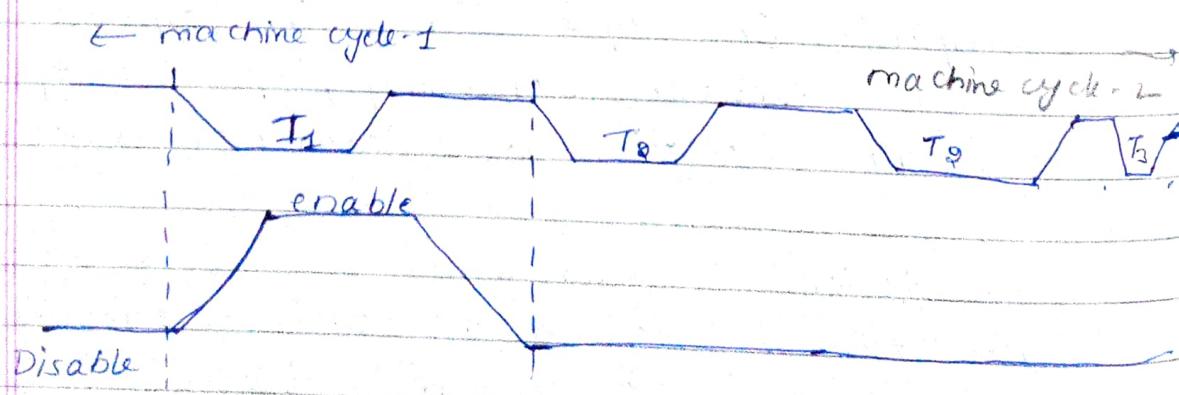
② Group of signal (Bus) :-



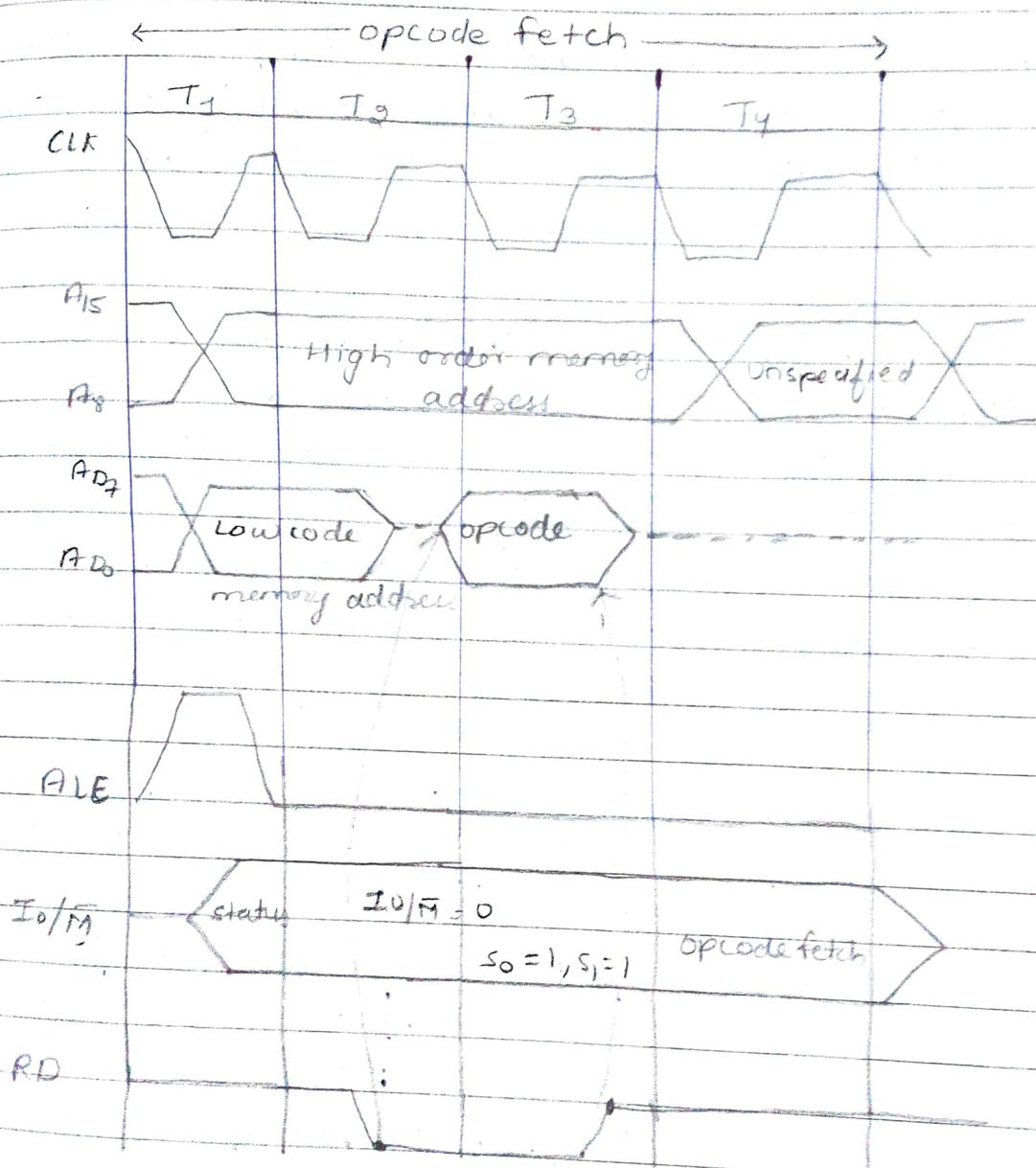
③ Clock signals :-



④ Address latch enables :-



## Opcode fetch machine cycle -



memory RD

memory WR

I<sub>O</sub> RD

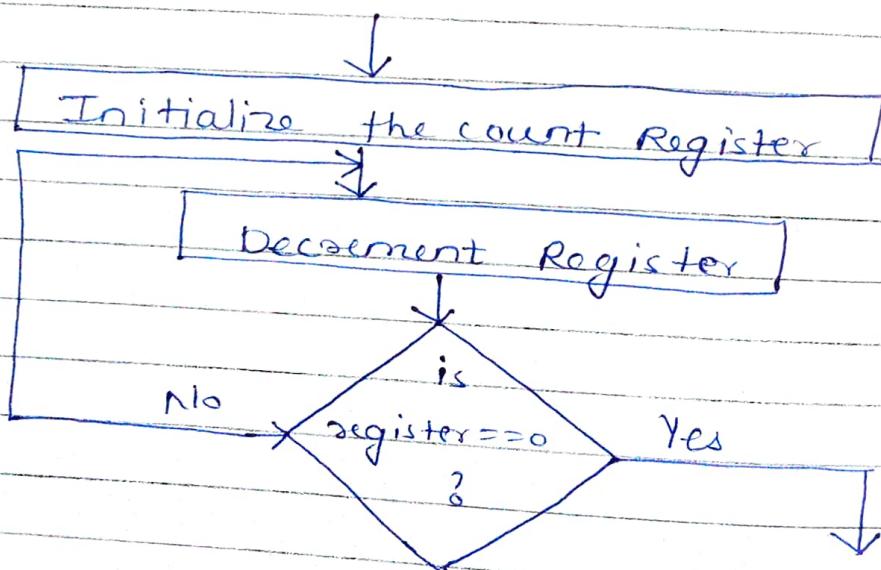
I<sub>O</sub> WR

## # Time delay using counter-

A counter can be used to provide the time delay according to this technique a counter is initialized with the desired value and decremented by 1.

This looping operation remains continue till the counted value reach to 0 since the execution time of the instruction used in counting are known the initial value of counter can be determined.

The counter can be designed by a register or register pair.



## Interrupts:-

The interrupts is define as a signal which is generated by peripheral to break the sequences of the main program and program execution jumps to pre-specified memory location.

## Classification of interrupts:-

- Software Interrupts "works during execution"
- Hardware interrupts.

1) a) Software interrupts- The interrupts caused by executing special interrupt special interrupt instruction called software interrupts.

The 8085 microprocessor instruction set includes 8- RST (Restart).

These instruction are executed in a similar way to that of all instruction.

Ques Explain RST or software induction?

Instruction	Binary code								Hex code	Call location
	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
RST 0	1	1	0	0	0	1	1	1	C7	0000H
RST 1	1	1	0	0	1	1	1	1	CF	0008H
RST 2	1	1	0	1	0	1	1	1	D7	0010H
RST 3	1	1	0	1	1	1	1	1	DF	0018H
RST 4	1	1	1	0	0	1	1	1	E7	0020H
RST 5	1	1	1	0	1	1	1	1	EF	0028H
RST 6	1	1	1	1	0	1	1	1	F7	0030H
RST 7	1	1	1	1	1	1	1	1	FF	0038H

b) Hardware Interrupts- The types of interrupt whose microprocessor pins are used to receive interrupt requests are called hardware interrupts.

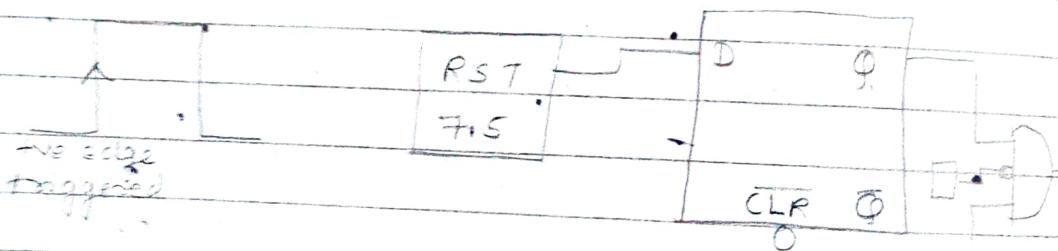
The 8085 microprocessor has 5 interrupts that are -

①	TRAP	vector	Non markable
②	RST 7.5	vector	markable
③	RST 6.5	vector	markable
④	RST 5.5	vector	markable
⑤	INTR (Non vector)		markable
	INTA	(Interrupt acknowledgement),	

- ① Vector and non-Vector interrupts.
- ② Markable and non-markable interrupts.

### Block diagram

Priority input mask-



## Interrupts Related instruction

EI → Enable interrupts

DI → Disable interrupts

SIM → set interrupts mask.

RIM → Read interrupts mask.

(i) EI → One byte instruction

non addressing mode

flags are not affected.

(ii) DI → 1 byte instruction

non addressing mode

and flags are not effective.

(iii) SIM → The instruction is used to set the  
interrupts mask. This is one byte instruction  
and operate on the data store in the  
accumulator

Implicit addressing mode.

Flag are non effective.

(iv) RIM → The RIM instruction is used to read  
the status of interrupts.

- one byte instruction.

- The status is stored in accumulator

- Implicit addressing mode.

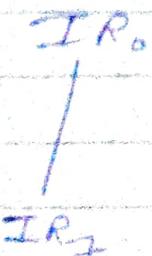
- flags are non - effective.

## Programmable Interrupt Controller (PIC) 8259

The 8259 can be used by provide additional interrupts other than software and Hardware interrupts of 8085 microprocessor.

\* Theory, points, functioning + Block diagram.

- ① It can manage 8 interrupt according to the instruction action into its control register.
- ② Vector an interrupt request anywhere in the memory map.
- ③ Provides 8-levels of interrupt priorities in a variety of modes:
  - fully nested mode → According to sequence of requests
  - automatic rotation mode → automatic change the specific rotation mode
- ④ Mask each interrupt request individually.
- ⑤ Read the status of pending interrupt, in-service interrupt and mask interrupt.
- ⑥ Be set-up to accept either the level triggered or the edge triggered interrupt request.
- ⑦ It is compatible with 8085, 8086, and 8088.

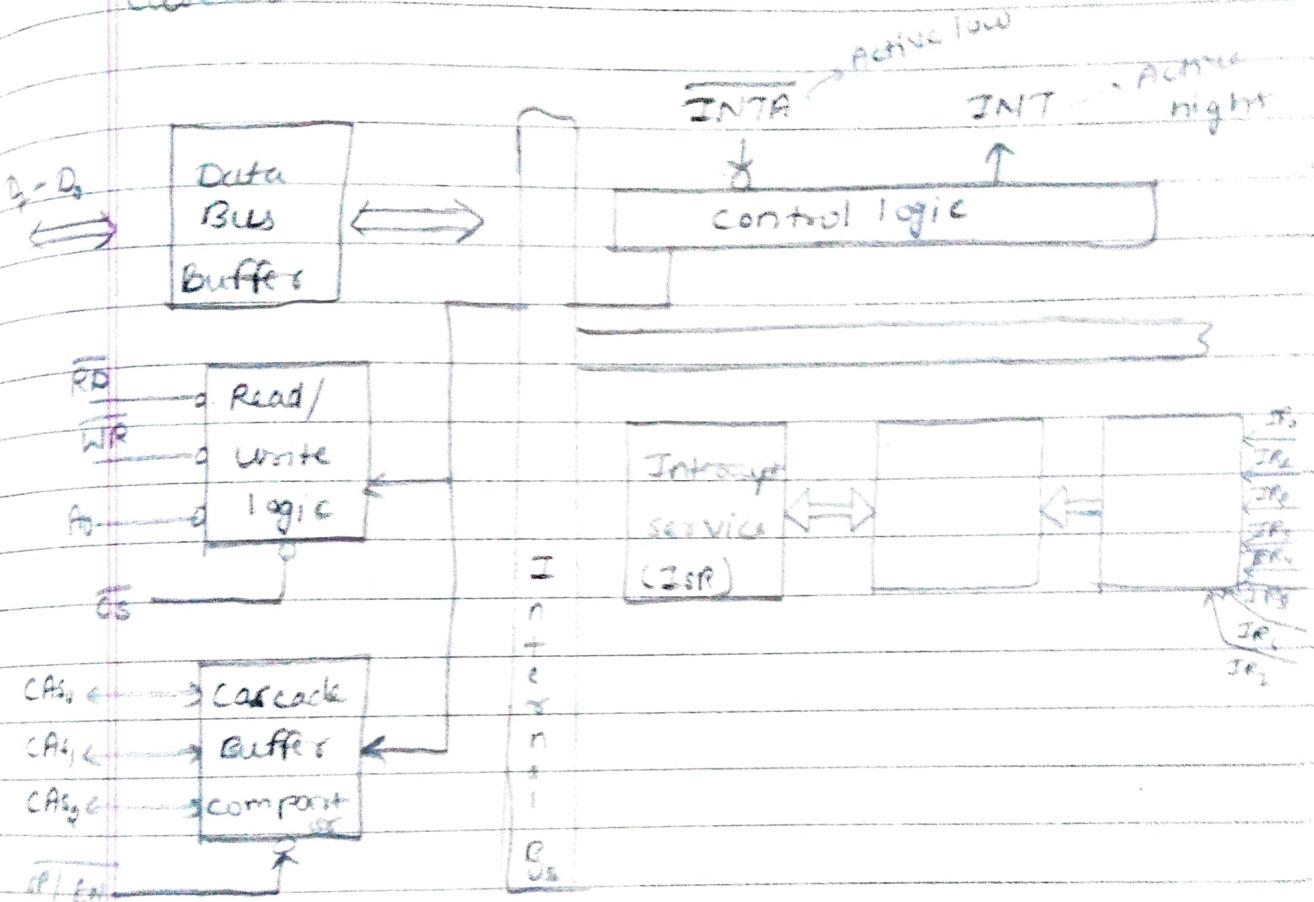


INTR\_low + priority

## Block diagram of 8259:-

(↑) control bus signal      (↔) Data Bus  
 (←) Address Bus

when 3 parallel 8259 is connected in cascade.



IRR - Interrupt request register.

The IRR has 8 interrupt input data ( $IR_0$  to  $IR_7$ ) when these lines goes high (1) the request R is stored in the register.

ISR - In-service Register.

The ISR stores all the interrupts those are currently being serviced.

IMR - Interrupt Mask register.

The IMR stores the masking bits of the interrupt lines to be masked.

Operation of interruption-

- If interrupt line ( $IR_0$  to  $IR_7$ ) are high it means the Request is stored and the corresponding IRR bit is set.
- All the three register are checked by parity resolver and INT pin set to high.
- Microprocessor acknowledge the interrupt by sending INTA pulse.
- When INTA pulse received from microprocessor the ISR bit with the highest parity is set and the corresponding IRR bit is reset.
- These after call instruction code is set on pin ( $D_0$  to  $D_7$ ).
- Two more INTA signal on the data bus are placed by decoding the code CALL instruction while

## Memory interfacing:

One of the most important part of the design of microprocessor or based systems is a design of interface.

The first part of it is the interface of memory following steps need to be followed to interface memory to microprocessor.

- (i) Calculate the number of address line required
- (ii) select the address lines from the available memory space
- (iii) Identify the pins those are required for interface.
- (iv) Design the logic circuit to fulfill the interfacing circuit required by to select the memory chip.

Note:- To control the reading and writing operation with the memory appropriate control signals are needed.

Truth table for memory operation:-

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$
1	1	0
0	1	0
1	0	0
0	0	0
X	X	1

Characteristics

Non-operation

Read data

Write data

illegal

Fifo state

Unit - 4# Programmable peripheral interface (PPI) - 8255

8255 is a programmable parallel input output device it can be programmed to transfer data under different conditions from simple input output.

It is flexible, versatile and economical.

The 8255 has 40 pins and out of these 24 input-output pins can be grouped in 8 bit parallel ports and that are

Port - A, Port - B and Port - C.

8 bit

8 bit

8 bit = 24 bit

8255 - pin diagram

PA <sub>3</sub>	1	40	PA <sub>7</sub>
PA <sub>2</sub>	2	39	PA <sub>5</sub>
PA <sub>1</sub>	3	38	PA <sub>6</sub>
PA <sub>0</sub>	4	37	PA <sub>7</sub>
RD	5	36	WR
CS	6	35	Reset
GND	7	34	D <sub>0</sub>
A <sub>1</sub>	8	33	D <sub>1</sub>
A <sub>0</sub>	9	32	D <sub>2</sub>
PG <sub>7</sub>	10	31	D <sub>3</sub>
PE <sub>6</sub>	11	30	D <sub>4</sub>
PG <sub>5</sub>	12	29	D <sub>5</sub>
PG <sub>4</sub>	13	28	D <sub>6</sub>
PG <sub>0</sub>	14	27	D <sub>7</sub>
PE <sub>1</sub>	15	26	V <sub>cc</sub>
PE <sub>2</sub>	16	25	PB <sub>7</sub>
PE <sub>3</sub>	17	24	PB <sub>6</sub>
PE <sub>4</sub>	18	23	PB <sub>5</sub>
PE <sub>5</sub>	19	22	PB <sub>4</sub>
PE <sub>6</sub>	20	21	PB <sub>3</sub>

PA<sub>0</sub> - PA<sub>7</sub>

PB<sub>0</sub> - PB<sub>7</sub>

PC<sub>0</sub> - PC<sub>7</sub>

input  
output

## 8255 - block diagram :-

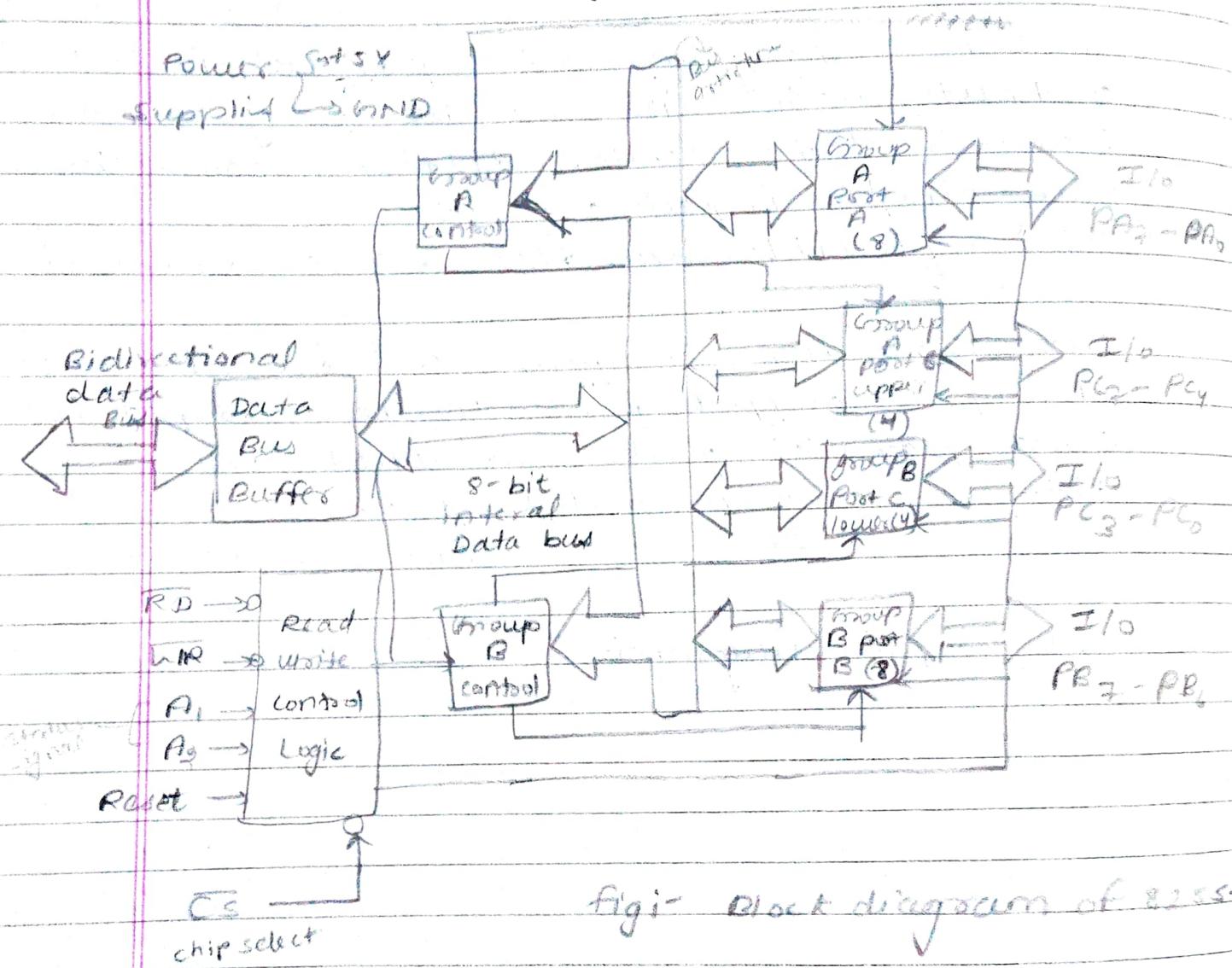
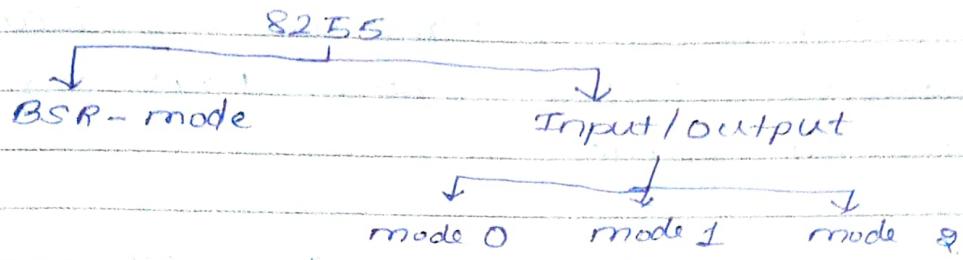


fig:- Block diagram of 8255

## Operation of 8255 :-

Table - address decoding of 8255.

CS	A <sub>1</sub>	A <sub>0</sub>	Port selected.
0	0	0	port - A
0	0	1	port - B
0	1	0	port - C
0	1	1	control-registers
1	X	X	8255 not selected



### Bit set / Reset - mode:-

The BSR mode includes only 8-bits of port-C which can be set or reset by writing the suitable control word in the control register.

In BSR mode  $D_7$  bit of control word is at logic 0 and it does not affect previously transmitted but with bit of  $D_7=1$  this indicate that input output operation of port-A and port-B are not altered by a BSR control word.

### mode-0:- (simple input / output mode)

In this mode port-A and port-B are used as two simple 8-bit input / output ports and port-C has two 4-bit ports. Each port can be programmed to function as simply an input port or an output port.

### mode-1:- (Input / output mode with handshake)

In this mode input or output data transfer is controlled by Handshake signal.

Handshake signals are used to transfer data between devices whose data transfer speed are not same.

Handshaking signals are used to inform the microprocessor whether peripheral is ready to communicate or not.

- Port-A and port-B function as a 8-bit input-output ports
- Each port uses the 3 lines from the port-C as the handshake signal.  
The remaining two lines of the port-C can be used for simple input output operation.

mode-2 : (Bidirectional data transfer)

This mode allows bidirectional data transfer over a single 8-bit data bus. Only in mode-2, port-A with port-B, has the 8-bit bidirectional data bus. Lines  $PL_3 - PL_7$  are used for handshaking purposes. The port-B can be configured in mode 0 or in mode-1.

Programmable Interval timer (PIT) 8253 / 8254

- The 8254 programmable interval timer is similar to software design counter and timers.
- Accurate time delay can be generated by both 8253 / 8254 IC.

- Software technique for generation time delay are not accurate and most microprocessors are busy in delay loop. So, to overcome this difficulty addition hardware in the form of 8253 or 8254 is used.
- 8254 can be used for application such as real-time clock and event counter or digital one shot, a square wave generator and complex wave generator.
- The 8254 includes three identical 16-bit counters that can operate independently in any one of the 6-modes.

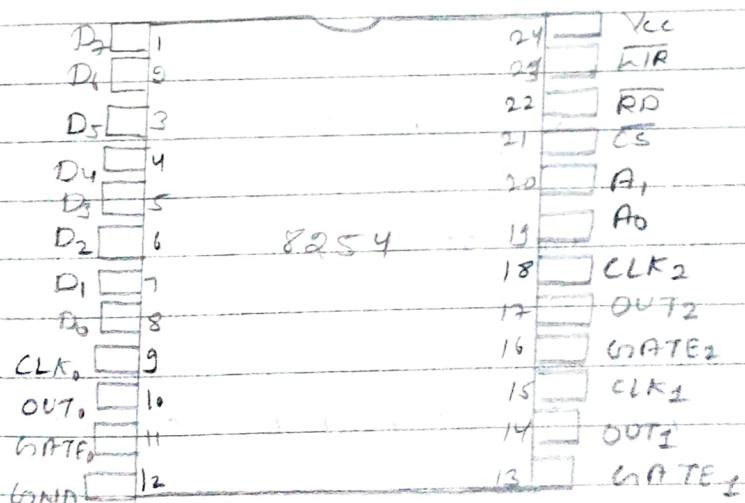


fig:- Pin Diagram of 8254

Block diagram - 8253/8254.

$$V_{CC} = +5V$$

$$V_{DD} = 0V$$

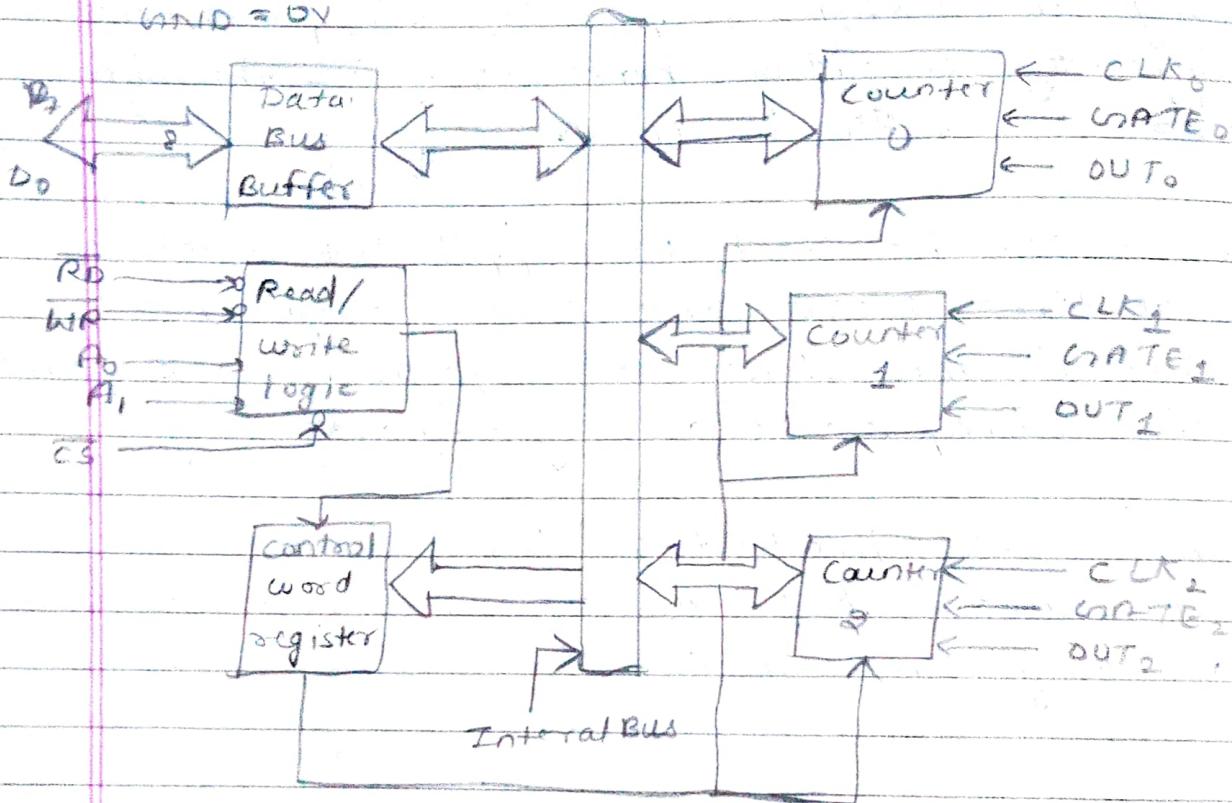


fig i - Block diagram of 8254

### Mode of operation of 8254:-

#### 1) Mode-0:-

(Interrupt on terminal count).  
define particular time period (low & high signal)

CLK

WR	$m=4$	4	13	9
----	-------	---	----	---

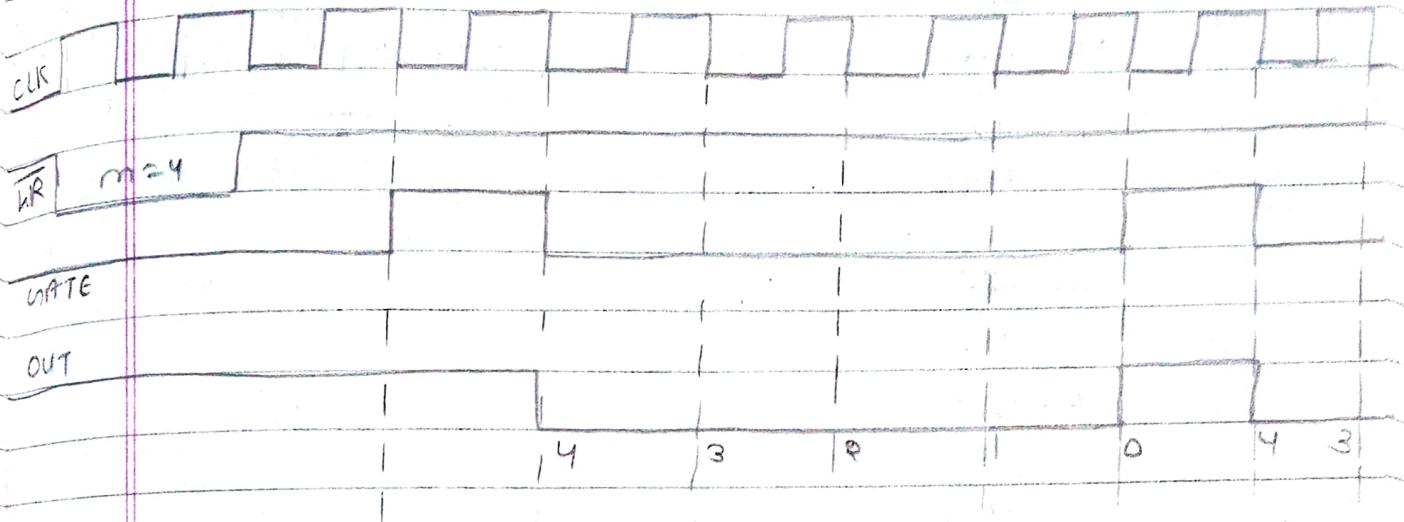
Gate (counter state count  
is start and off)

out

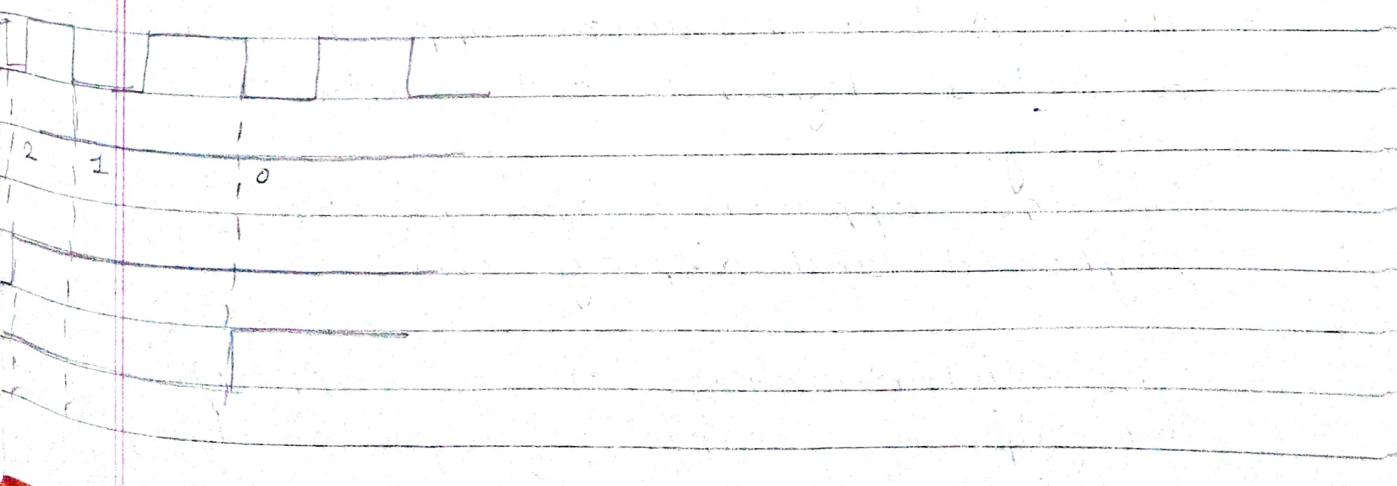
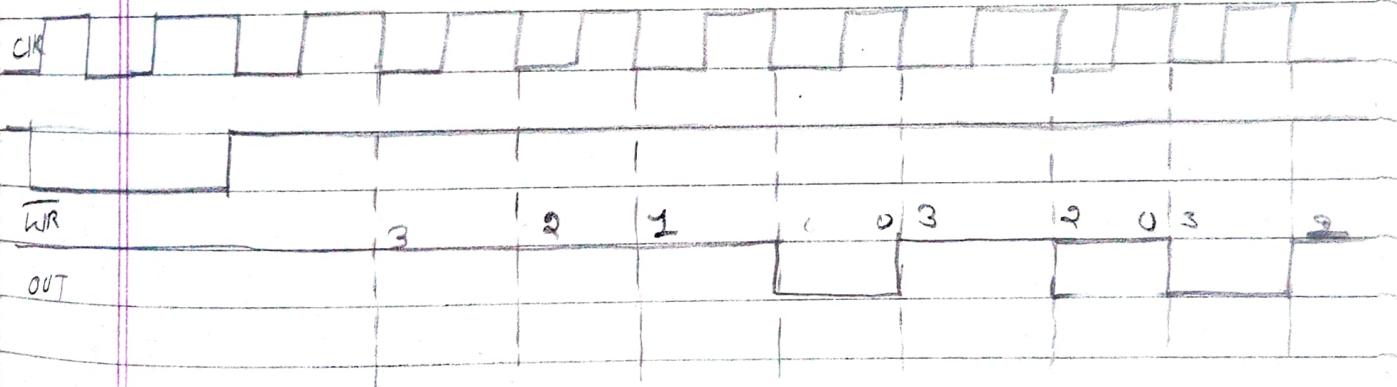
— Count is 0 the right.

2) Mode-1:-

(Hardware Retriggable one start).



3) mode-2:- (Rate Generators).



## # Keyboard display controllers (8279)

RL <sub>2</sub>	1	14	16
RL <sub>3</sub>	2	13	PL <sub>2</sub>
CLK	3	38	PL <sub>3</sub>
IRQ	4	37	DATA/CS
RL <sub>4</sub>	5	36	SIZZT
RL <sub>5</sub>	6	35	SL <sub>3</sub>
RL <sub>6</sub>	7	34	SL <sub>2</sub>
RL <sub>7</sub>	8	33	SL <sub>1</sub>
RESET	9	32	SL <sub>0</sub>
RD	10	31	OUT E <sub>3</sub>
WR	11	30	OUT E <sub>2</sub>
DB <sub>0</sub>	12	29	OUT E <sub>1</sub>
DB <sub>2</sub>	13	28	OUT E <sub>0</sub>
DB <sub>3</sub>	14	27	OUT F <sub>3</sub>
DB <sub>5</sub>	15	26	OUT F <sub>2</sub>
DB <sub>6</sub>	16	25	OUT F <sub>1</sub>
DB <sub>7</sub>	17	24	OUT F <sub>0</sub>
DB <sub>8</sub>	18	23	BD
DB <sub>9</sub>	19	22	CS
V <sub>SS</sub>	20	21	A <sub>3</sub>

fig:- Pin diagram of 8279

- The 8279 is a Hardware approach to interface a matrix keyboard and multiplexed display.  
Software approach is also possible to interface keyboard and display unit.
- The disadvantage of soft approach is that the MIP is occupied for a considerable

amount of time in checking the keyboard and refreshing the display.

The 8279 is 40 pin device with 9 major segments that are key and display.

The keyword segment can be connected to a 64 contact-key matrix, max 8 key entries can be stored in FIFO RAM.

The display segment can provide a 16 char scanned display interface with such devices as LED and LCD.

