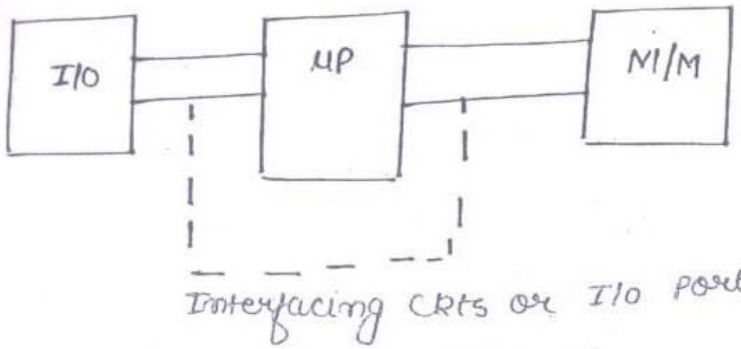
UNIT 4: 8085 MICROPROCESSOR INTERFACING

INTERFACING :-



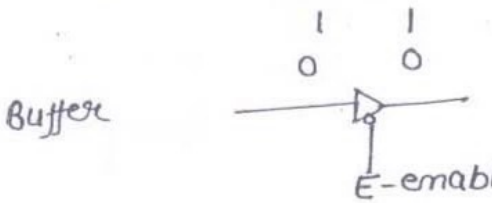
- Designing logic ckt & writing program to make the processor communicate with peripheral devices or memory is known as interfacing.
- The logic ckt used are known as interfacing ckt or I/O ports.

Basic Interfacing components

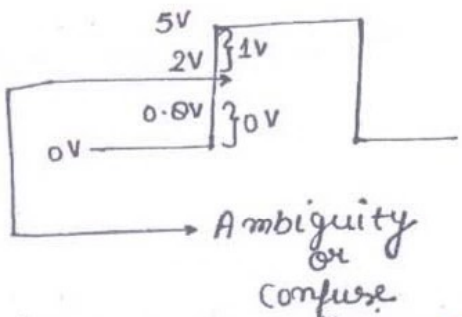
1→ Tri-state buffer
2→ Decoder
3→ Encoder
4→ Latch

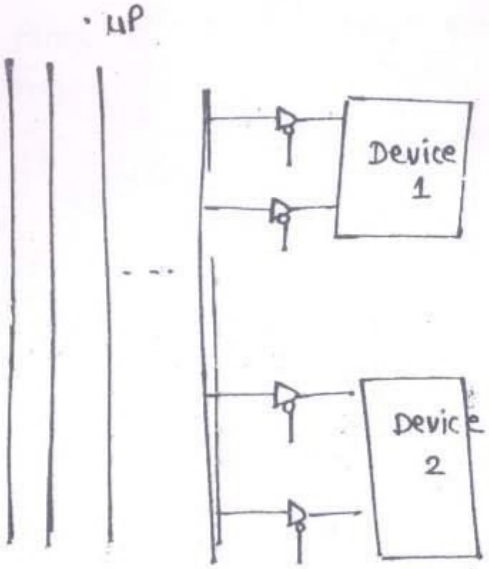
1→ Tri-State Buffer

- It is used to increase current or power handling capability of a bus when more no. of devices are connected to common bus.
- It has 3 states logic 0, logic 1 and high impedance state.



E=0 : Logic 0/1
E=1 : H.I.S
↓
'Z'



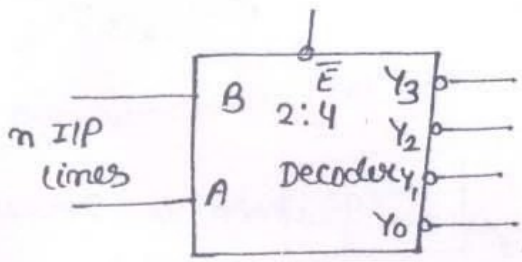


- When the enable line is active it may be in logic 0 or 1.
- If it is inactive it enters into high impedance state i.e the device connected to the bus would behave as it if is ~~for~~ it is disconnected from bus.

74LS244 → unidirectional buffer
74LS245 → Bidirectional buffer
. LS → low power Schottky.

NOTE
The line does not draw any current in high impedance state.

Decoder →

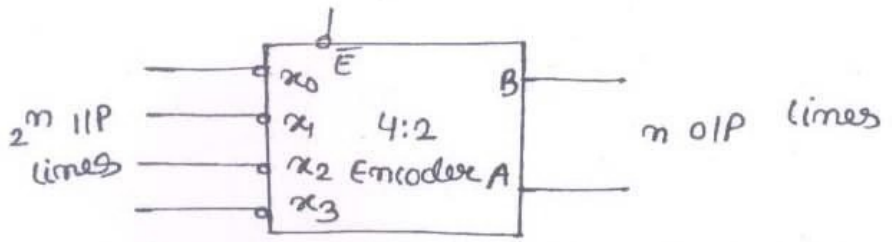


B	A	OIP
0	0	Y_0
0	1	Y_1
1	0	Y_2
1	1	Y_3

- It is a logic ckt which identifies the combination of IIP signals & selects one of the output. used for decoding logic of memories or I/O devices.

eg: 74LS138 → 3:8 Decoder

Encoder

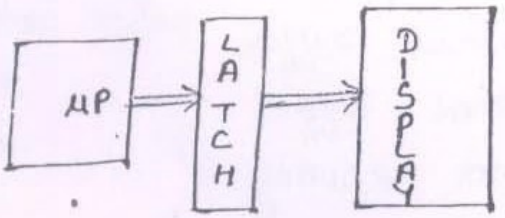


- It is a logic ckt which produces / generate code of one of the input signals at the O/P.

I/P	O/P B	A
x_0	0	0
x_1	0	1
x_2	1	0
x_3	1	1

eg: 74LS148 → 8:3 encoder

LATCH



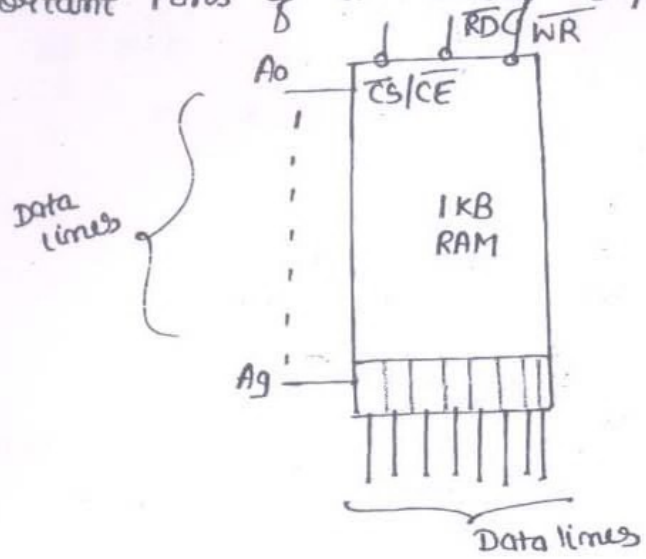
As the data is present on bus for few µs, latches are used to hold the data for sometime such that O/P devices like display unit may recognise the data

eg: 74LS373

Register Memory

- It is due to internal registers within a processor.
- More the no. of general purpose register more is the speed of processor and also cost.

Important Pins of a Memory chip :-



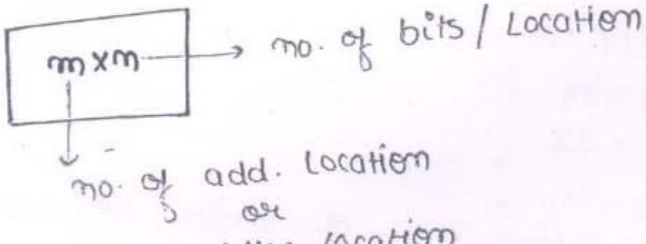
1) Address lines → depends on capacity of memory
2→ Data lines → depends on no. of bits per location
3→ CS/CE → chip select / Enable → To select the chip using decoding logic.
4→ $\overline{RD}$ / $\overline{WR}$ → Read/ write control signals → depend on type of M/A processor

$2^m = N$

m → no. of add. lines
N → no. of address / MIM location

2^{10} → 1KB → 1024 Byte
2^{20} → 1 MB
2^{30} → 1 GB
2^{40} → 1TB

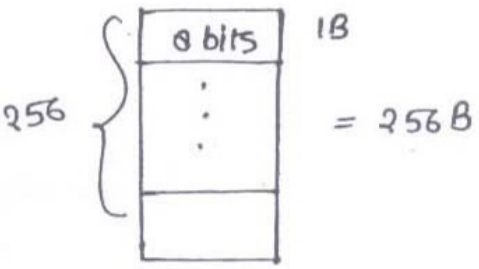
Memory Representation / Notation



$2^m = N = m$
$N = m$

eg: 256X8 RAM

m=256
n=8



TYPE 1→

Q→ Calculating address and data bus line

Find the length of address & data bus for a 256X8 RAM chip.

Ans→ 8 & 8

256X8

address line

$2^m = m$

$2^m = 2^8 = 256$

$m = 8$

A·B = 8

D·B = 8

Q→ 1024 X 1024

m = 1024

D·B = 1024

A·B = $2^m = 2^{10} = 1024$

$m = 10$

$m = 1024$

A·B = 10

Q → 16K X 32

$= 2^4 \times 2^{10}$

$= 2^{14}$

$n = 14$

AB = 14

DB = 32

TYPE 2

Q→ No. Calculating no. of chips required to design a memory

No. of chips required = $\frac{\text{M/M to be designed}}{\text{Available capacity}}$

Q→ Find no. of 256X8 RAM chip Required to design a memory of 8KB

8KB = 8×2^{10}

$= 2^3 \times 2^{10}$

AB m = 13

DB = 8

no. of chips = $\frac{8\,KB}{256 \times 8}$

1 KB = 1024 Byte

= 1024X8

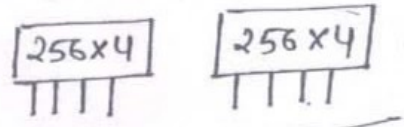
= $2^{10} \times 8$

$= \frac{8\,(1024 \times 8)}{2^8 \times 8} = 32$

2^{10} = 1KB

1KB = $2^8 \times 2$

Q→ To Design 256X8 MIM how many 256X4 chips are required.



Q→ Calculate no. of 1024X2 ic to design 1KB and 16KB memory.

1KB → 4

16KB → 16X4 → 64

Q→ Find out the length of data bus for a 1KB, 2KB & 4KB MIM chips if Length of add. bus is fixed to 10

1KB ⟶ 8 data lines

2KB ⟶ 16 data lines

4KB ⟶ 32 data lines

1KB = 1024X8

2KB = $2^{11} \times 8$

$= 2^{10} \times 2 \times 8$

= 16 data

4KB = $2^{12} \times 8$

$= 2^{10} \times 2^2 \times 8$

= 32 data lines

Interfacing Memory

$$n - x = Y$$

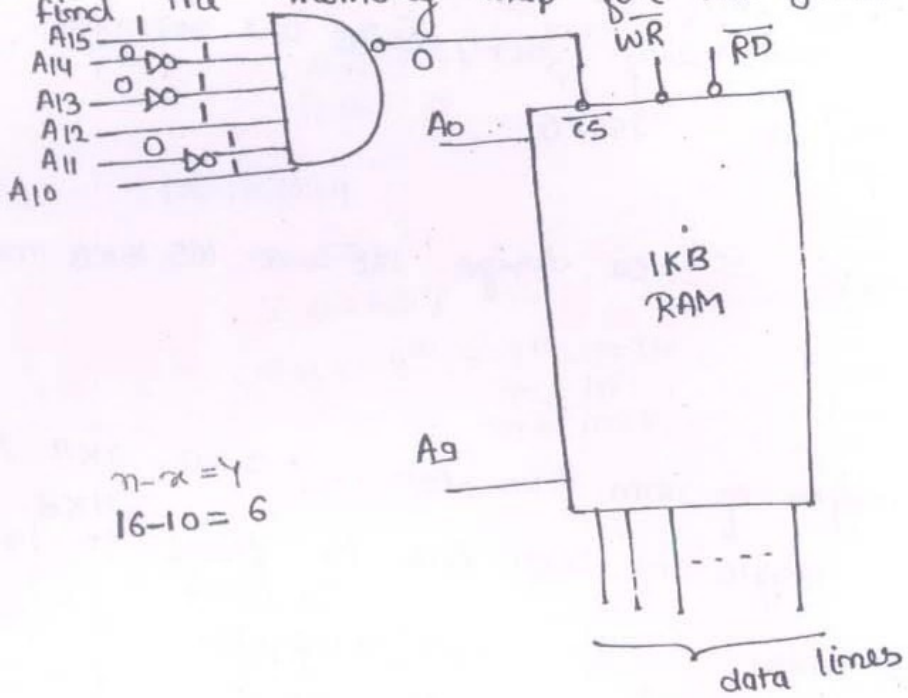
n = Total no. of address lines of µP
x = No. of lines required for m/m to be interfaced
Y ⇒ Address lines for decoding logic

Memory Mapping →

- Giving names or addressing memory locations is known as memory mapping.
- Memory map indicates starting and ending address of a memory chip.

TYPE 1

Q→ Find the memory map for the given interfacing Logic.



$n - x = Y$
$16 - 10 = 6$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

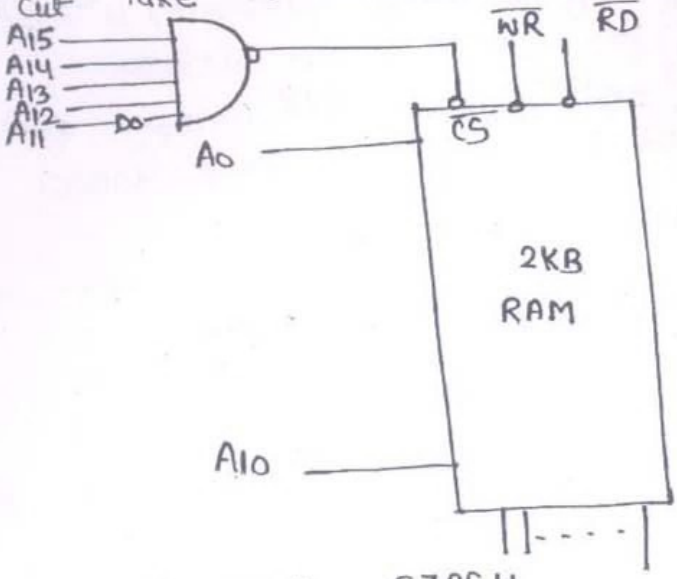
9400H

1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1

97FF

9400H – 97FFH

* Short cut Take 16 address as 4 nibbles



$n - x = Y$
$16 - 11 = 5$

F000H – F7FFH

TYPE 2 - Calculating starting and ending Addresses

Method

- Step 1 Find the no. of address line according to capacity of the memory.

Step 2 - Put equivalent no. of 1 as that of address line and obtain the Hex value that must be added or subtracted to get ending address or starting address.

eg → i → 1KB

$2^n = 1KB$

$= 2^{10}$

$n = 10$

1 1 1 1 1 1 1 1 1 1

3 F F

ii 2KB

$2^n = 2 \times 2^{10}$

$= 2^{11}$

$n = 1$

1 1 1 1 1 1 1 1 1 1 1

7 FF

Q → Find the ending address of a 2KB ROM if starting address is 6C5DH

$2KB = 2 \times 2^{10} = 2^{11}$

$n = 11$

1 1 1 1 1 1 1 1 1 1 1

7 FF

```
  1 1 1
  6C5D
+ 07FF
------
  745CH
```

```
  1 1 1
  6C5D
+ 07FF
------
  745CH
```

Q→ Find the starting address of a 8 KB RAM if ending address is D1B4H

$2^3 \times 2^{10}$

2^{13}

$n = 13$

1 1 1 1 1 1 1 1 1 1 1 1 1

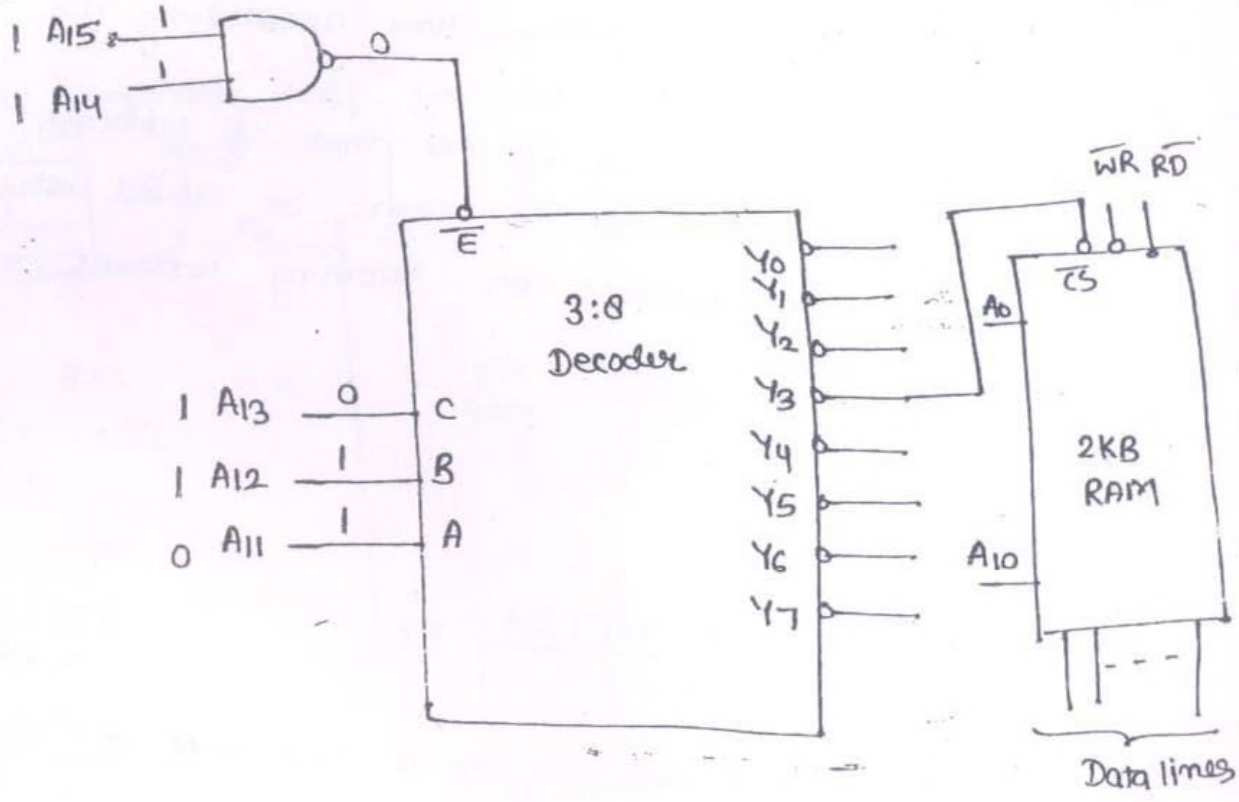
1 F F F

D1B4 − 1FFF = D5

CDBA4 − 1FFF = B1B5H

Ans → B1B5H

TYPE 3 → Q→



1101

D800H

DFFFH

Q→ If the CS is connected to Y_6 then find memory map

F000 − F7FFH

Design a memory of 8KB using 2048×8 RAM chip such that 2048×8 has memory capacity of 2KB so no. of chip required 8KB = 4 chip
C000H – DFFFH is satisfied.

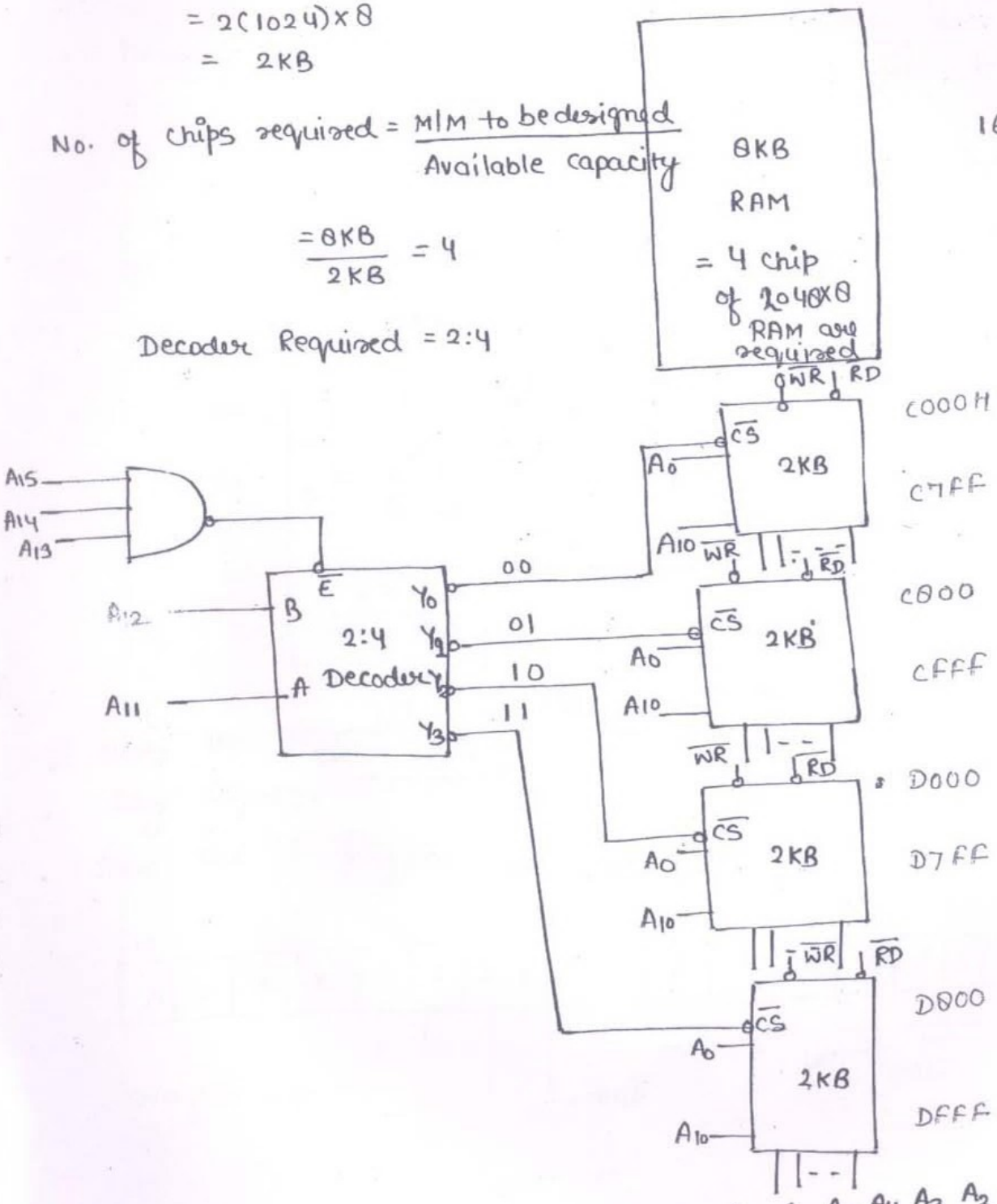
Given → 2048×8
= 2(1024)×8
= 2KB

No. of chips required = $\frac{\text{M/M to be designed}}{\text{Available capacity}}$

$= \frac{8KB}{2KB} = 4$

Decoder Required = 2:4

16 – 13 = 3



A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

C000H

1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

DFFFH

1 chip has starting add.

C000

and it is 2048x8 MIM chip so last add. is

$$\begin{array}{r} C000 \\ +\ 7FF \\ \hline C7FF \end{array}$$

2nd chip has starting ad.

$$\begin{array}{r} {}^{1}{}^{1} \\ C7FF \\ +1 \\ \hline C800 \end{array}$$

ending add.

$$\begin{array}{r} C800 \\ 7FF \\ \hline CFFF \end{array}$$

3rd chip has starting add.

$$\begin{array}{r} {}^{1}{}^{1} \\ CFFF \\ +1 \\ \hline D000 \end{array}$$

ending add.

$$\begin{array}{r} D000 \\ 7FF \\ \hline D7FF \end{array}$$

4rd chip has starting add.

$$\begin{array}{r} D7FF \\ +1 \\ \hline D800 \end{array}$$

ending add.

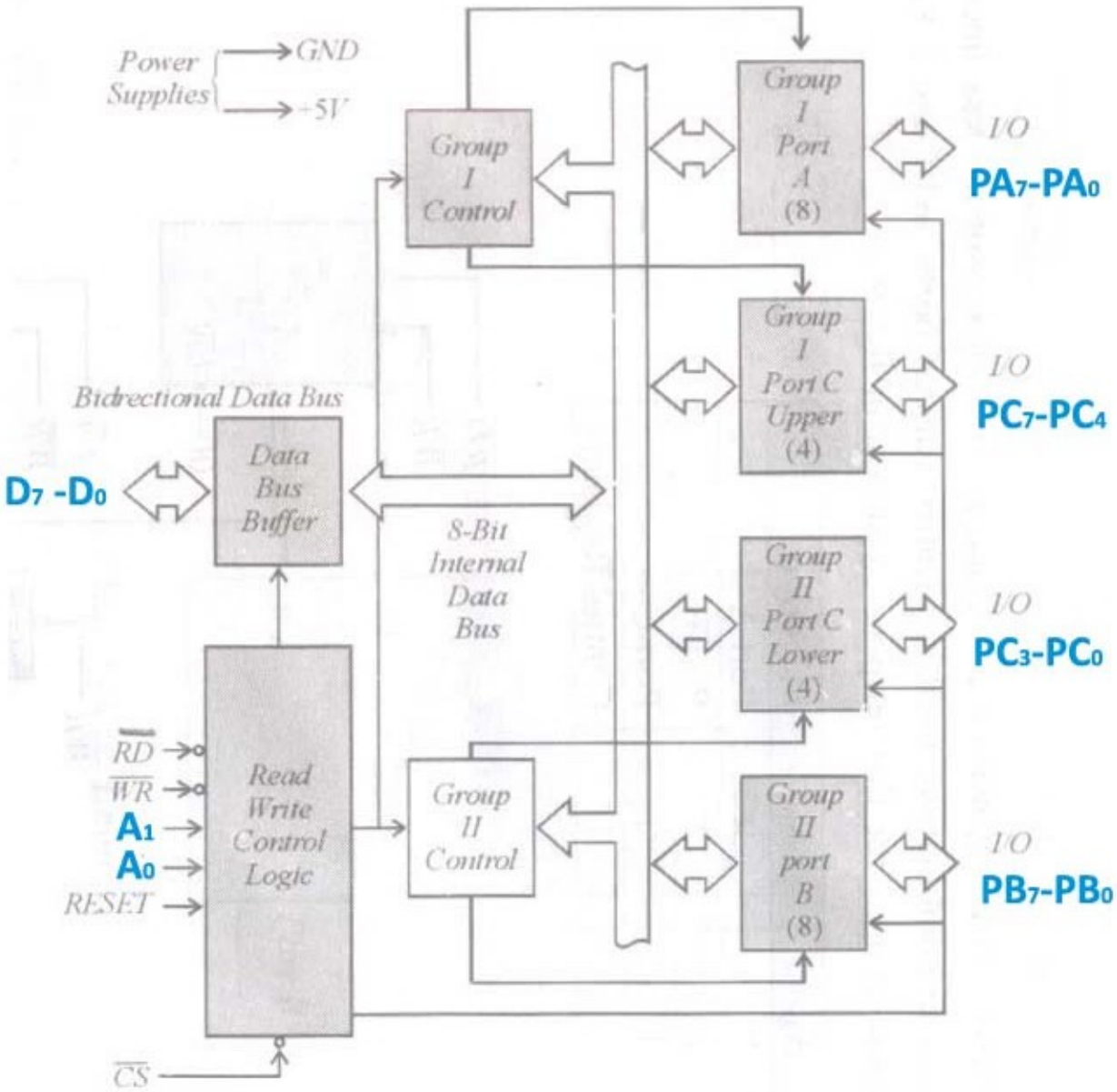
$$\begin{array}{r} D800 \\ 7FF \\ \hline DFFF \end{array}$$

Hence the range is satisfied.

PROGRAMMABLE PERIPHERAL INTERFACE (PPI) - 8255

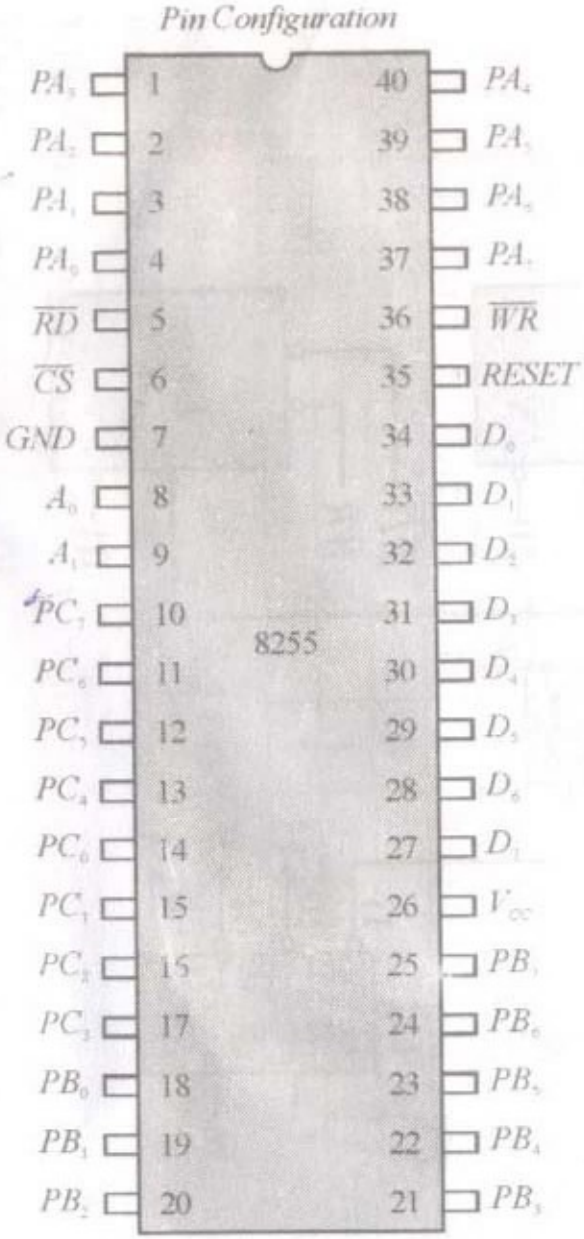
The 8255 is commonly used chip for Parallel Input/Output. It is an important general-purpose I/O device that can be used with almost any microprocessor. It can be programmed to function in various mode, such as simple I/O mode, I/O with handshake signals, Bidirectional I/O mode etc. by writing a Control Word into the internal Control Register.

The 8255 has three 8-bit ports namely, Port A, Port B and Port C. The port A and Port B are used as 8-bit parallel ports. The port C can be used as 8-bit parallel port or can be grouped in two 4-bit ports: Port C-upper (C_U) and Port C-lower (C_L), as shown in fig.



BLOCK DIAGRAM OF 8255

8255 PIN DIAGRAM



The 8255A chip has 40 pins. The pin diagram is shown in fig.

The functions of various pins and their signals are explained below:

PA_7-PA_0 – 8 pins for receiving/sending data from/to Port A.

PB_7-PB_0 – 8 pins for receiving/sending data from/to Port B.

PC_7-PC_0 – 8 pins for receiving/sending data from/to Port C.

D_7-D_0 – 8 pins to be connected to the Data Bus.

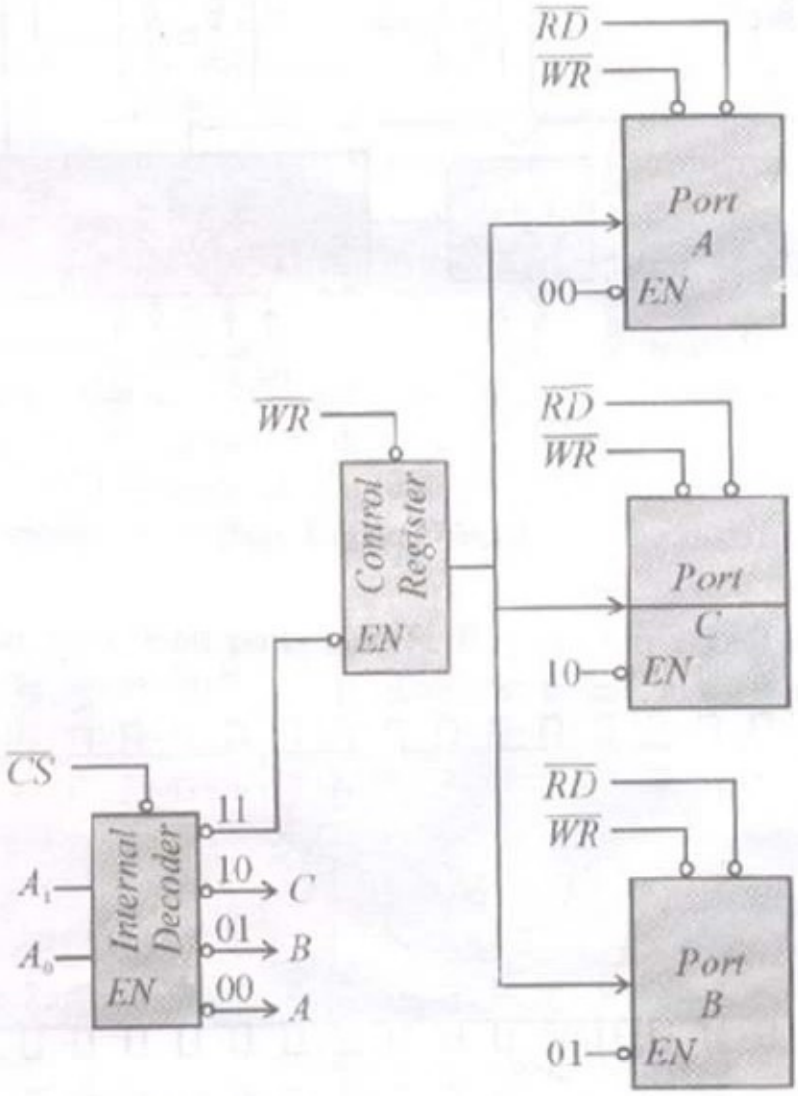
$\overline{RD}$ – It is an active low control signal, used for Read operation. When it is low (0), the microprocessor reads data from a selected I/O port of 8255A. It is connected to $\overline{IOR}$ / $\overline{MEMR}$ signals of the microprocessor.

$\overline{WR}$ - It is an active low control signal, used for Write operation. When it is low (0), the microprocessor sends (writes) data to a selected I/O port of 8255A. It is connected to $\overline{IOW}$ / $\overline{MEMW}$ signals of the microprocessor

RESET – It is an active high signal. When it is high (1), it clears the control register and sets all ports in the input mode.

A_0, A_1 – These pins are generally connected to microprocessor address lines - A_0 and A_1. These are, in combination, used to identify various ports and Control Register. An internal decoder is used for this purpose as shown in fig.

A_1	A_0	Selection
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Register



Control Logic Diagram of 8255

$\overline{CS}$ (Chip Select) – Address lines other than A_0 and A_1 may be used in any combination to make the Chip Select logic It is an active low signal. If it is low (0) the 8255 chip will be selected. The address of each port of the 8255 can be determined by $\overline{CS}$, A_0 and A_1 lines.

Vcc – It is connected to +5V.

GND – It is connected to 0V.

Control Register and Control Word

The 8255A chip has an internal register, called ***Control Register***. This register is used to store the ***Control Word***. The control word is used to define the functions and modes of various ports of 8255. Control Register can be used only for writing the control word and it cannot be used for read operation.

Various Modes of 8255

There are two basic modes: (i) BSR (Bit Set/Reset) Mode and (ii) Input/Output Mode

1. BSR (Bit Set/Reset) Mode

This mode is used to set/reset a single bit of Port C, without affecting the previously set mode of Port A and Port B. The D_7 bit of the control word must be 0 for this mode.

Control Word for BSR Mode

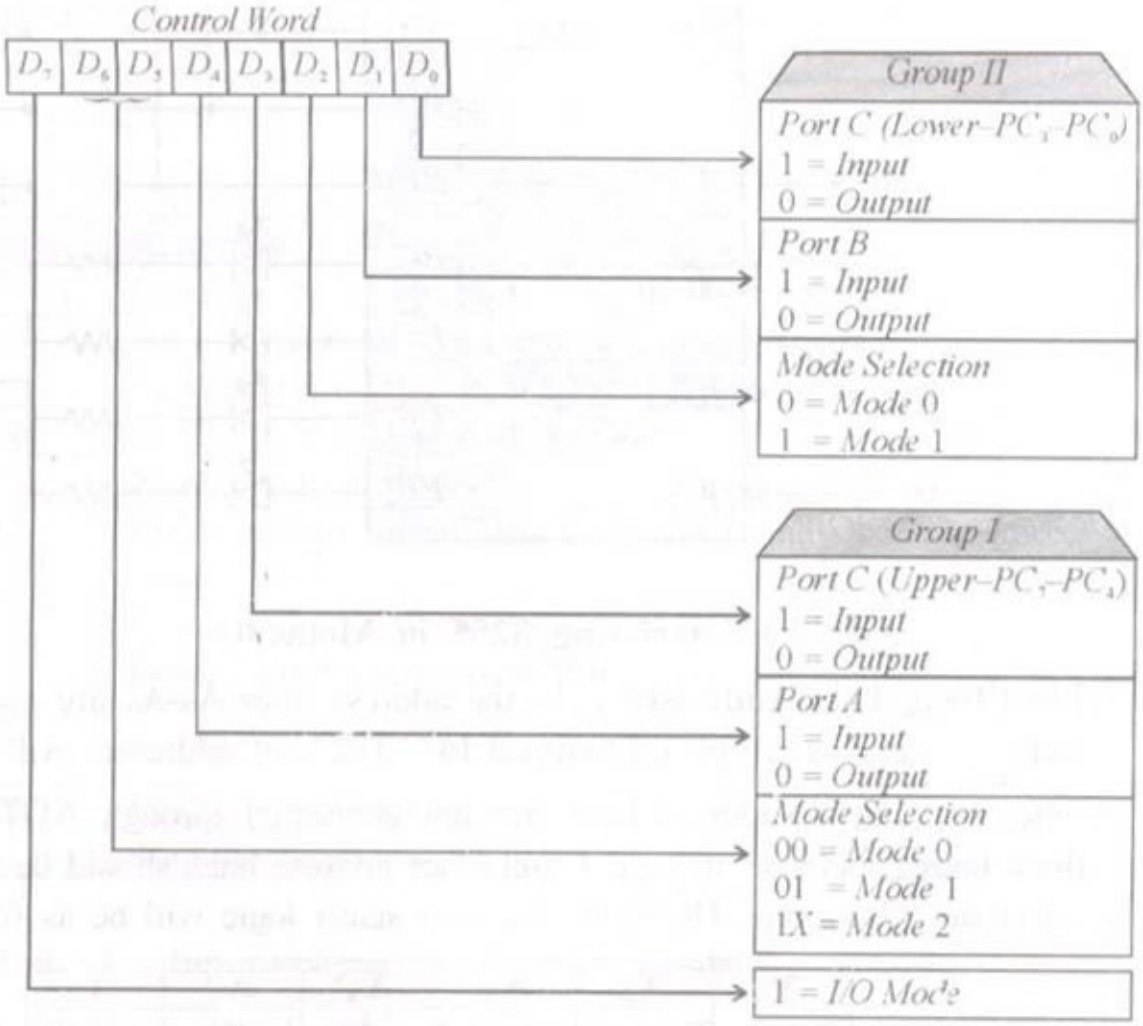
The control word format for this mode is shown if fig given below. When this control word is written in the control register, a single bit of Port C is set or reset at a time.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	X	X	X	Bit Select			S/R
Always 0	Undefined Generally Set to 0			000 – PC_0 001 – PC_1 010 – PC_2 011 – PC_3 100 – PC_4 101 – PC_5 110 – PC_6 111 – PC_7			1–Set 0–Reset

Control Word Format for BSR Mode

2. Input/Output Mode

The D_7 bit of the control word must be 1 for this mode. Three different types of I/O modes are available in 8255: (a) Mode 0-Simple I/O Mode, (b) Mode 1-I/O mode with handshake signals and (c) Mode 2-Bidirectional Mode. The Control Word Format for I/O mode is shown in fig. below:



Control Word Format for Input/Output Mode

Programmable Interval Timer (PIT) - 8253/8254

Both 8253 and 8254 are basically used to provide accurate time delay.
There are various software techniques of providing time delay. But the disadvantages of software techniques are that they are not accurate and microprocessor is busy in delay loop. These disadvantages are overcome by using additional hardware in the form of 8253/8254 chip.

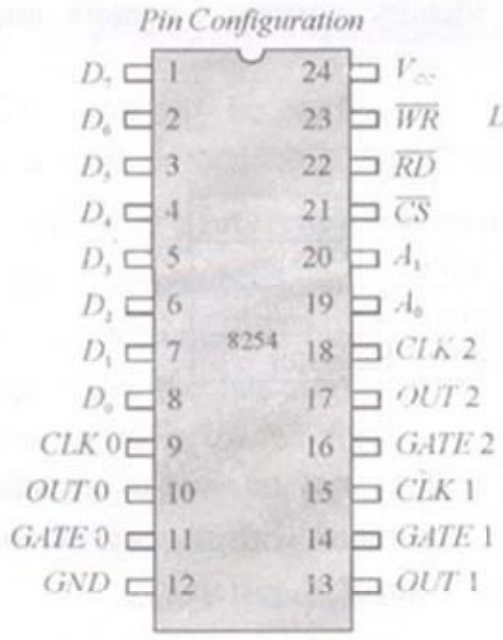
8253/8254 has three identical 16-bit counters named Counter 0, Counter 1, Counter 2 Each counter can operate independently in any one of the six modes.
Hence it can be used in various applications other then providing time delay, e.g., real time clock, an event counter, a digital one-shot, a square wave generator and a complex waveform generator.

8253 and 8254 are pin compatible, i.e., having same number of pins (24). They have almost same features except the following:

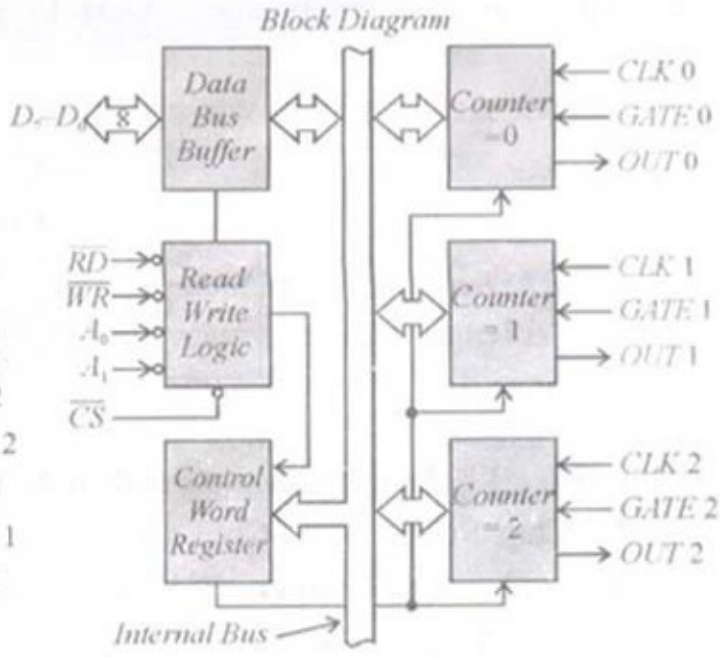
- The 8254 is an upgraded version of 8253. It can operate with higher frequency range (DC to 8 MHz and 10 MHz for 8254-2), while 8253 can operate with clock frequency range (DC to 2 MHz).
- The 8254 includes a status read-back command, which can latch the count and the status of the counters.

Pin Diagram of 8254

The 8254 chip has 24 pins. The pin diagram is shown in fig.



Pin Diagram of 8254



Block Diagram of 8254

PIN DESCRIPTION OF 8254 IC

The functions of various pins and their signals are explained below:

D_7–D_0 – 8 pins to be connected to the Data Bus.

CLK0, CLK1, CLK2 (Clock signal) – Input signals for Counter 0, Counter 1 and Counter 2, respectively. Normally on each clock cycle the contents of the respective counters are decremented to provide delay.

GATE0, GATE1, GATE2 (Gate signal) – Input signals for Counter 0, Counter 1 and Counter 2, respectively. GATE signal is normally use to start and stop the counting of the respective counter. When GATE signal is high, the counting starts and when it is low, the counting stops.

OUT0, OUT1, OUT2 (Output signal) – Output signals for Counter 0, Counter 1 and Counter 2, respectively. When the contents of a counter reach zero the OUT signal of that counter goes high. This signal can be used as an interrupt signal for microprocessor to activate any Interrupt Service Routine (ISR).

$\overline{RD}$ (Read) – It is an active low signal used to read the value of the counters. $\overline{IOR}$ signal is connected to this pin, for peripheral mapped I/O and $\overline{MEMR}$ signal is connected to this pin, for memory mapped I/O.

$\overline{WR}$ (Write) – It is an active low signal used to write command or data in counters or control register. $\overline{IOW}$ signal is connected to this pin, for peripheral mapped I/O and $\overline{MEMW}$ signal is connected to this pin, for memory mapped I/O.

A_0, A_1 – These pins are generally connected to microprocessor address lines - A_0 and A_1. These are, in combination, used to identify various Counters and Control Register.

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

$\overline{CS}$ (Chip Select) – Address lines other than A_0 and A_1 may be used in any combination to make the Chip Select logic. Chip select logic combined with A_0 and A_1 lines make the complete addresses of various Counters and Control Register.

Vcc – It is connected to +5V.

GND – It is connected to 0V.

Control Register and Control Word

Similar to 8255, 8253/8254 also has a Control Register, which is used to store the control word, to configure various options, as shown below:

- Define the counter as 8/16 bit counter.
- Select one out of six modes available, for each counter.
- Define the counter as Binary/BCD counter.

The control word format and bit definitions are shown in the fig. below .

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD
00 – Select Counter 0 01 – Select Counter 1 10 – Select Counter 2 11 – Read-Back Command (see fig. 9.23)		00 – Counter latch command (see example 9.4) 01 – R/W low-order 8-bits only (8- counter) 10 – R/W high-order 8-bits only (8- counter) 11 – R/W 16-bits (16-bit counter)		000 – Mode 0 001 – Mode 1 x10 – Mode 2 x11 – Mode 3 100 – Mode 4 101 – Mode 5			1–BCD Counter 0–Binary Counter

Control Word for 8253/8254 and Bit Definitions

Modes of Operation of 8253/5254

The 8253/8254 can be configured to operate in any one of the six modes available by writing a suitable control word. These modes are below:

1. **Mode 0 (Interrupt on Terminal Count)**
2. **Mode 1 (Hardware Retriggerable One-Shot)**
3. **Mode 2 (Rate Generator)**
4. **Mode 3 (Square-Wave Generator)**
5. **Mode 4 (Software Triggered Strobe)**
6. **Mode 5 (Hardware Triggered Strobe)**

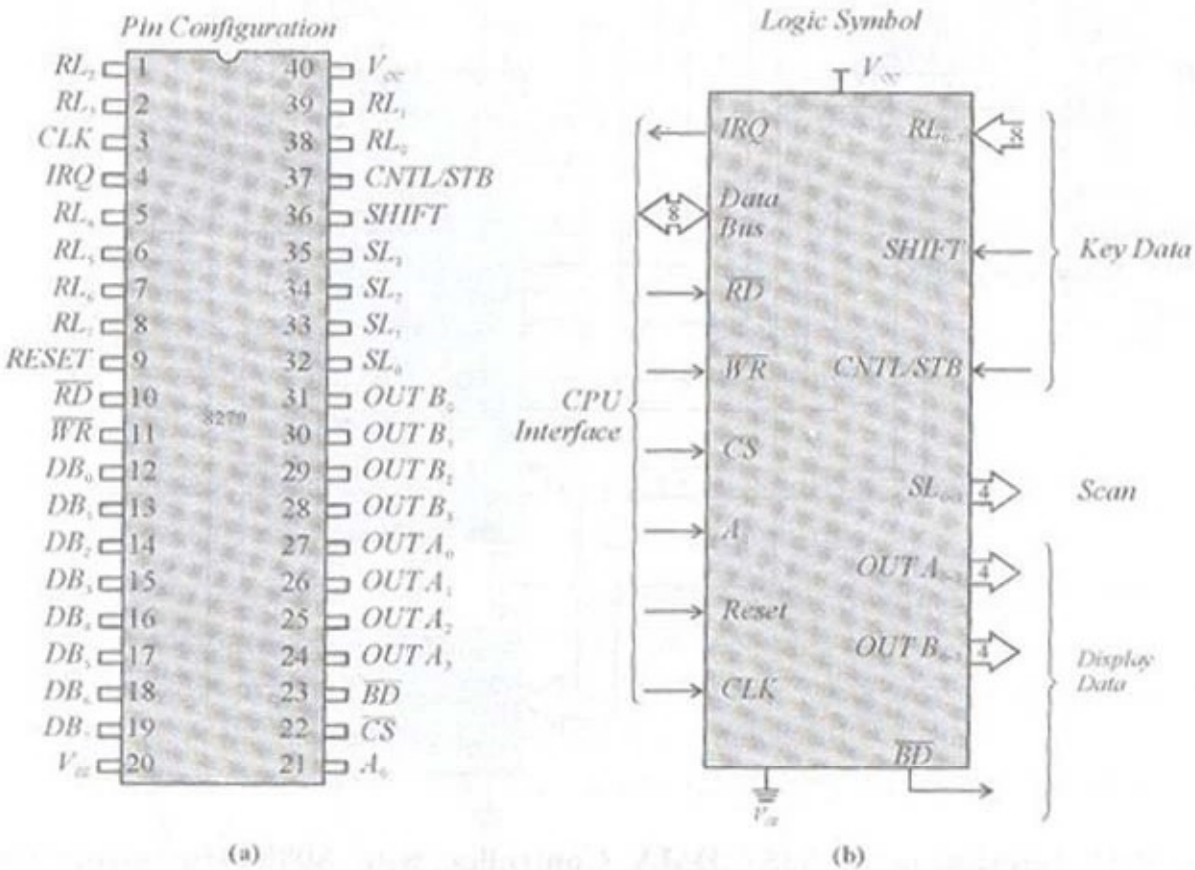
Keyboard/Display Controller – 8279

It is a general-purpose keyboard/display controller, which simultaneously controls the display of the system and interfaces a keyboard with the microprocessor. To interface with keyboard, it scans the keyboard to identify, if any key has been pressed and sends the code of the pressed key to the microprocessor. To interface with the display, it transmits the data received from the microprocessor to the display device. Software approach is also possible to interface keyboard and display unit. But, in software approach the microprocessor is busy for a considerable amount of time in checking the keyboard and refreshing the display. The 8279 is the hardware approach to do the same task, in which the microprocessor is free from this time consuming task.

The keyboard segment can interface an array of maximum 64 keys. Maximum 8 keyboard entries (codes) can be stored in the FIFO (First In First Out) RAM. Every time, a key is pressed, an interrupt signal is generated, to request the microprocessor to read the key code. The display section provides maximum of 16-character scanned display interface with LEDs. This segment contains 16-byte display RAM, which is used to read/write data for display.

Pin Diagram of 8279

The 8279 chip has 40-pins. The pin diagram of 8279 is shown in fig. below.



(a) Pin Diagram (b) Block Diagram of 8279

According to the functions, the 8279 can be divided into four major sections. block diagram of 8279, as shown in fig. These are: Keyboard section, Scan section, Display section and Processor section.

The functions of various pins and their signals are explained, section wise, below:

Keyboard Section

The functions of various pins of this section are explained below:

RL_7-RL_0 (Return Lines) - These lines are the input lines, which are connected to 8-columns of the keys.

SHIFT – The status of SHIFT key is stored along with key code in FIFO RAM. It is internally pulled up to keep it high, till it is pulled down with a key closure.

CNTL/STB (Control/Strobe) – In keyboard mode, this line is used as a control input and stored in FIFO RAM on a key closure. In strobed input mode, this line is strobe line, which enters the data into FIFO RAM. It also has an internal pull up. It is pulled down with a key closure.

Keyboard section also has its internal 8 x 8 FIFO RAM. i.e., it has 8 registers of 8-bits each. The IRQ signal is generated, when the FIFO is not empty.

Keyboard Modes : 8279 provides three keyboard (input) modes:

1. Scanned Keyboard Mode

In this mode matrix key can be interfaced using either encoded (8 x 8 keyboard) or decoded (4 x 8 keyboard) scans. This mode possition of depressed key (Row number and column number) along with status of CNTL and SHIFT keys are entered into FIFO RAM location.

(a) **Two-key Lockout** In this mode, if two keys are pressed simultaneously, then no key is recognised till one of them remains closed and other is released. Then the pressed key is recognised.

(b) **N-key Rollover**: In this mode simultaneously pressed keys are recognised.

(c) **Special Error Mode**: This mode is valid only under N-key rollover mode. In this mode, if two keys are found pressed an error flag is set, which prevents further writing in FIFO RAM.

2. Sensor Matrix Mode

In this mode *sensor* array can be interfaced with 8279 using either encoded or decoded scans. In this mode, the data on the return lines (**RL_7- RL_0**) is entered directly into the correspoiding location of sensor RAM. THe location of sensor RAM is specified by scan counter (row number of sensor matrix). Therefore each sensor switch position can be scanned by the CPU. The SHIFT and CNTL inputs are ignored.

3. Strobed Mode

In this mode, if the control line goes low, the data on return lines (RL_7- RL_0), is stored in the FIFO, byte by byte at the rising edge of STB pulse.

Scan Section

The functions of various pins of this section are explained below:

SL_3- SL_0 (Scan Lines) – These lines are used to scan the keyboard matrix and display digits.

These four scan lines are used as the input for 4-to-16 decoder to generate 16 output lines for scanning. These lines can be connected to the rows of a matrix keyboard and the digit drivers of a multiplexed display.

Display Section

The functions of various pins of this section are explained below:

OUT A_3- OUT A_0 and OUT B_3- OUT B_0 (Output Lines) – these 8 output lines are divided in two groups. These lines can be used either as a group of eight lines or two groups of four lines. These lines, in combination with 4 scan lines, used for a multiplexed display.

$\overline{BD}$ (Blank Display) – It is an active low output lines, used to blank the display.

Display (output) modes: The 8279 provides two display modes:

(i) **Display Scan Mode:** In this mode 8279 provides 8 or 16 character multiplexed display, which can be organised as dual 4-bit or single 8-bit display units.

(ii) **Display Entry Mode(right entry or left entry mode):** In this mode, 8279 allows to display data to be entered either from right side or left side.

Processor Section

The functions of various pins of this section are explained below:

DB_7- DB_0 - These are bidirectional data bus lines.

IRQ – It is an active high interrupt output line. It goes high when there is data in FIFO RAM. It goes low when FIFO is empty.

A_0 – Connected to A0 line of the address bus. It should be high while writing the command or reading status and low when transferring data.

$\overline{CS}$ (Chip Select), **$\overline{RD}$** (Read signal), **$\overline{WR}$** (Write signal) have their usual functions.

RESET – A high signal on this pin resets the 8279.

CLK - Clock input.