VLSI LAB – EC372

IMPLEMENTATION OF FINITE IMPULSE RESPONSE FILTER USING MAGIC VLSI LAYOUT TOOL

Brief Report

Submitted by:
Mohita Chowdhury (15EC226)
N. Subbalakshmi (15EC228)

Submitted to:
Dr. Ramesh Kini
Associate Professor
Dept. of E&C, NITK Surathkal

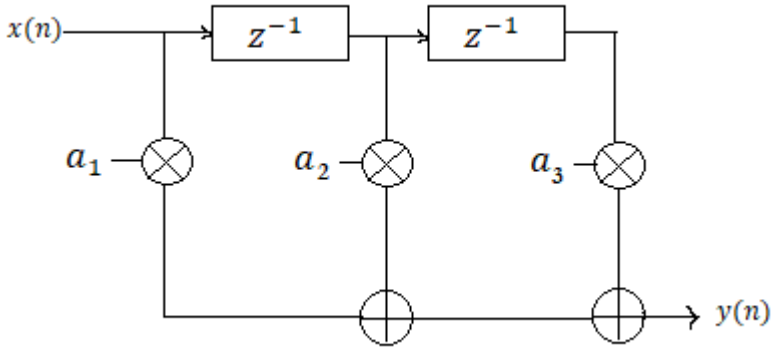
Introduction

This project deals with the implementation of a 3-tap Finite Impulse Response (FIR) Filter for integral input sequences of length 3 bits. An FIR filter implementation consists of adders, multipliers and delay elements. We will be dealing with unsigned adder and multiplier blocks. We will get the filter coefficients from MATLAB and feed them as one of the inputs to the multiplier block.

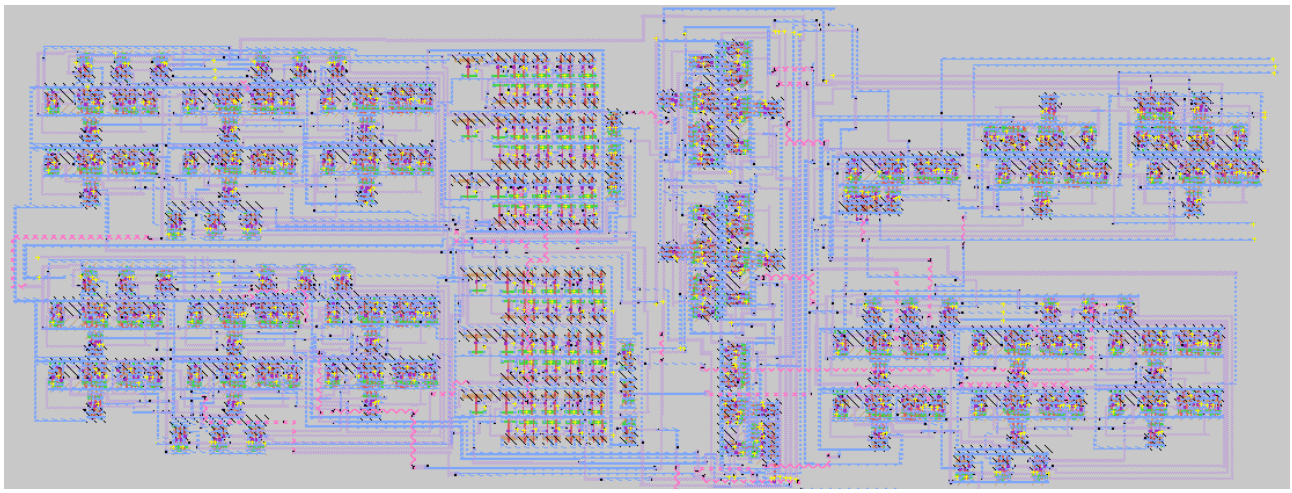
Say, our response is

$$y(n) = a1.\ x(n) + a2.\ x(n-1) + a3.\ x(n-2)$$

Here, the coefficients a1, a2, a3 can be generated from MATLAB or given directly.



Layout



Features of the Design

Metrics	Value
Capacitance	168.122879 pF
Power	2.1 nW
Area	3455136 λ^2

No. of Transistors	N-channel=1520, p-channel=1410
Maximum Operation Frequency	2.27 Mhz

To check the output in IRSIM

```
h vdd
l vss
vector Q q2_M1 q1_M1 q0_M1
vector B1 b2_M2 b1_M2 b0_M2
vector B0 b2_M1 b1_M1 b0_M1
setvector Q 110
setvector B0 101
setvector B1 011
vector D1 q2_M2 q1_M2 q0_M2
vector D1 q2_M2 q1_M2 q0_M2
vector AM2 b5_A1 b4_A1 b3_A1 b2_A1 b1_A1 b_A1
vector AM1 a5_A1 a4_A1 a3_A1 a2_A1 a1_A1 a_A1
vector S c5_A1 s6_A1 s5_A1 s4_A1 s3_A1 s1_A1 so_A1
vector AM3 a5_M3 a4_M3 a3_M3 a2_M3 a1_M3 a0_M3
vector B2 b2_M3 b1_M3 b0_M3
vector D2 q2_M3 q1_M3 q0_M3
vector S2 s8_A2 s7_A2 s6_A2 s5_A2 s4_A2 s3_A2 s1_A2 so_A2
setvector B2 011
clock en 1 0
step 200
w D1 D2 AM1 AM2 AM3 S S2
```