Power management and Sleep modes

- Sleep modes enable the application to shut down unused modules in the MCU
- Hence useful for saving Power .
- AVR Provides six sleep modes.

MCU Control Register– MCUCR

•To enter any of the six sleep modes, the SE bit in MCUCR must be written to logic one after that .

•SLEEP instruction must be executed

•MODES:

- Idle
- ADC Noise Reduction
- Power-down
- Power-save
- Standby
- Extended Standby

7	6	5	4	3	2	1	0	
SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

cont...

7	6	5	4	3	2	1	0	
SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

Table 13. Sleep Mode Select

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Standby(1)

Idle Mode

- SM2..0 bits are written to 000
- Stop the CPU
- SPI, USART, Analog Comparator, ADC, Two-wire Serial Interface, Timer/Counters, Watchdog, and the interrupt system to continue operating.
- This sleep mode basically halts clkCPU and clkFLASH, while allowing the other clocks to run.
- Wakes up : external triggered interrupts as well as internal ones

ADC Noise Reduction Mode

- SM2..0 bits are written to 001
- Stop the CPU
- ADC, External Interrupts, Two-wire Serial Interface address watch, Timer/Counter0 and the Watchdog continue to work operating (if enabled).
- This sleep mode basically halts clkI/O, clkCPU, and clkFLASH, while allowing the other clocks to run.
-

Power-down Mode

•SM2..0 bits are written to 010

•External Oscillator is stopped

•External Interrupts, the Two-wire Serial Interface address watch, and the Watchdog continue operating (if enabled).

- Only an External Reset, a Watchdog Reset, a Brown-out Reset, a Two-wire Serial Interface address match interrupt, an External Level Interrupt on INT7:4, or an External Interrupt on INT3:0 can wake up the MCU

	Active Clock Domains					Oscillators		Wake-up Sources					
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Osc. Enabled	INT1 INT0	TWI Address Match	Timer 2	SPM/ EEPROM Ready	ADC	Other I/O
Idle			X	X	X	X	X(2)	X	X	X	X	X	X
ADC Noise Reduction				X	X	X	X(2)	X(3)	X	X	X	X	
Power Down								X(3)	X				
Power Save					X(2)		X(2)	X(3)	X	X(2)			
Standby(1)						X		X(3)	X				

Notes:
1. External Crystal or resonator selected as clock source.
2. If AS2 bit in ASSR is set.
3. Only level interrupt INT1 and INT0.

Refer Page number 33 – 35 of data sheet