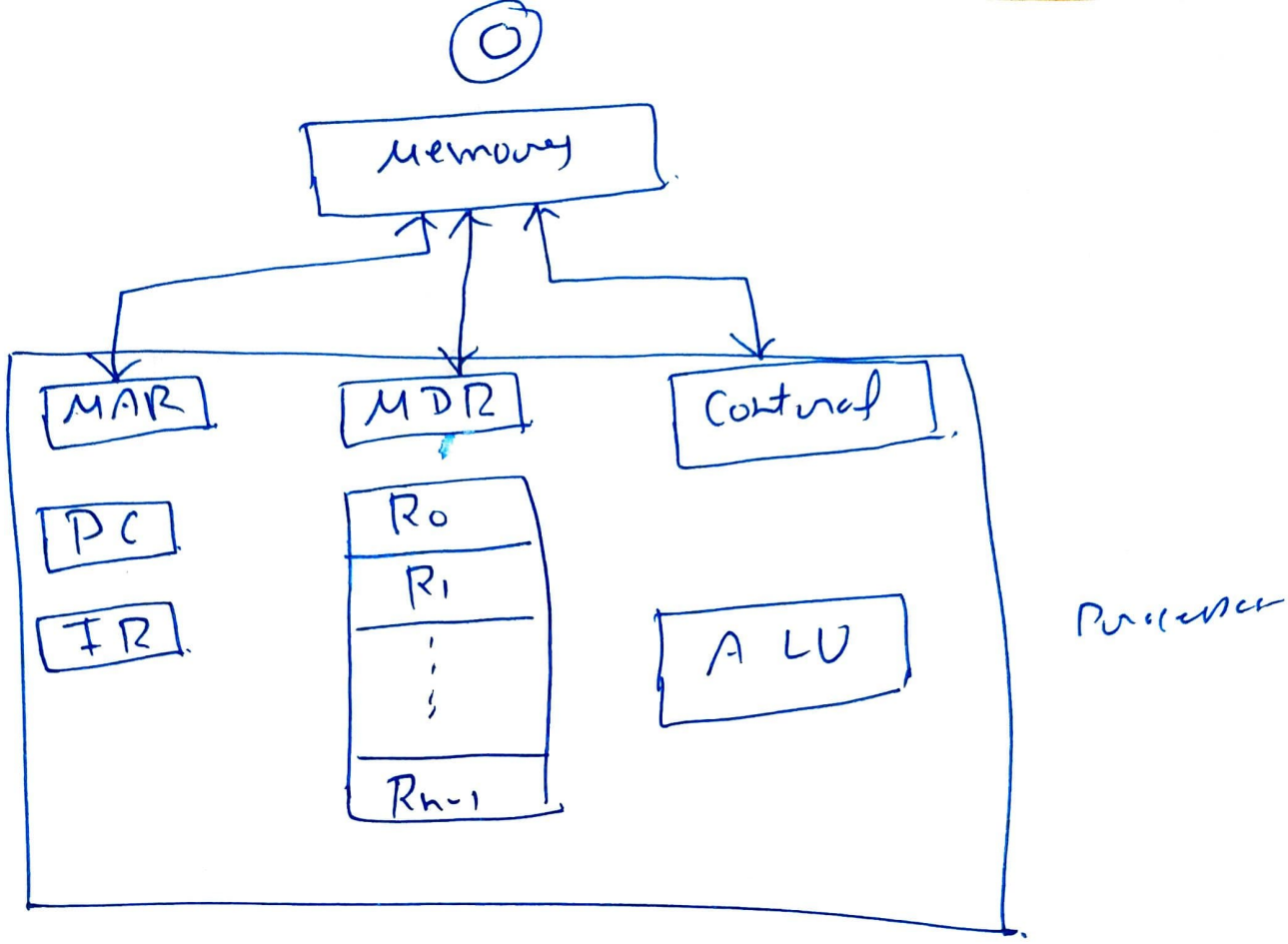
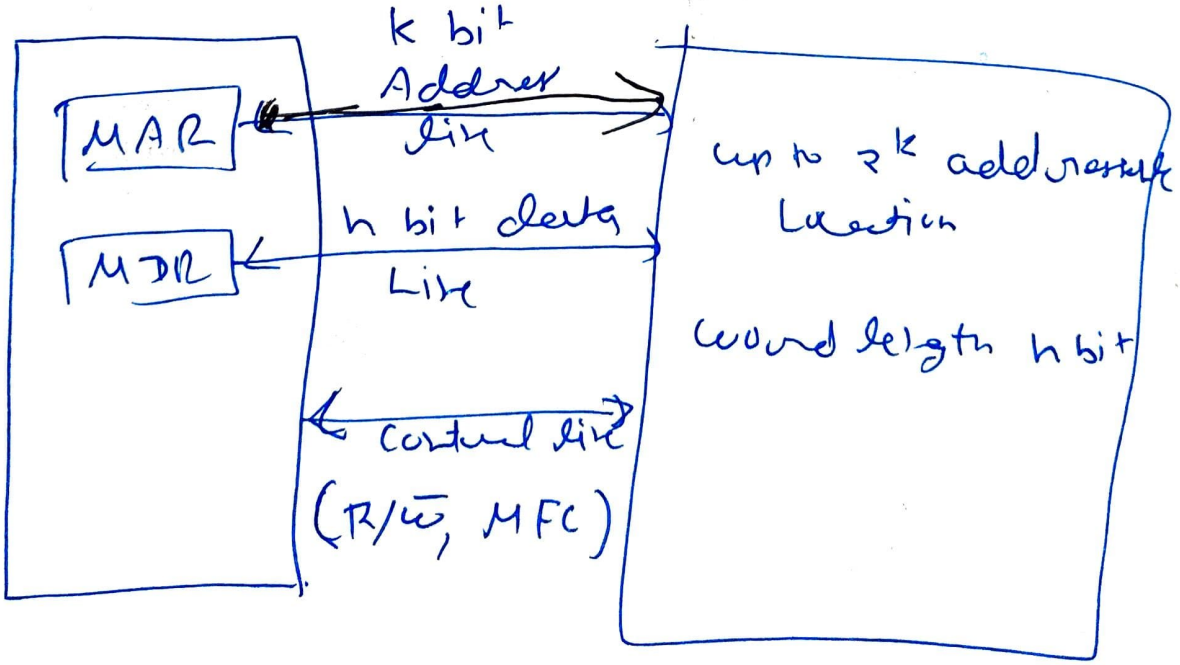


Connection between processor & Memory

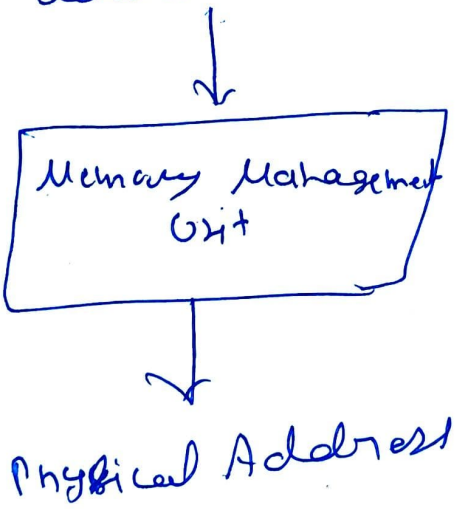


→ The time between the read and MFC signal is referred to as a Memory access time.

→ Memory cycle time is minimum time delay required between the initiation of two successive memory operation.

→ A memory unit is called random-access memory if any location can be accessed in fixed amount of time.

→ virtual address or logical address



Memory

→ Suppose you have to write a term paper on computer H/w development.

→ You are sitting on a desk library with a collection of books that you pulled from the shelves and are examining.

→ Now you found many thing about the computer H/w but EDSAC is not available.

→ So you go back to library shelves to get some more books which have EDSAC.

good selection of books on

→ Once you have ~~all the relevent information~~ the desk in front of you, there is a good probability that many of the topic you need can be found in them and most of the time you just using books which are available on the desk.

→ Having several books on the desk in front of you saves time compared to having only one book there and constantly having to go back to the shelves to return it and take out other.

→ Same principle allow us to create the illusion of a large memory that we can access as fast as a very small memory.

→ Just as we did not need to access all the books in the library at once with equal probability.

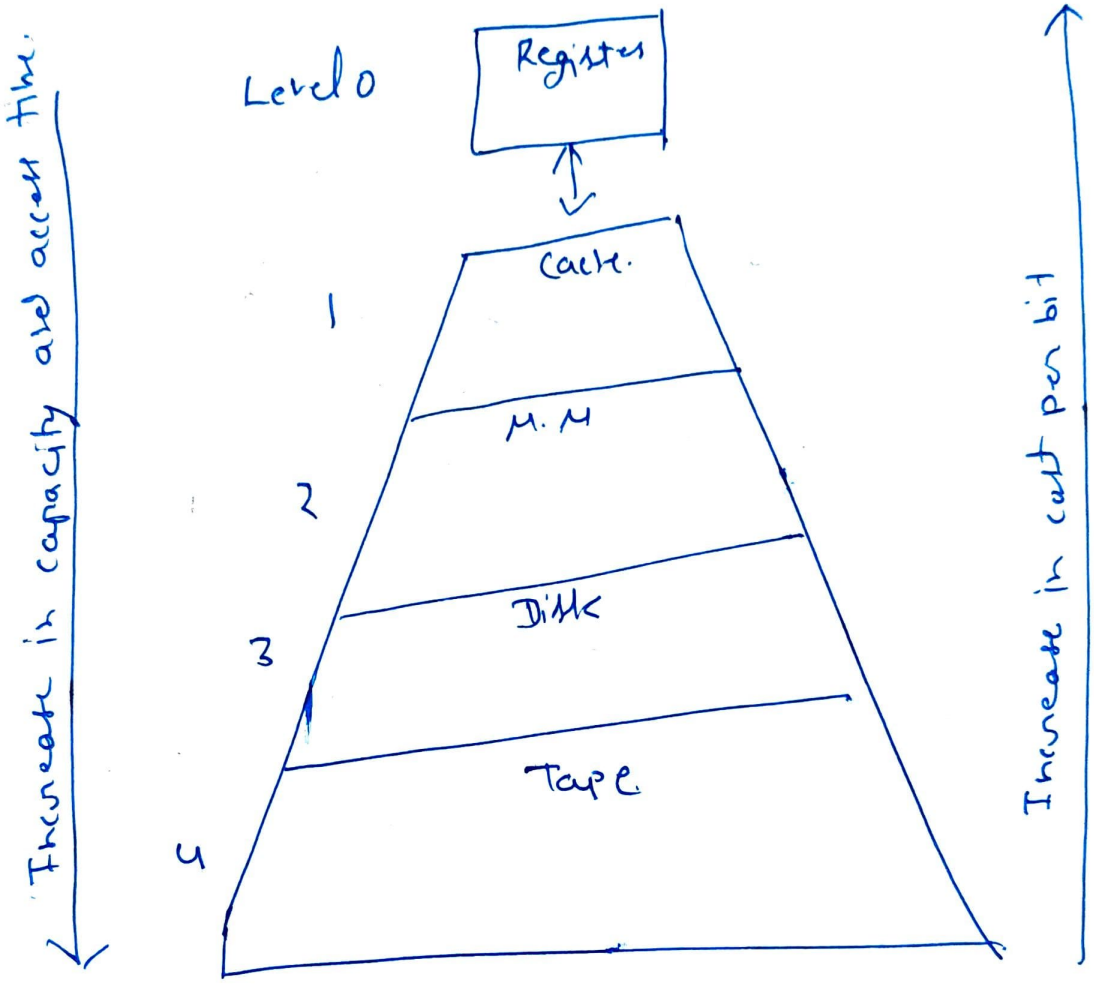
→ In same manner, a program does not access all of its code or data at once with equal probability.

→ otherwise' it would be impossible to make most memory accesses fast and still have large memory in computer, Just as it would be impossible for you to fit all the library books on your desk and still find what you wanted quickly.

→ It shows "principle of locality". It states that programs access a relatively small portion of their address space at any instants of time, ~~fast~~ Just as you only accessed a small portion of the library's collection.

Memory Hierarchy (1)

Register, cache, Main Memory, disk device, and tape Units are organized as a hierarchy



There are some parameters:

Access time (t_i) :- Round-trip time CPU to the ith ith level

Memory size (S_i) :- # of bytes or word in level i

cost per byte (C_i) :- The cost of the ith level is estimated by the ~~S_i~~ $C_i \cdot S_i$

Transfer Bandwidth (b_i) :- Rate at which information is transferred between adjacent level

(2) (Memory Hierachy)

Unit of transfer (x_i) :- Refer to the grain size of data transfer between level i and i+1.

In Memory Hierachy

$f_{i-1} < f_i$

$s_{i-1} < s_i$

$c_{i-1} > c_i$

$b_{i-1} > b_i$

$x_{i-1} < x_i$, (for $i = 1, 2, 3, 4$)

IRC

Inclusion, Coherence, and Locality

Inclusion :- The inclusion property is stated as

$$M_1 \subset M_2 \subset M_3 \subset \cdots \subset M_n$$