③ (Inclusion, C & L)

Locality of Reference :- It is a program behavior which develop memory hierachy.

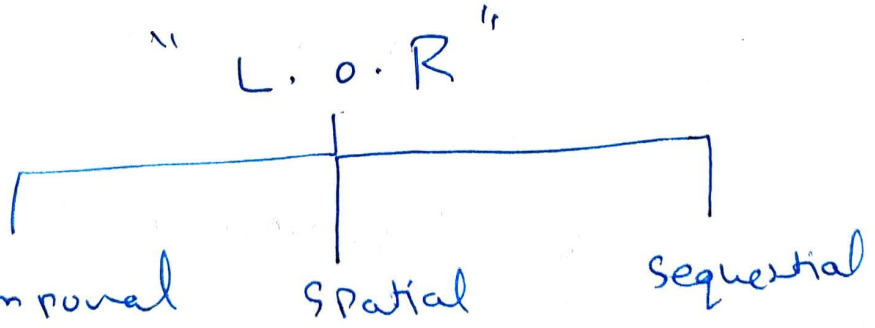
→ Memory references are generated by the CPU for either instruction or data accest.

→ These accessed tend to be clustered in certain regions in time, space, and ordering.

→ Most programs act in favar of certain portion of their address space at any time window.

→ Hennessy & Patterson pointed out a 90-10 rule. Means that a typical program may spend 90% of its execution time on only 10% of the code.

→



4- (Inclusion, CSL)

Temporal :- Recently referenced items are likely to be referenced again in the near future. It often caused by special programming constructs

- Loop
- Process stack
- temporal variable
- Subroutines

Spatial :- The tendency for a process to access items whose addresses are near one another.

- Operations on tables or array involve accesses of a certain clustered ~~or~~ area in address space
- Sequential and Macros

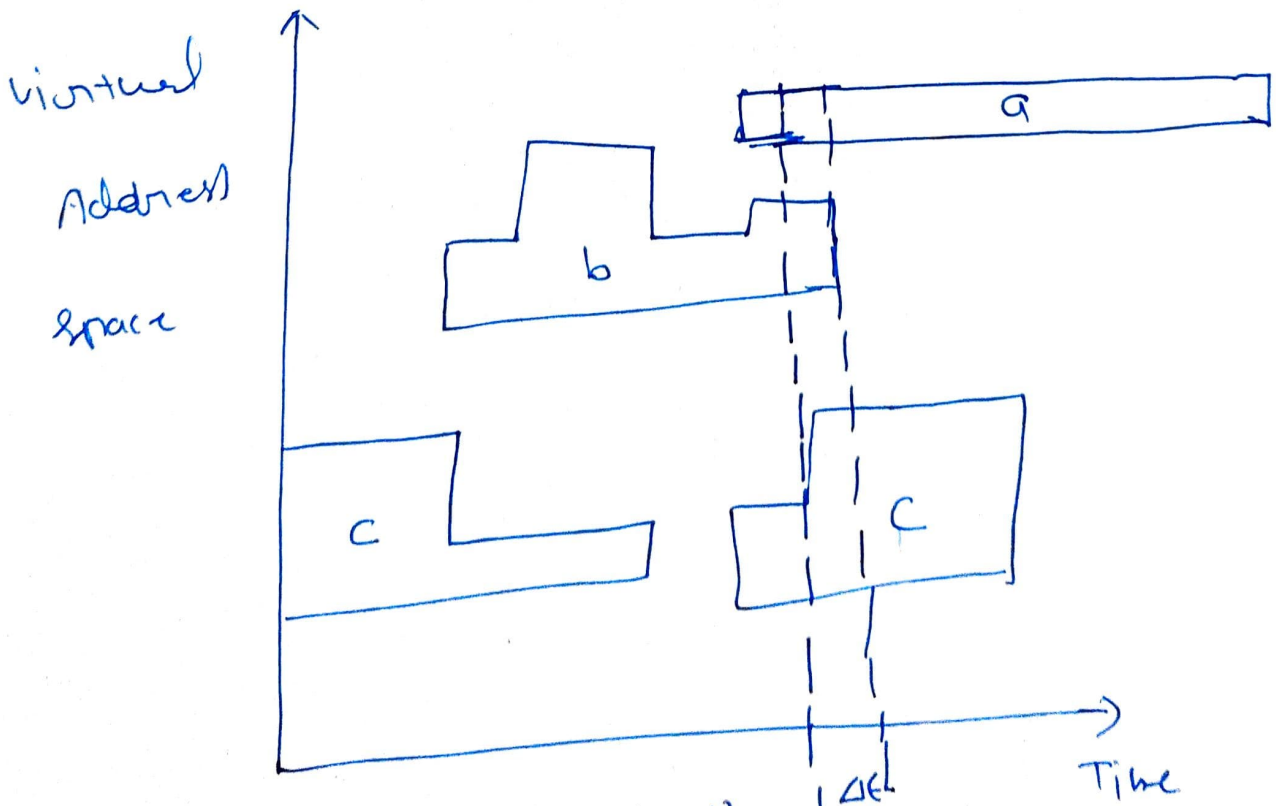
Sequential :- In typical programs, the execution follow a sequential order unless branch instructions created out-of-order execution

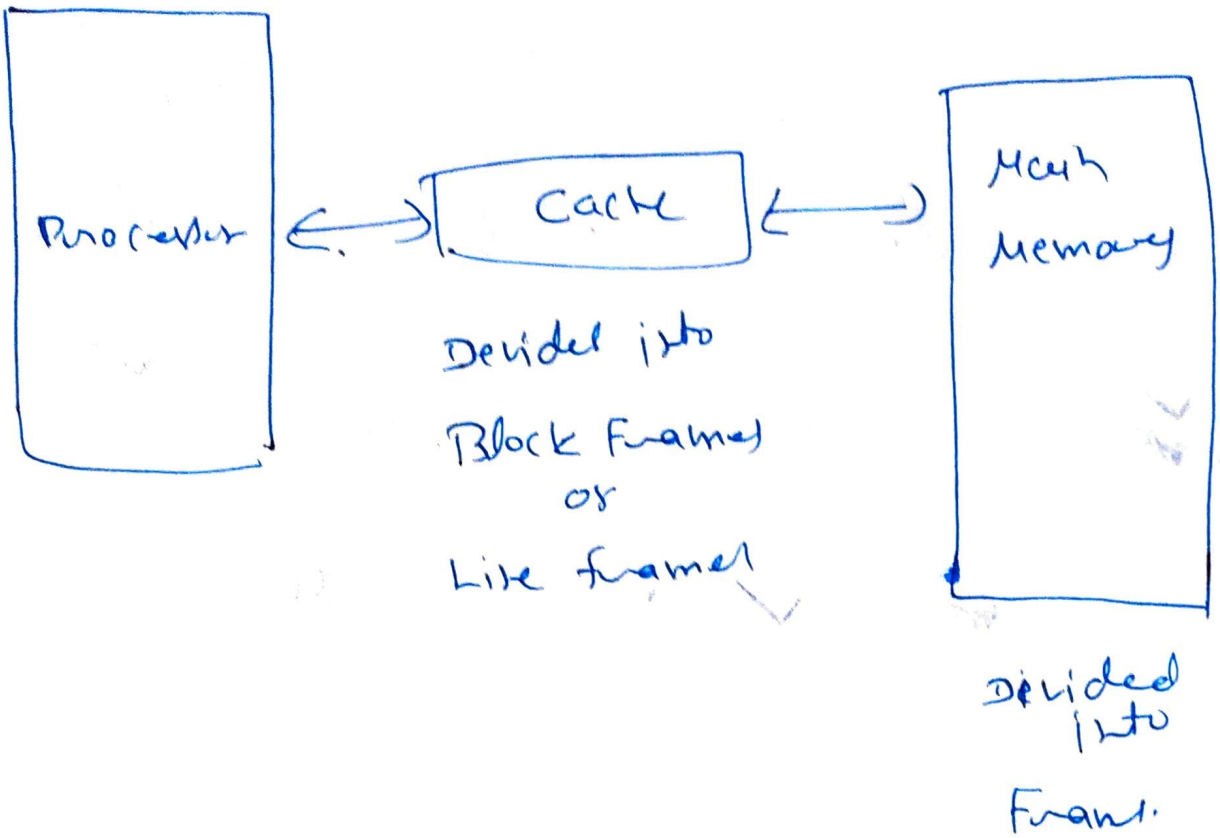
5 (Inclusion, C & L)

→ Sequentiality in program behavior also contributes to the spatial locality. Instruction (sequentially coded) and array elements are often stored in adjacent locations.

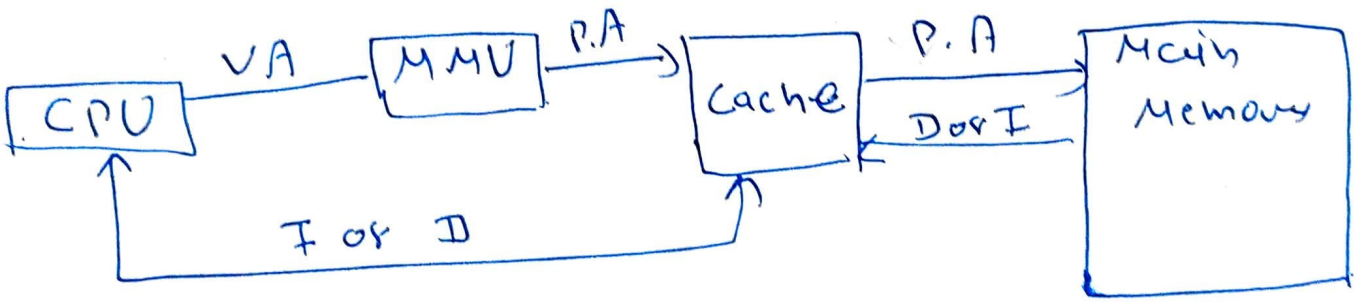
→ Each type of locality affects the design of Memory hierarchy.

→ Prefetch techniques are heavily affected by the locality properties.

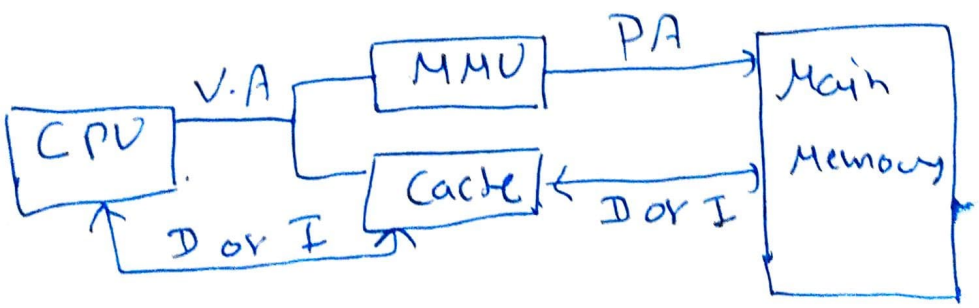




Physical Address Cache :- When a cache is accessed with a physical memory addressed

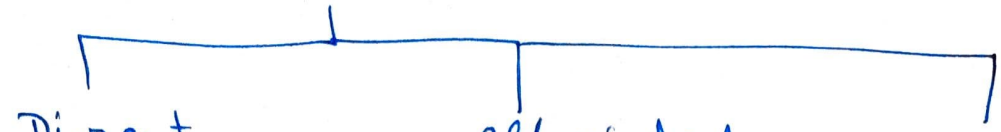


Virtual Address Cache :- When a ~~the~~ Cache is indexed or tagged with virtual Address



C.M (2)

Cache Mapping



Direct Mapping

~~Block Index ← Block_j % # Block Frame~~

$$Block\_Frame_i \leftarrow Block_j \% \#Block\_Frames$$

Block size = Block_Frame size.

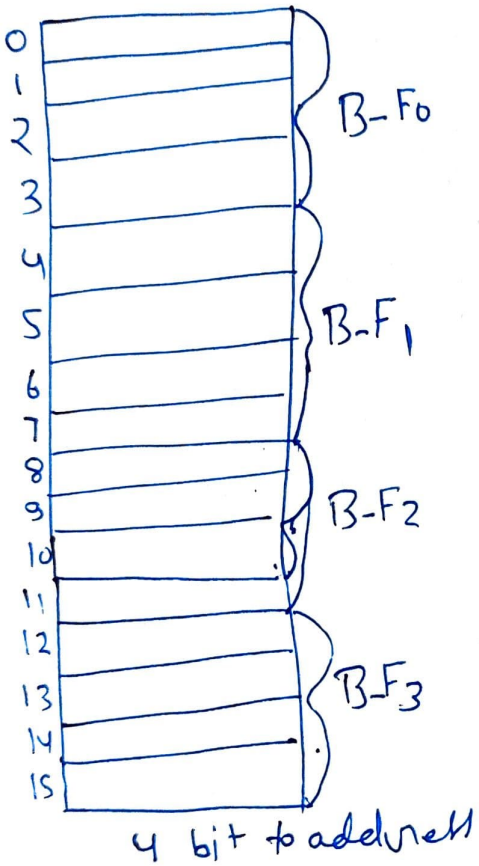
→ Let Memory is word addressable and Block size is 4 word.

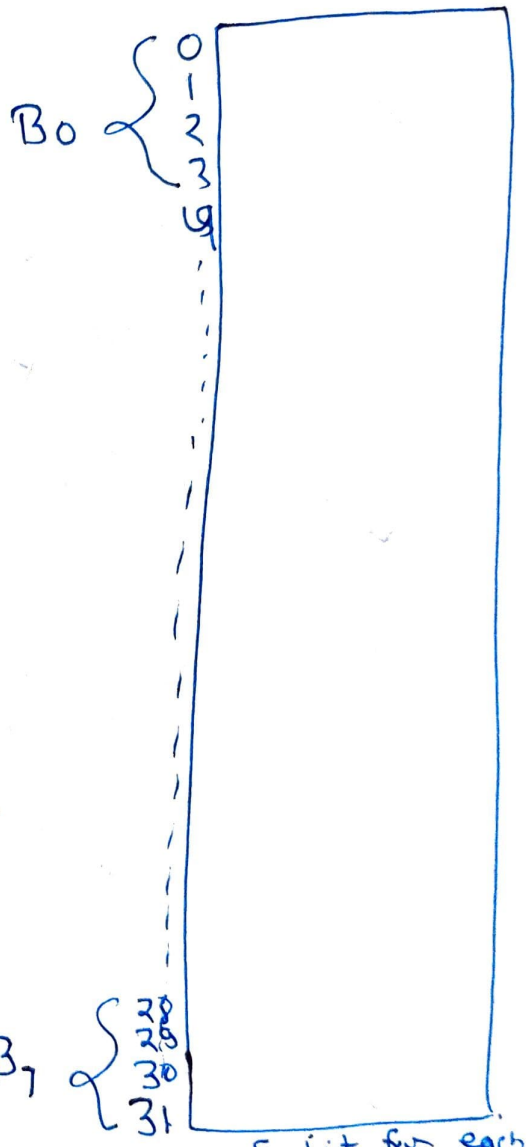
Mean that each ~~word~~ block will have 4 four word. It require 2 bit to address each word

→ Now Cache size is 16 word. So # Block_Frames are 4. So it also Requires 2 bit to address each Block_frame.

C. M (3)

→ Main Memory size is 32 word. So # Blocks are 8 and total bits required to access each Block are is 3 bit





B-F	W
2	2

B	W
3	2

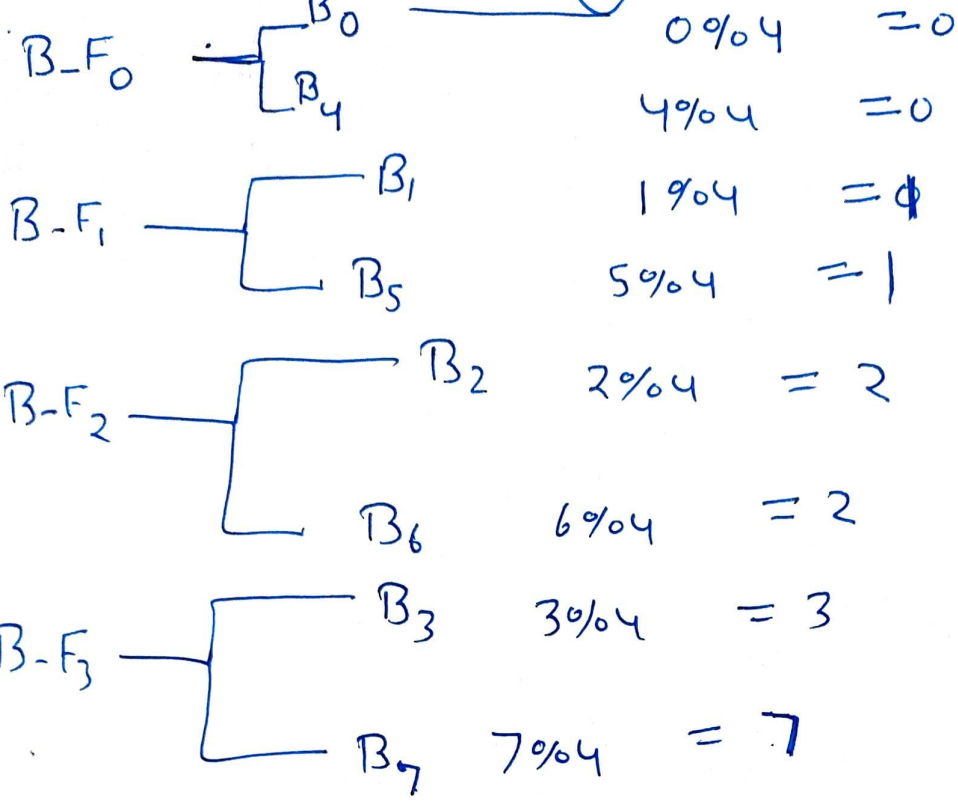
Mapping Arrangement

Tag	Block	W

B-(B-F)	B-F	W

Tag	B-F	W
1	2	2

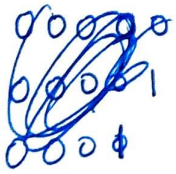
C.M. (4)



1	2	2

Example.

initially cache is empty –



0 0 0 0 0

0 0 0 0 1

0 0 0 1 0

0 0 0 1 1

0 0 1 0 0

0 0 1 0 1

0 0 1 1 0

0 0 1 1 1

0 1 0 0 0