Computer Organization & Architecture

"Computer Organization and Embedded Systems"

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Control signals

- In each clock cycle:
  - Results of actions in one stage stored in inter-stage registers
  - Available for use by the next stage in the next clock cycle
- Data transferred from one stage to next in every clock cycle:
  - Inter-stage registers are always enabled
  - This is the case for registers RA, RB, RZ, RY, RM, and PC-Temp
- Contents of other registers, namely, PC, IR, and register file, must not be changed in every clock cycle
  - New data are loaded only when called for in a particular processing step
  - They must be enabled only at those times

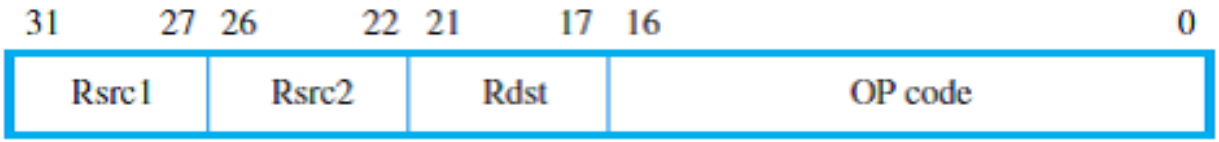
Control signals

- Role of multiplexers: select data to be operated on in any given stage
- Ex., in stage 3, MUXB:
- Selects immediate field in IR:
  - For instructions that use an immediate source operand
  - For instructions that use immediate data as offset when computing effective address of a memory operand
- Otherwise, it selects register RB

Control signals

- Data selected by multiplexer MUXB are used by ALU
  - ALU is used only in step 3
    - Selection made by MuxB matters only during that step
  - To simplify required control circuit, same selection can be maintained in all execution steps
  - Similar observation can be made about MuxY

Instruction Encoding



(a) Register-operand format

(b) Immediate-operand format

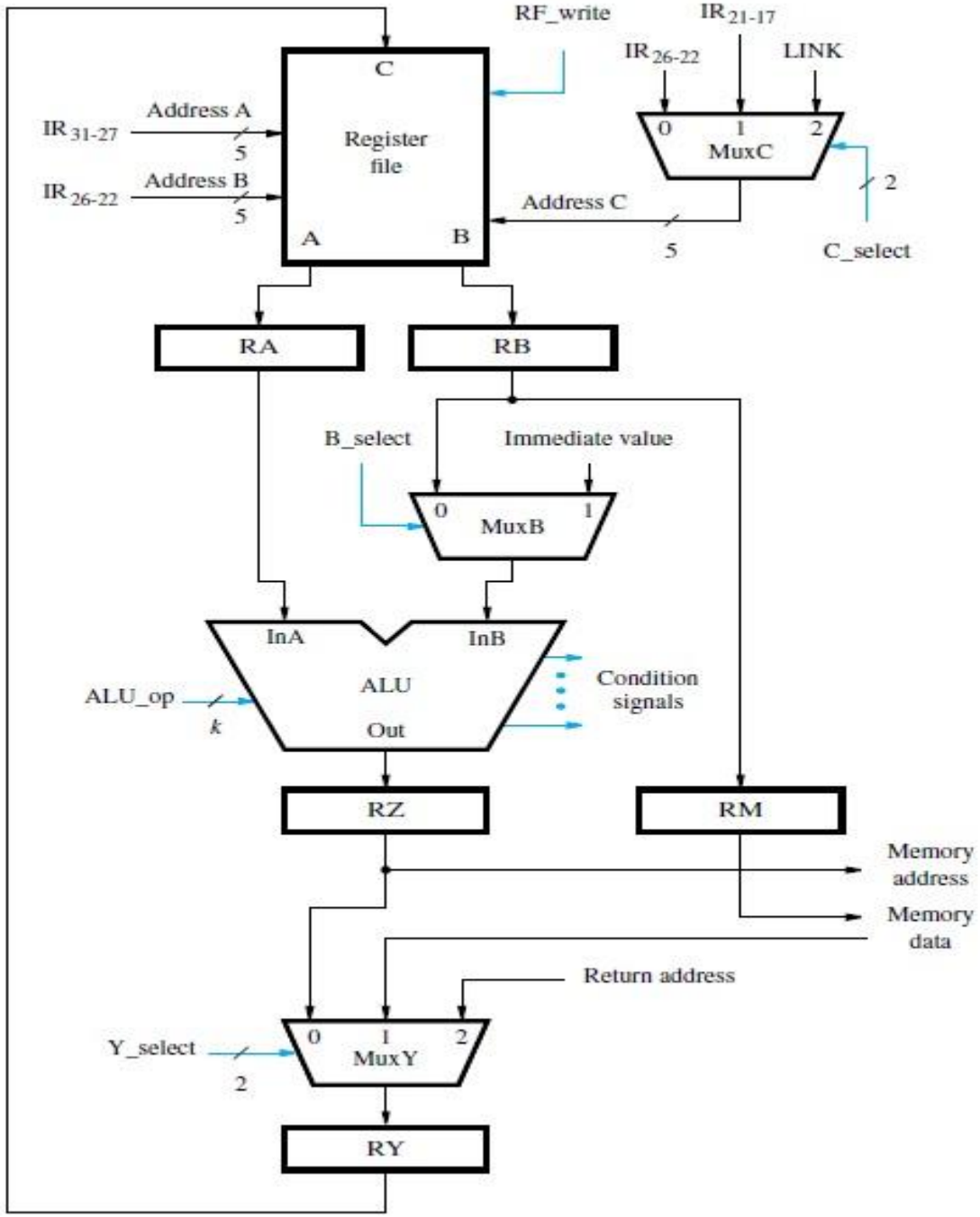
(c) Call format

Control signals

- Assume register file has three 5-bit address inputs
  - Allows access to 32 general-purpose registers
- Addresses A and B determine registers to be read:
  - Connected to fields $IR_{31–27}$ and $IR_{26–22}$ in instruction register
- Address C selects the destination register:
  - Multiplexer MuxC selects the source of that address
  - Three-register instructions use bits $IR_{21–17}$ and other instructions use $IR_{26–22}$ to specify the destination register
  - Third input of multiplexer is address of the link register
  - New data are loaded into the selected register only when the control signal RF_write is asserted

Control signals

- Operation performed by ALU is determined by a k-bit control code, ALU_op
  - Can specify up to 2^k distinct operations
- When an instruction calls for two values to be compared
  - A comparator performs the comparison specified
  - Comparator generates condition signals that indicate result of the comparison
  - These signals are examined by control circuitry during the execution of conditional branch instructions to determine whether the branch condition is true or false.


RF_write
IR21-17
IR26-22
LINK
C
Address A
IR31-27
5
Register file
Address B
IR26-22
5
A
B
0
1
2
MuxC
2
Address C
5
C_select
RA
RB
B_select
Immediate value
0
MuxB
1
InA
InB
ALU_op
k
ALU
Out
Condition signals
RZ
RM
Memory address
Memory data
Return address
Y_select
2
0
1
2
MuxY
RY

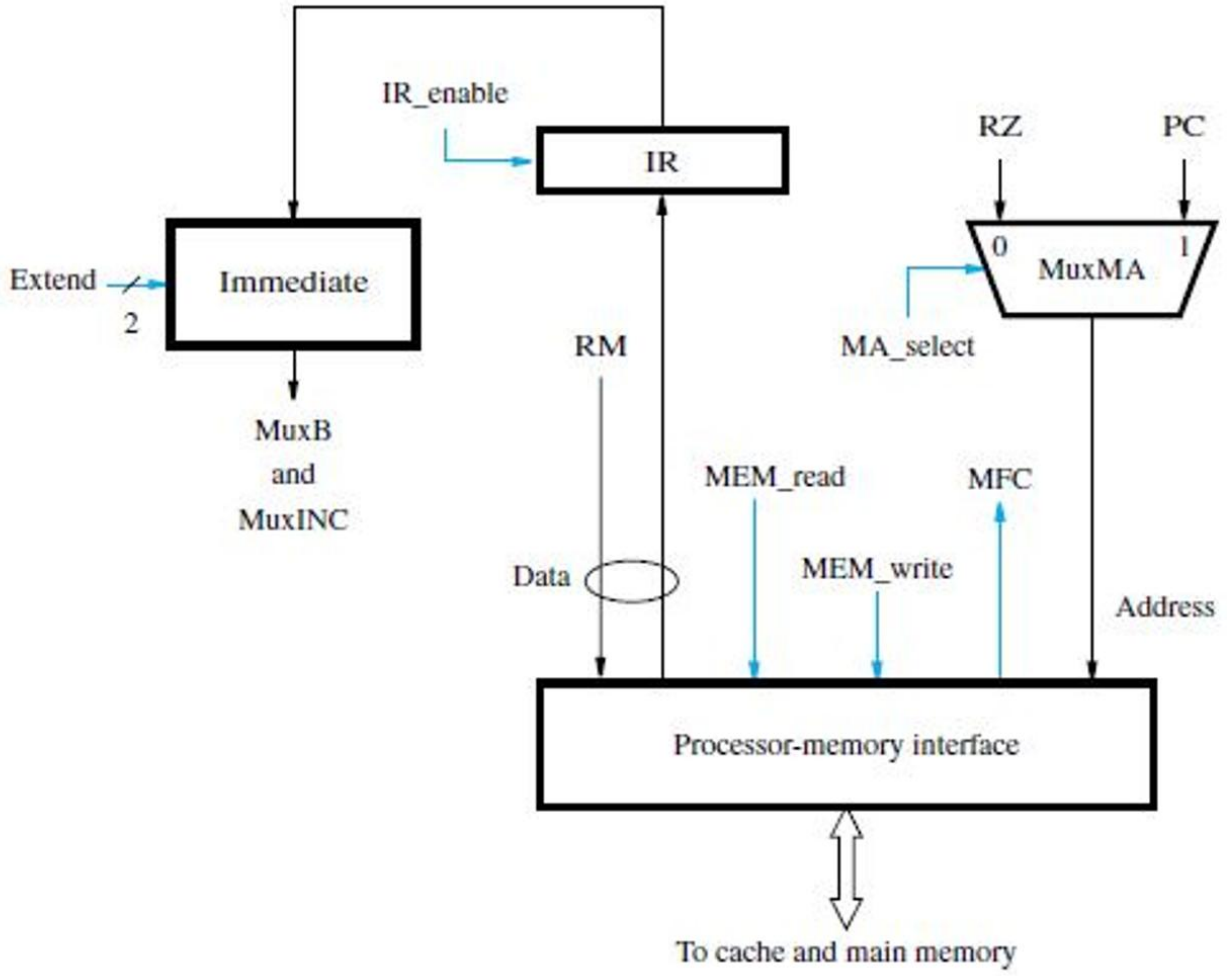
Control signals

- MuxMA must change selection in different execution steps
- Selects PC as source of memory address during step 1
  - When a new instruction is being fetched
- Selects register RZ during step 4 of Load and Store instructions
  - Contains effective address of memory operand

Control signals

- Interface between the processor and the memory:
  - Two signals, MEM_read and MEM_write are used to initiate a memory Read or a memory Write operation.
  - When requested operation has been completed, interface asserts the MFC signal.
- Instruction register has a control signal, IR_enable
  - Enables a new instruction to be loaded into the register.
  - During a fetch step, it must be activated only after MFC signal is asserted.

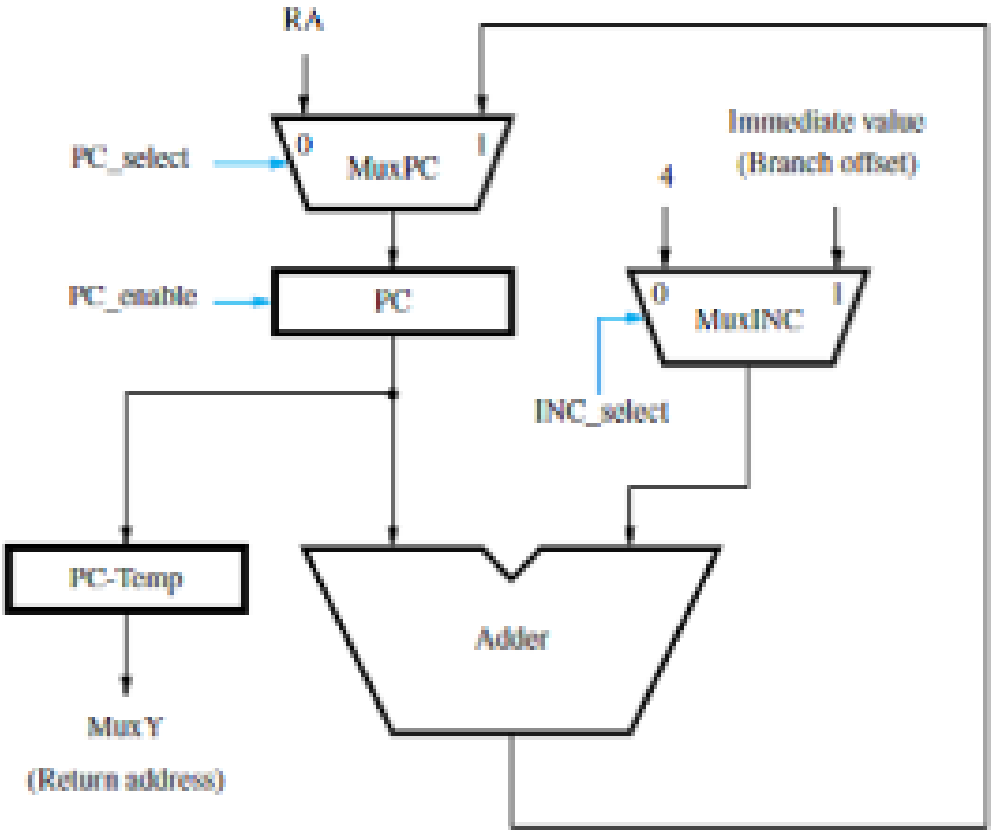
Control signals: Processor-memory interface



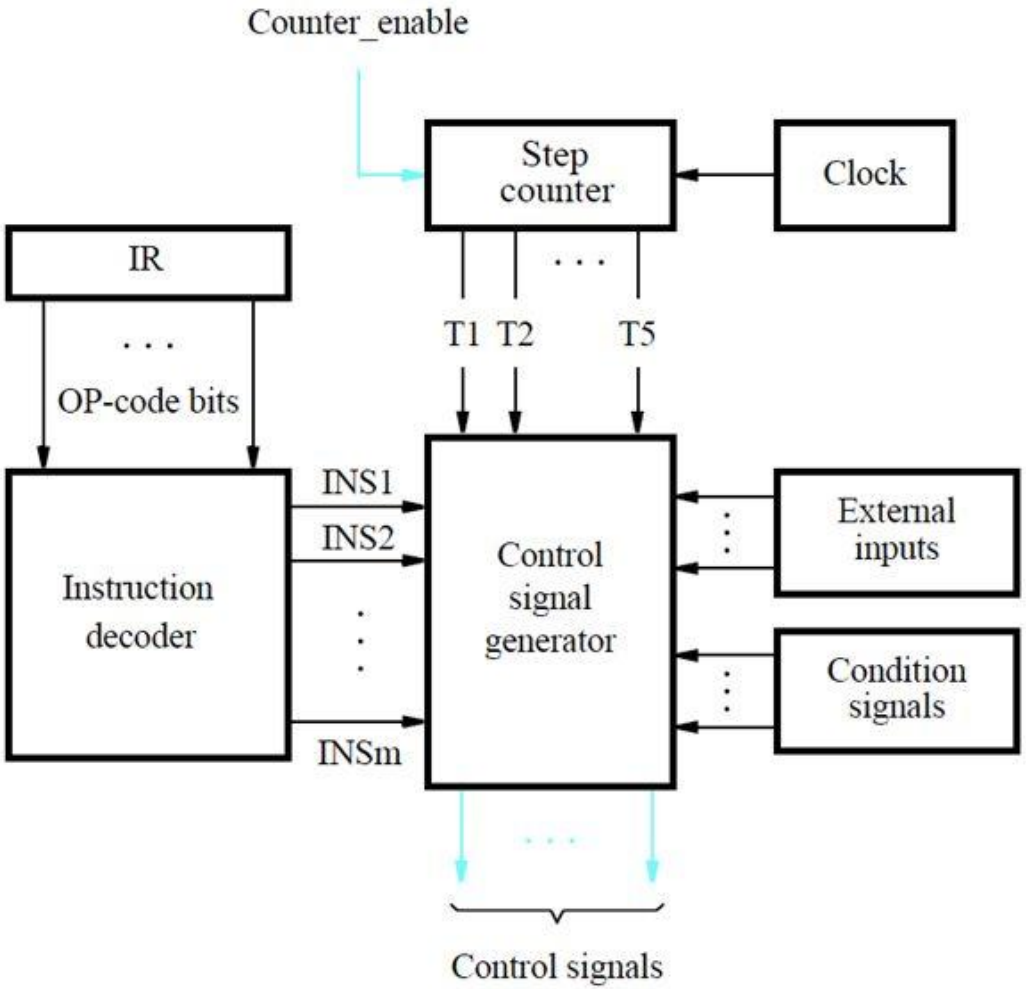
Control signals

- Signals that control the operation of the instruction address generator:
  - INC_select signal selects the value to be added to the PC
  - Either constant 4 or branch offset specified in the instruction.
- PC_select signal selects:
  - Either updated address
  - Or the contents of register RA
  - To be loaded into the PC when the PC_enable control signal is activated

Control signals: Address generator



Hardwired generation of control signals



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