Computer Organization and Architecture LAB

ASSIGNMENT-7

Pipeline

Q. On a three-address machine, the following instructions are to be executed in the given sequence.

I1: LOAD @R1, R2

I2: SUB R3, R2, R2 //Third operand is used to store result

I2: NOP //No operation

I3: AND R2, R3, R8

The instructions are stored in binary format. Assume instruction length of 15 bits and 4-bit register addresses.

The machine uses a 4-stage pipeline with the Fetch, Decode, Execute and Write-back stages. The operands needed for execution are put in the ALU input buffers at the end of the second stage. Assume that the memory address computed in Instruction 1 is not found in the cache and it takes 1 extra clock cycle to read contents from memory.

Write a program to simulate a “Hazard Check” unit to determine if there are RAW and WAW data hazards. The program should be able to display a message if hazards are present. The message should identify the instructions and registers which are causing the hazard and also print the type of hazard.