Computer Organization & Architecture (Instruction Set Architecture)

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Design of Instruction Sets

CISC Vs RISC

Complex Instruction Set Computing (CISC)

- Characteristics of CISC Style
    - Complete a task in as few lines of assembly as possible.
    - Compiler has to do very little work to translate a HLL statement into assembly language
    - Very little RAM is required to store instruction
    - Build processor hardware that is capable of understanding and executing the operations.
    - Complex instructions, hence complex instruction decoding.
    - Instruction generally take more than single clock cycle to get executed.
    - More complex instructions, hence may span multiple words
    - Less number of general purpose register.

Reduced Instruction Set Computing (RISC)

- Characteristics of RISC Style
  - Compiler must perform more work to convert a high level language statement into code of this form
  - Simple instructions, hence simple decoding
  - More instruction, so program is larger in size
  - All instructions fit in a single word
  - Instruction take single clock cycle to be executed
  - Load/Store architecture is used
  - More number of general purpose registers
  - Pipelining can be achieved

Expanding Opcodes

Consider a machine supports an (n + k) bit instruction with a k-bit opcode and a single n-bit address

- How many different operations and addressable memory cells possible?

Example: Expanding Opcode

Consider a machine in which instructions are 16 bits long and addresses are 4 bits long.

- Requirement:15 three-address instructions, 14 two-address instructions, 31 one-address instructions, and 16 instructions with zero address.

Expanding Opcodes

Steps to solve problems on expanding opcodes

1. Identify high order instruction
2. Identify total no. of possible instruction
3. Identify no. of free opcode from primitive instruction
4. Calculate the no. of drived instruction possible by multiplying the no. of free opcode with a decoded value of address field.

Example: Expanding Opcodes

- Consider a hypothetical 24-bit CPU which support one word long instruction. Instruction is placed in a 256KW memory.If there exist 60 1-address instructions, then how many zero-address instructions are possible?

Example

- Consider a hypothetical CPU which support both One-address and Zero-address instruction. A 32-bit instruction is placed in 32MW memory. What is the range of 0-address and 1-address instruction possible in the CPU.