The LNM Institute of Information Technology

Computer Science and Engineering
Computer Organization and Architecture (CSE 216)
Mid Term Exam 2020-21

Duration: 90 minutes **Date: 26-Sept-2020** **Maximum Marks: 20**

Instructions: Please be precise and concise while writing the answers.

1. Short Questions: answer the following questions with True or False. Then use exactly one sentence to describe why you chose your answer. Without stating the reasoning, you will not get any points. **(0.5 + 0.5 + 0.5 + 0.5 + 0.5 + 0.5 + 0.5 + 0.5)Marks**

   (a) In instruction decode phase, first the memory is read and then the contents of memory at the address contained in the PC regtister are loaded into Instruction Register.
   Solution: False: Instruction fetch phase.

   (b) The 2's-complement system is the most efficient method to represent the signed numbers.
   Solution: True: Single representation of zero.

   (c) The load instruction is used to load the desired immediate value.
   Solution: False, Memory Operands.

   (d) The assembler can detect all the programming errors.
   Solution: False: The assembler can only detect and report syntax errors, programming errors are detected by debugger.

   (e) For nested subroutines, the return addressess are stored in stack and used in first in first out manner.
   Solution: False, LIFO Manner.

   (f) Indexed Addressing Mode is suitable for program relocation at runtime.
   Solution: False, PC-Relative Addressing Mode.

   (g) In 2's-complement system, shifting a number one bit position to the left is equivalent to dividing it by 2 and shifting it to the right is equivalent to multiplying it by 2.
   Solution: False, In 2's-complement system, shifting a number one bit position to the left is equivalent to multiplying it by 2 and shifting it to the right is equivalent to dividing it by 2.

   (h) In both autodecrement and autoincrement mode, the address is decremented and incremented respectively before it is used in the instruction.
   Solution: False, In autodecrement, first decrement then use while in autoincrement mode first use then increment.

2. Consider the following questions: **(2 + 1+ 1) Marks**

   (a) Convert the following pairs of decimal numbers to 5-bit 2's-complement numbers, then perform addition and subtraction on each pair. For subtraction, the second number of each pair is to be subtracted from the first number. Also state whether or not overflow occurs in each case.

   (i) -9 and -15
   (ii) 6 and -8

   Solution 2a:
   (i)

   -9 = 10111 (2's complement)
   -15 = 10001 (2's complement)

   Addition = (-9) + (-15) = 01000 (overflow)

   Subtraction = (-9) - (-15) = 00110 (not overflow)

   (ii)
   2's complement representations

6 = 00110

-8 = 11000

Addition = 6 + (-8) = 11110 (not overflow)

Subtraction = 6 - (-8) = 01110 (not overflow)

(b) Convert the given IEEE-754 single-precision 32-bit pattern 11011011001100000000000000000000 into decimal representation.
Solution 2b:
Sign = 1
$E^{'} = 10110110 = 182$
$E = E^{'} - 127 = 55$
$M = 1.01100000000000000000000$
$M = 1 + (0.25) + (0.125) = 1.375$

Answer $=1.375 * (2^{55}) = 4.95 * (10^{16})$

(c) Represent the given decimal number -105.25, into IEEE-754 standard single-precision 32-bit format and compute its equivalant hexadecimal notation.
Solution 2c:

$105.25 = 1101001.01 = 1.10100101 * (2^6)$
Sign = 1

E' = 6 + 127 = 133 = 10000101

M = 10100101000000000000

Answer = 1 100 0010 1101 0010 1000 0000 0000 0000

Hexadecimal representation = C2D28000

3. Consider a hypothetical CPU that supports two addresses, one address and zero-address instruction formats. A 24-bit instruction is placed in a word-addressable 1K word memory. If there exist 8 two address instructions and 150 one address instructions, then how many zero-address instructions can be formulated? **4 Marks**
Solution Q3: Expand opcode technique:
1K word memory so 1K = 2^{10} hence 10 bit address
(i) Highest 2 address instruction: 4bit for opcode + 10bit for address1 + 10bit for address2= 24bits Instruction Format
(ii) Number of operations: $2^4 = 16$
(iii)8 two address instructions so remaining number of free opcode after allocating 8 two address instruction: $16 - 8 = 8$
(iv) Number of one address instruction supported: $8 \times 2^{10} = 8192$
(v) Number of free opcode after allocating 150 one address instructions: $8192 - 150 = 8042$
(vi) Number of Zero Address Instruction: $8042 \times 2^{10} = 8235008$

4. Consider a hypothetical machine which uses different operand accessing mode as shown below:

$OperandAccessingMode$	$Frequency\%(Probability)$
$ImmediateAM$	25
$RegisterAM$	28
$DirectAM$	18
$MemoryIndirectAM$	14
$IndexedAM$	15

(1)

assume the 3 clock cycles consumed for memory access, 2 clock cycle consumed for arithmetic computation, 0 clock cycle consumed when data is present in the register or Instruction itself, What is the average operand fetch rate of the machine? **2 Marks**

Solution Q4: Average Operand Fetch Rate: $(25\% \times 0cycle) + (28\% \times 0cycle) + (18\% \times 3cycle) + (14\% \times 2 \times 3cycle) + (15\% \times (0+2+3)cycle) = \frac{213}{100} = 2.13cycle$

5. For the 5-stage machine discussed in class, give the complete sequence of actions in each stage for the instruction STORE R7, (R8). **2 Marks**
Solution Q5:

T1: MAR ← [PC], Read, Wait for MFC, PC← [PC] +4, IR← [MDR]
T2: Decode, RA ← [R8], RB ← [R7]
T3: RZ ← [RA], RM ← [RB]
T4: MAR ← [RZ], MDR ← [RM], Write, Wait for MFC
T5: No action, End

6. Assume a 5-stage machine executes only two instructions: ADD Reg, Reg, Reg and CALL (Reg). For generation of the control signal RF_WRITE (to enable register file), two AND gates (G1 and G2) and one OR gate G3 is used. Specify the inputs to each of the gate. **2 Marks**
Solution Q6:
Input to G1: ADD, T5
Input to G2: CALL, T5
Input to G3: Output of G1 and G2

7. Consider the mentioned program which uses eight temporary variables a, b, c, d, e, f, g h. All the operations must take their operands from registers except constant values.
a = 1
b = 11
c = 10
d = a+b
e = c+d
f = c+e
b = c+e+f
e = b+f
d = 5+e
h= d+1
g = 5+e +h+d
return d+f
Determine the minimum number of registers needed to execute this program? Also show the steps for determining the minimum count. **2 Marks**

Solution Q7: Minimum number of required regiesters are: 4
a = 1 ; R1
b = 11 ; R2
c = 10 ; R3
d = a+b ; R1 = R1+R2
e = c+d ; R2= R3+R1
f = c+e ; R1= R3+R2
b = c+e+f ; R3= R3+R2+R1
e = b+f ; R2= R3+R1
d = 5+e ; R3= 5+R2
h= d+1 ; R4= R3+1
g = 5+e +h+d ; R2= 5+R2+R4+R1
return d+f ; R1+R3