ECE214(L): Digital Circuits and Systems Lab

Programme: B.Tech./Dual Degree (ECE) Year: IInd Semester : I
Course : Core for all ECE, and CCE Credits : 2 Hours : 30

Course Context and Overview (100 words):

Introduction to the Digital Logic Circuits and systems is towards the aim of designing the fastest growing technology digital systems over given specifications. This course will equip the students to think of their own digital processors and build them on hardware (ASICs or FPGAs). This is laboratory course and students would learn VHDL language to implement basic digital systems first and then move on to daily life examples of digital systems.

Prerequisites Courses: None

Course outcomes (COs):

On completion of this course, the students will have the ability to:
CO1: Know the basics of VHDL coding and different styles of coding.
CO2: Implement and synthesize adders, and multiplexers using Xilinx Vivado.
CO3: Implement and synthesize various encoder and decoder blocks.
CO4: Implement and synthesize flip flop, counters and registers.
CO5: Implement and synthesize finite state machines using VHDL.

Course Topics:

Topics	**Lab Sessions**	**Hours**
UNIT - I **1. Topic** Function Implementation using VHDL in Vivado.	1	3
1.1 Realize the function, mentioned below with at least four different physical ways. F(x) = x0+ x1 + x2 + x3 + x4 + x5 + x6 + x7 + x8 + x9	1	
UNIT - II **2. Topic** VHDL implementations of Adders and MUXes	4	12
2.1 Design, simulate and implement Half adder, Full adder using dataflow, behavioral and structural modeling in VHDL.	1	
2.2 Implement 4 bit ripple carry adder using structural modelling. Implement 4 bit adder/subtractor using structural modelling.		
2.3 Implementation of 2x1, 4x1 and 8x1 multiplexers using dataflow, behavioral and structural modeling in VHDL	1	
2.4 Implement 1x2, 1x4 and 1x8 demultiplexers using dataflow, behavioral and structural modeling in VHDL. Implement Boolean functions using MUX	1	

UNIT - III **3. Topic** VHDL Implementations of Encoder, decoders and multipliers	6	6
3.1 Implement 1 to 2, 2 to 4 and 3 to 8 line decoder using dataflow, behavioural and mixed modeling in VHDL. Implement Booleans functions using decoders.	1	
3.2 , Implement a 3 bit multiplier to perform the operation A*B on two 3 bit vectors. Design a combinational circuit that has three inputs and three outputs and specified problem statement.	1	
UNIT - IV **4. Topic** Sequential Circuit Design	6	6
4.1 Design D latch, JK flip flop, RS flip flop and T flip flop using behavioral and structural modeling.	1	
4.2 Design 4 bit binary counter by using clock variable and 8 bit Gray counter. Implement both as up as well as down counters.	1	
UNIT-V **5. Topic** Finite State Machine Design	3	3
5.1 Design moore's machine and mealey machine for a candy vending machine	1	

Textbook references (IEEE format):
Text Book:

1. *FPGA Prototyping by VHDL Examples*: *Xilinx Spartan-3 Version*, Pong P. Chu
2. *Essential VHDL: RTL Synthesis Done Right*" Sundar Rajan
3. *VHDL: Programming by Example*, Douglas L. Perry

Reference books:
Additional Resources (NPTEL, MIT Video Lectures, Web resources etc.):
https://onlinecourses.nptel.ac.in/noc15_ec01

Evaluation Methods:

Item	Weightage
Quiz 1	10
Quiz 2	10
Quiz 3	10
Quiz 4	10
Lab record evaluation	10
Mid Term Lab Test	20
End Sem Lab Test	30