DCS Lab

Experiment - 7

Aim: Shift Register Design Using VHDL

Description:

Part1:

A. Write a VHDL code for 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out. In your testbench show at least 25 cycles and starts loading the data 1000111100011100011001100. Confirm with the help of simulation that the same data is output at **Serial Out** after 8 cycles.

B. Repeat the problem statement of part A by adding an extra reset input signal. If reset is 1 then the current state of register becomes 00000000. Load the same serial input data and provide reset = 1 for t = 10 and 19.

C. Write a VHDL code for 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out. In your testbench show at least 25 cycles and starts loading the data 1000111100011100011001100. Confirm with the help of simulation that the same data is output at Parallel Out after 8 cycles.

D. Write a VHDL code for 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out. Take 2 different 8-bit Shift-Left Registers as component and implement the final 16 Bit register. Show at least 40 cycles in your testbench and load the data 1000111100011100011001100 serially starting from t =0.