LNMIIT
The LNM Institute of Information Technology

DCS Lab

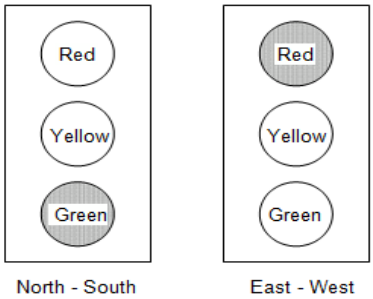
Experiment - 10

Aim: Traffic Light Controller using state Machines

Part1:

Description:

The set of traffic lights are shown in Figure. The lights are assumed to be at a four-way intersection with one street going north-south and the other road going east-west.



If we use a 3 Hz clock to drive this state diagram then a delay of 1 second is achieved by staying in a state for three clock cycles. Similarly, a delay of 5 second is achieved by staying in a state for fifteen clock cycles. Write a VHDL code for the same using state machines. Show at least 25 clock cycles in your testbench.

State	North-South	East-West	Delay (Sec)
S0	Green	Red	5
S1	Yellow	Red	1
S2	Red	Red	1
S3	Red	Green	5
S4	Red	Yellow	1
S5	Red	Red	1

Part2:

A. For each type of the above implementations generate the synthesis report.
B. Study delay, power and cell usage for each implementation.
C. Generate the corresponding testbench to verify the design.