Experiment No.: 05

1 AIM

1. To generate frequency modulated signal (using varactor diodes in the oscillator circuit).
2. To study the characteristics of Phase Locked Loop, identify Lock and Capture range.

2 List of components and equipments

1. Varactor diodes
2. 565 PLL IC
3. Digital signal oscilloscope
4. Opamp-741 IC
5. DC power supply
6. Function Generator
7. Resistors
8. Connecting wires
9. Breadboard
10. Capacitors

3 Theory

3.1 Connection Diagram of Frequency Modulation and PLL

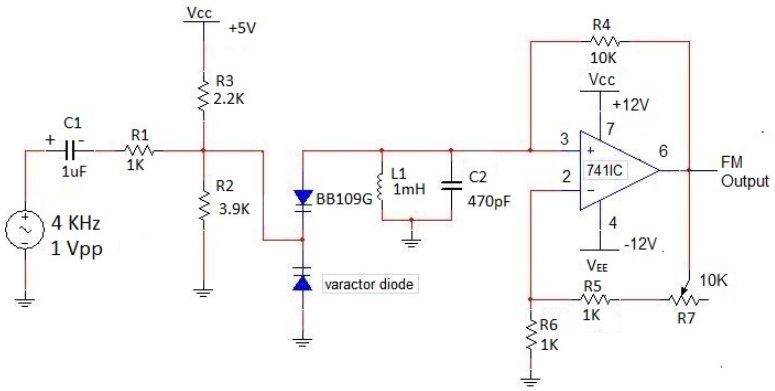

Figure 1: Frequency modulator using varactor diodes in the oscillator

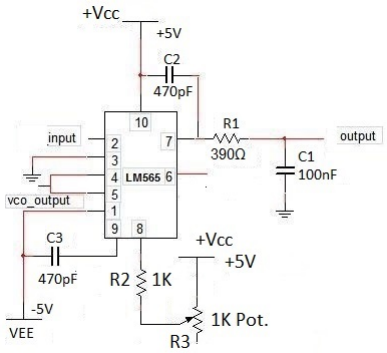

Figure 2: Phase Locked Loop

4 Procedure

4.1 Generation of FM using varactor diodes

1. The capacitance of varactor diode in $Figure1$ is given by 100/sqrt(V), where V is the amount of reverse bias voltage across p-n junction. Increasing the reverse bias voltage applied across the diode decreases the capacitance, the depletion region becomes wider. When an ac voltage is applied across the diode, the capacitance varies with the change in amplitude.
2. Generate a modulating signal of an amplitude $1V_{pp}$ with a fundamental frequency $f_m = 4KHz$ and apply as input to FM modulator as shown in $Figure1$.
3. Caluculate the oscillating frequency from the $Figure1$ using the expression
$$\frac{1}{2\pi\sqrt{LC}} \tag{1}$$
4. Observe the frequency modulated wave and note down the frequencies corresponding to the positive peak and negative peak of the modulating signal.

4.2 Study of PLL characterstics

1. Connect the circuit as shown in $Figure2$. Now adjust the potentiometer R_3 to get the free running of $200KHz$ which is given by
$$f_0 = \frac{0.3}{(R_2 + R_3)C_3} \tag{2}$$
2. Give sine wave of $1V_{pp}$ of $200KHz$ as input to $pin2$. Connect input signal at $channel1$ of DSO and VCO output at $channel2$ of DSO. When PLL is in frequency-lock with input, input signal and output signal of VCO will not move with respect to each other(why?). Now decrease the frequency of input signal very slowly (why?) and keep on observing both signals on DSO. At some frequency both signals will start moving with respect to each other, this is lower lock frequency at which PLL looses it's frequency lock. Now PLL is out of lock, keep on increasing input frequency. At some frequency PLL will retain it's lock, this is lower capture frequency. In the same way, caluculate upper lock and capture frequency. Difference between lower and upper lock and capture frequency is defined respectively as lock range and capture range, which is given by
$$f_L = \pm\frac{8f_o}{V_c} \tag{3}$$
where $V_c = V_{cc} - (-V_{cc})$
$$f_c = \pm\frac{1}{2\pi}\sqrt{\frac{2\pi \times f_L}{3.6 \times 10^3 \times C_2}} \tag{4}$$
3. Study the Voltage-Frequency(V-F) characteristics, by changing f_i from $50kHz$ to $400kHz$ (following the same procedure given in Exercises: 4.2.2) and observe the DC output at $pin7$. Draw the V-F curve.

5 Observation

Write/ Plot Your Own With Observation Table (If Required).

6 Analysis of Results

Calculations/Display/plot/typical graph Write/Plot Your Own.

7 Conclusions

Write Your Own.

Precautions

(1) Check the connections before Switching ON the power supply.
(2) Connections should be done properly.
(3) Observation should be taken properly.