COL215 LAB Assignment 5 : Creating Display Effects using 7-Segment Display

Mohit Sharma(2019CS10372), Arka Mandal(2019CS50617)

1 Aim

A 4-digit BCD input taken from the slider switches is to scroll from right to left at a pre-determined speed. But the intensity of the digit being displayed on the rightmost display should be minimum and that on the leftmost display should be maximum

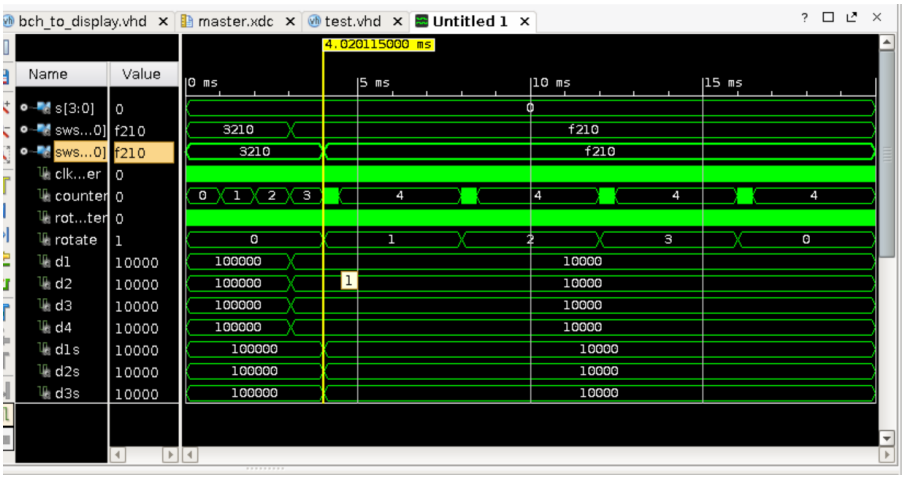
2 Design

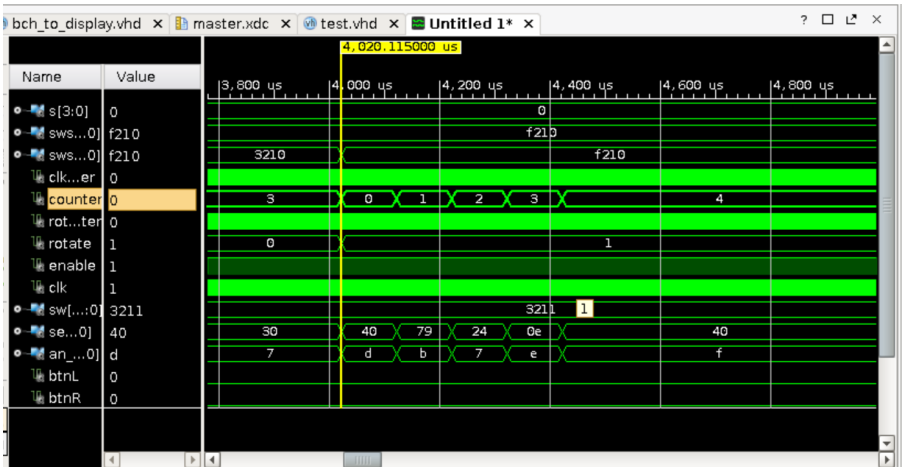
There are two push button inputs.
The left push button sets the hexadecimal value to be shown on display as the corresponding 16 bit binary from the 16 slider switches.
The right push button is used to set the brightness level of all four digits. The rightmost 8 slider switches dictates the brightness level of the displayed digits(2 slider switch for each digit -¿ 4 levels of brightness).
Also the clock is taken as input from the FPGA board, the clock is of 100MHz frequency.
A counter is made which changes the 'to be' lighted anode every 100000 clock cycles , i.e, every 1ms. So the overall refresh cycle is of 4 ms.
When brightness level of corresponding digit is low then its anode is turned on for a lesser number of clock cycles then 100000. For the extra clock cycles all anodes are turned off.

3 Simulation

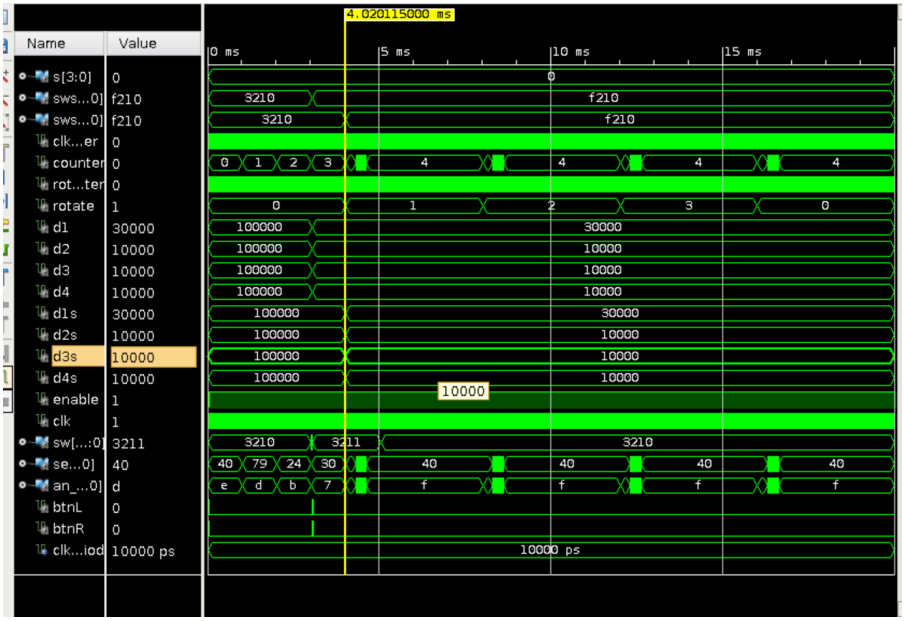
The code is simulated on test-bench created by the name test.vhd.

The below two images show the changes of digits are being done after the rotation is completed and not abruptly in between.





The below two images show the change of brightness are being done after the rotation is completed and not abruptly in between and also these denotes how brightness is attached to the digits it self and not display.



4 Utilisation Report

192 LUT's are used (as logic)
183 registers are used as flip-flops.
30 Input Output Blocks are used (16 switch inputs(sw) and 1 clock input(clk) and 7 segment outputs(seg) and 4 display outputs(an) and 2 push button inputs)
1 BUFGCTRL is used (to enable clock)

Ref Name	Used	Functional Category
FDRE	183	Flop & Latch
LUT2	76	LUT
LUT1	56	LUT
LUT6	36	LUT
CARRY4	32	CarryLogic
LUT4	31	LUT
IBUF	19	IO
LUT5	12	LUT
OBUF	11	IO
LUT3	7	LUT
BUFG	1	Clock

(Utilisation report is also given in the submission.)