COL215: Digital Logic and System Design

Special Laboratory Semester, AY 2021-22

Department of Computer Science & Engineering

Course Schedule

Assignment 1 (25th April to 27th April 2022)

Familiarize with the BASYS board as well as XILINX synthesis tools. Try downloading any simple logic gate controlled by switch inputs while showing the result on an LED.

Assignment 2 (28th April to 30th April 2022)

Design a decoder for 4-bit BCD input to 7-segment display and demonstrate its functioning using the slider switches and 7-segment display.

Assignment 3 (2nd May to 4th May 2022)

Accept 4 BCD digits from the slider switches and display the same on the four 7-segment displays.

Assignment 4 (5th May to 7th May 2022)

Create a variable brightness and display effect on 7-segment displays using pulse width modulation.

Assignment 5 (9th May to 11th May 2022)

Modify design in Assign-4 so that the 4 digits scroll from right to left and keep on increasing in intensity as they approach the leftmost digit. Design should be based on a state machine that controls scrolling.

Assignment 6 (12th May to 14th May 2022)

Design a stopwatch with Start/Continue, Stop and Reset.

Assignment 7 (16th May to 18th May 2022)

Establish serial communication where data transmitted by the PC can be received and displayed in the BASYS board.

Assignment 8 (19th May to 21st May 2022)

Establish serial communication where data transmitted by the BASYS board can be received and displayed on the PC.

Assignment 9 (23rd May to 25th May 2022)

Design a 16X8 FIFO buffer using BRAM as memory and input BCD digits using switches and display on the 7-segment displays.

Assignment 10 (26th May to 28th May 2022)

Establish file transfer from PC to BRAM using the serial port.

Buffer Days (30th May and 31st May 2022)

Unfinished lab experiments or pending vivas.