

# COL215 LAB Assignment 10 : File Transfer through Serial Receiver/Transmitter

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## 1 Aim

Learn how to transfer files between PC and FPGA board. In this you need to utilize many of the previous modules including serial transfer, memory, 7-segment displays etc.

## 2 Design

Input is taken from 2 push buttons : up(transmit), down(reset)

Initially the display shows nothing.

While transferring a file, individual digits light up on the display.

After transmission is done or buffer gets full, no further data is recieved and we are ready to transmit.

On pressing the transmit button, all the data stored in buffer is transmitted back through the cable.

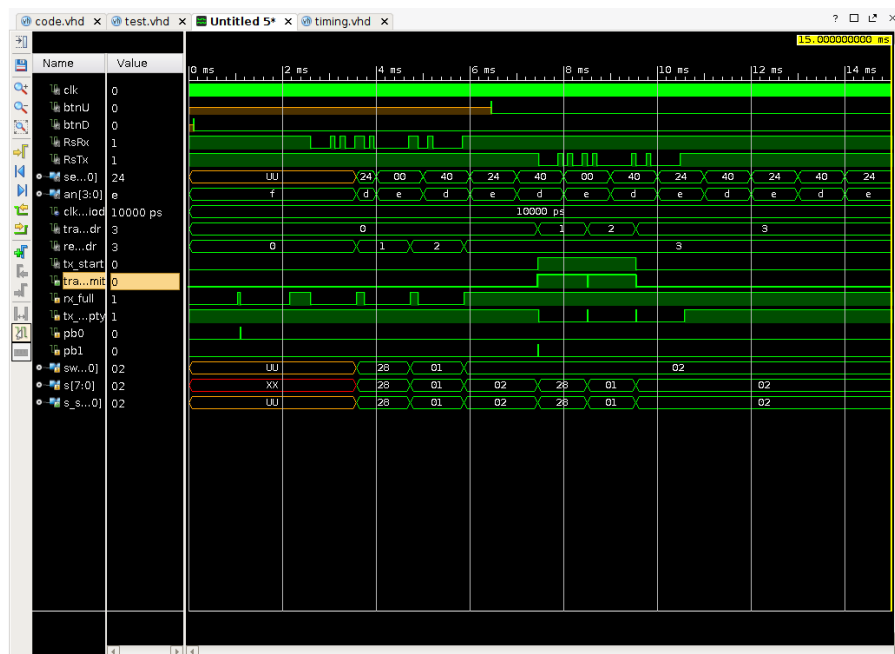
The display lights up again as each data passes through the transmitter.

After transmission is done, we need to press reset button to get the device ready for another file transfer.

## 3 Simulation

The code is simulated on test-bench created by the name test.vhd.

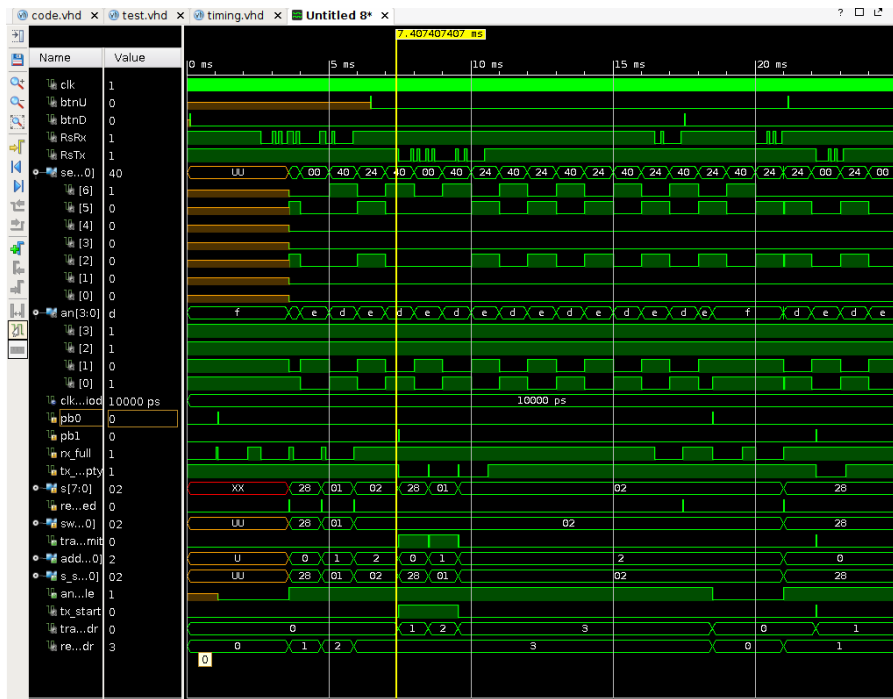
The below two images show the simulation of simple 3 bytes data received and then transmitted after pressing the up(transmit) button.





The below two images show how after transmission is done, the received bits are ignored until reset is pressed again. Only the bits received after reset is pressed are stored in bram and transmitted later on.





## 4 Utilisation Report

205 LUT's are used (as logic)

154 registers are used as flip-flops.

16 Input Output Blocks are used (1 clock input(clk) and 7 segment outputs(seg) and 4 display outputs(an) and 2 buttons(btnU,btnD), 1 RsRx (receiver) and 1 RsTx(transmitter) )

2 BUFGCTRL is used (to enable clock)

1 bram blk mem gen 0 0 is used as block memory for storage of file content.

The bram itself takes 0.5 Block RAM Tile and 1 RAMB18E1 primitive.

Ref	Name	Used	Functional Category
FDRE		152	Flop & Latch
LUT6		70	LUT
LUT1		54	LUT
LUT3		37	LUT
LUT4		31	LUT
LUT5		30	LUT
LUT2		22	LUT
CARRY4		14	CarryLogic
OBUF		12	IO
IBUF		4	IO
FDSE		2	Flop & Latch
BUFG		2	Clock

(Utilisation report is also given in the submission.)