COL215 LAB Assignment 3 : 4-Digit 7-Segment Display

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1 Aim

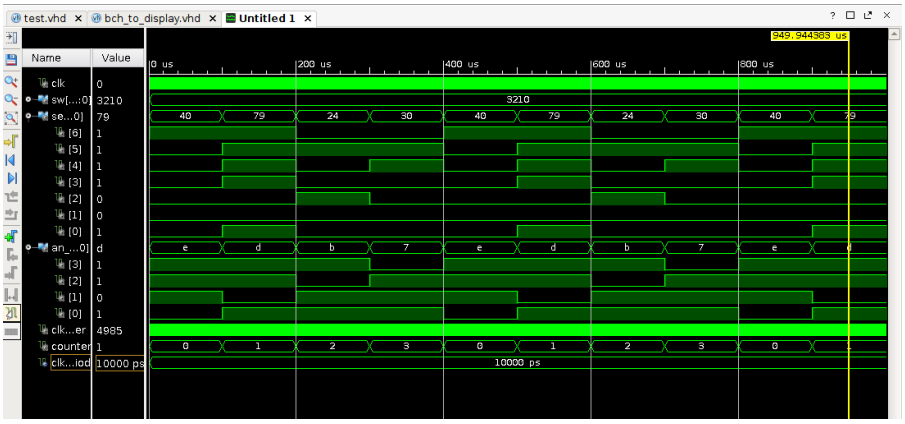
Design and implement a circuit that takes a 4-digit decimal/hexadecimal number from slide switches and displays it on seven segment displays of BASYS3 FPGA board. Use on-board clock and find valid range of refresh rates.

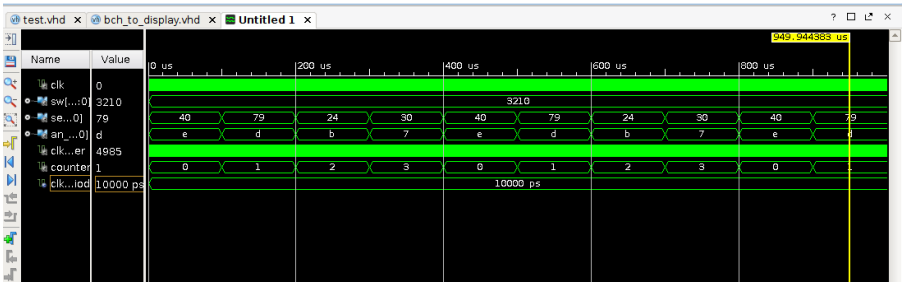
2 Design

The input taken is a 16 bit binary from the 16 slider switches.
This is shown in the hexadecimal format on the seven-segment display.
Also the clock is taken as input from the FPGA board, the clock is of 100MHz frequency.
A counter is made which changes the lighted anode every 10000 clock cycles , i.e, every 0.1ms. So the overall refresh cycle is of 0.4 ms.
We tested the code on the BASYS3 FPGA board by changing this refresh cycle and found that the upper limit of refresh cycle was roughly 20ms(500000 clock cycles per anode) after which the blinking of seven segment display was clearly visible and the lower limit of refresh cycle was roughly 0.02 ms (500 clock cycles per anode) below which there was slight overlap between values shown in different segments.
Multiplexer logic is written using case statements to select the one out of the four anode or switch values based on the counter as a selector.

3 Simulation

The code is simulated on test-bench created by the name test.vhd.





4 Utilisation Report

29 LUT's are used (as logic)
16 registers are used as flip-flops.
28 Input Output Blocks are used (16 switch inputs(sw) and 1 clock input(clk) and 7 segment outputs(seg) and 4 display outputs(an))
1 BUFGCTRL is used (to enable clock)

Ref Name	Used	Functional Category
IBUF	17	IO
FDRE	16	Flop & Latch
LUT1	13	LUT
OBUF	11	IO
LUT4	11	LUT
LUT6	5	LUT
LUT2	4	LUT
CARRY4	4	CarryLogic
LUT5	2	LUT
BUFG	1	Clock

(Utilisation report is also given in the submission.)

5 Running on BASYS3 FPGA Board