COL215 LAB Assignment 4 : Controlling Brightness of 7-Segment Display

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1 Aim

Learn how to control brightness of LED 7-segment displays using pulse width modulation

2 Design

The input taken is a 16 bit binary from the 16 slider switches.

This is shown in the hexadecimal format on the seven-segment display.

There are 4 seven segment displays on which the hexadecimal numbers are displayed. These numbers are not displayed at same brightness.

The displays are kept on for some time and kept off for some other time.

The displays which are on for more time appear brighter than those which were on for less time.

We implemented rotation of digits by using a variable called rotate which increments its value after every fixed duration (roughly 2.6 second in our case). Then we use this value to shift digits by the same value. Rotate goes from 0 to 3 and then back to 0 and the loop continues.
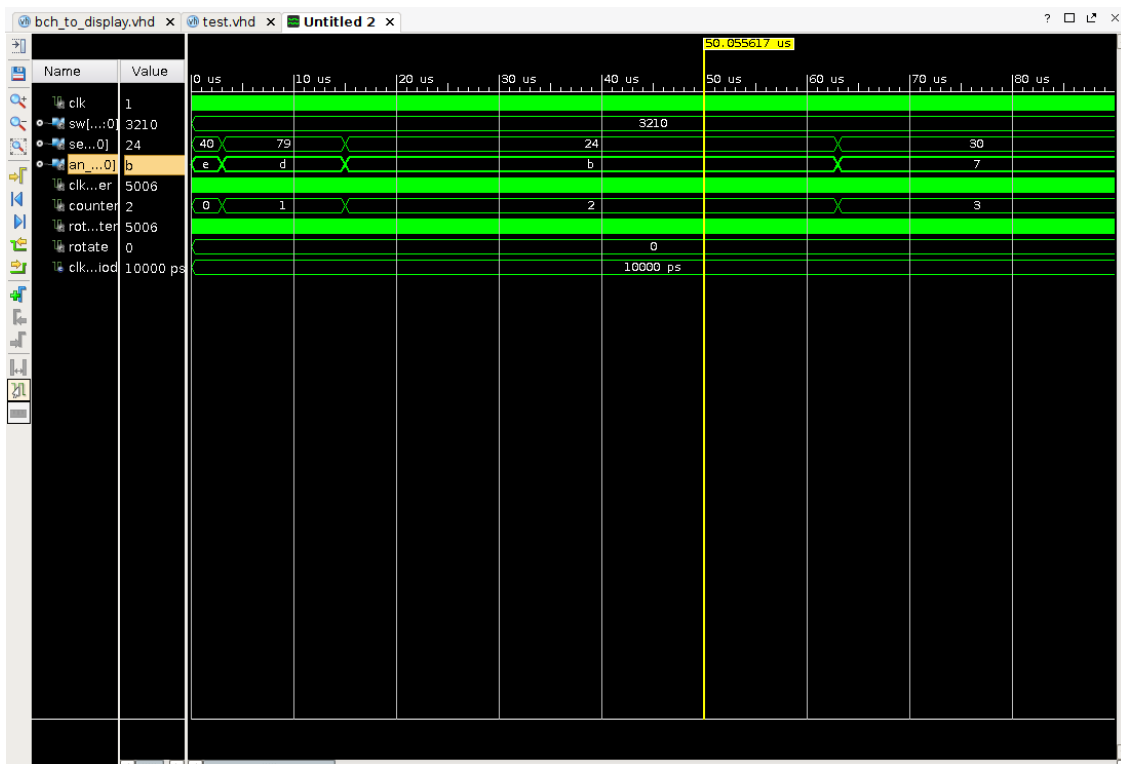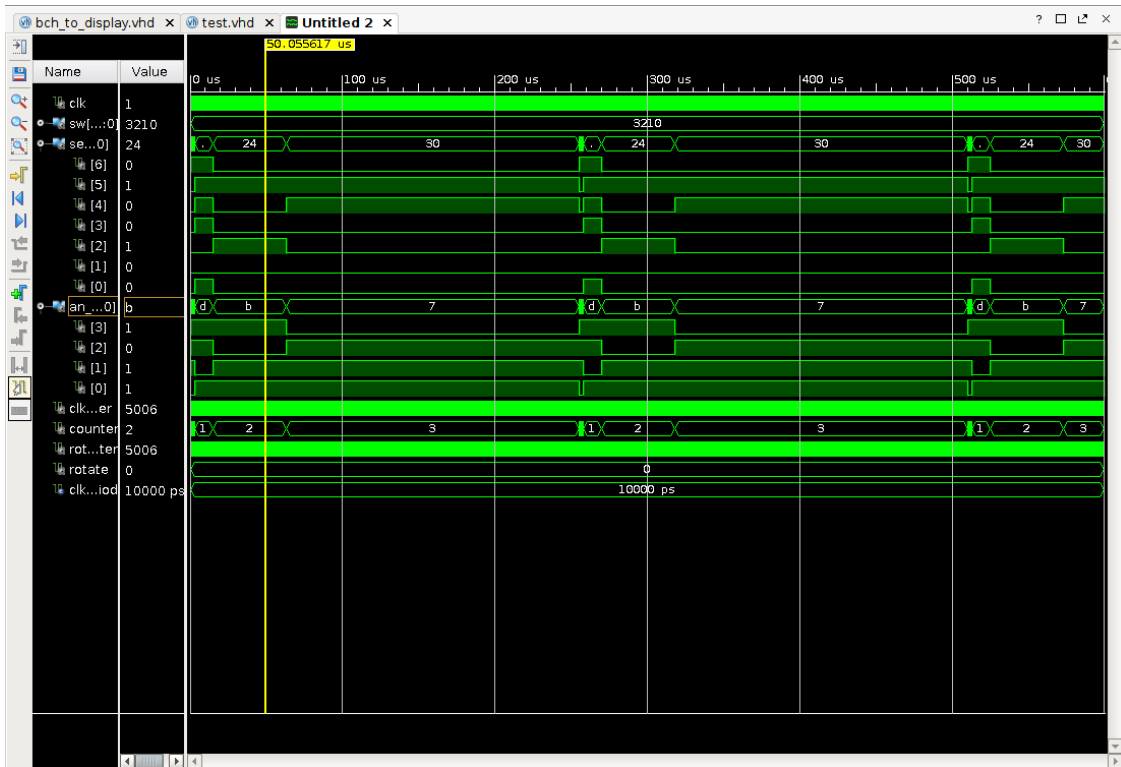
3 Simulation

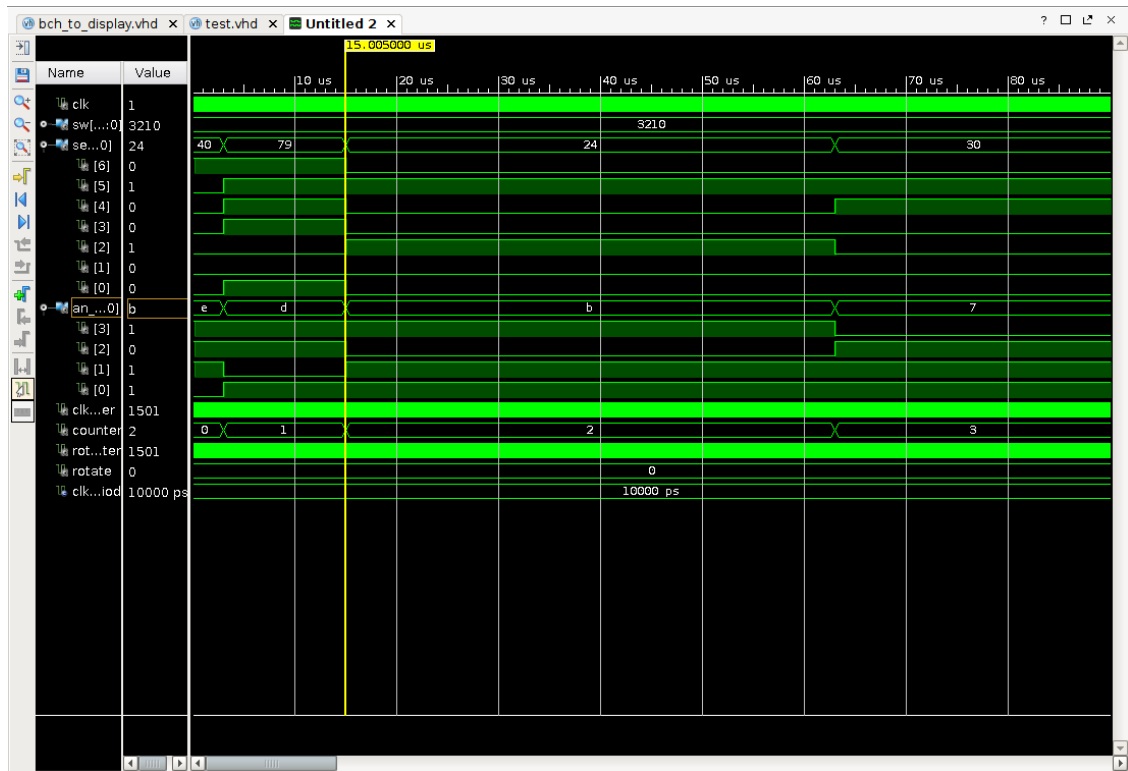The code is simulated on test-bench created by the name test.vhd.
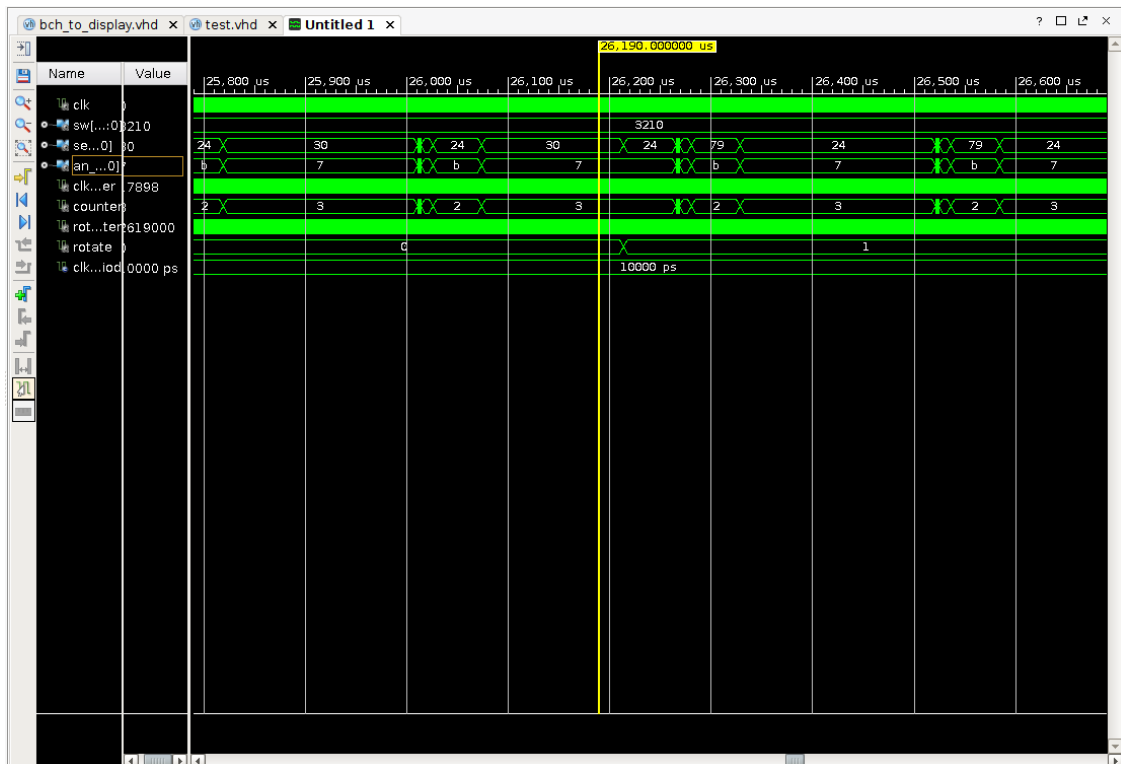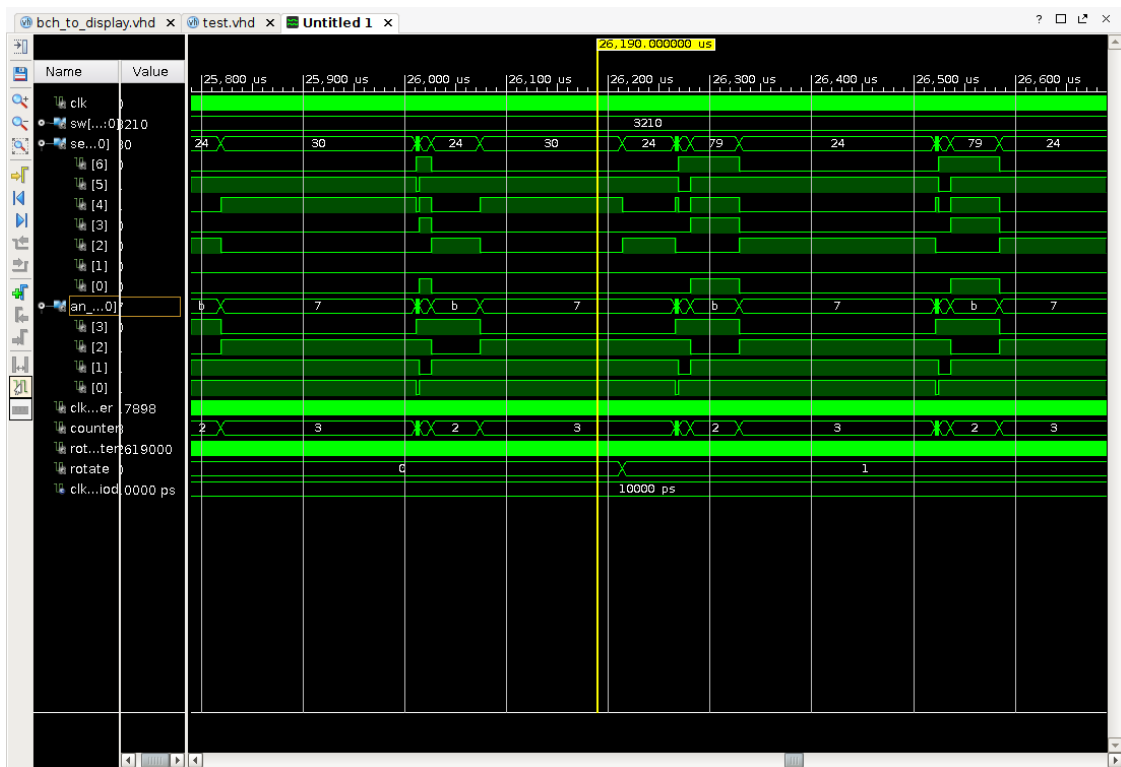
The above two images are showing rotation. For above two images, we changed rotation time to 0.026 seconds instead of 2.6 seconds for faster simulation. The below 4 images are for displaying changing brightness.

4 Utilisation Report

77 LUT's are used (as logic)
47 registers are used as flip-flops.
28 Input Output Blocks are used (16 switch inputs(sw) and 1 clock input(clk) and 7 segment outputs(seg) and 4 display outputs(an))
1 BUFGCTRL is used (to enable clock)

```
+----------+------+--------------------+
| Ref Name | Used | Functional Category |
+----------+------+--------------------+
| FDRE     |  47  |       Flop & Latch |
| LUT1     |  41  |                LUT |
| LUT4     |  17  |                LUT |
| IBUF     |  17  |                 IO |
| LUT6     |  13  |                LUT |
| OBUF     |  11  |                 IO |
| CARRY4   |  11  |         CarryLogic |
| LUT5     |   7  |                LUT |
| LUT2     |   6  |                LUT |
| LUT3     |   4  |                LUT |
| BUFG     |   1  |              Clock |
+----------+------+--------------------+
```

(Utilisation report is also given in the submission.)

5 Running on BASYS3 FPGA Board