CHAPTER 1

INTRODUCTION

1.1 Introduction:

An inverter is basically a device that converts electrical energy of DC form into that of AC. The purpose of DC-AC inverter is to take DC power from a battery source and converts it to AC. For example the household inverter receives DC supply from 12V or 24V battery and then inverter converts it to 240V AC with a desirable frequency of 50Hz or 60Hz. These DC-AC inverters have been widely used for industrial applications such as uninterruptible power supply (UPS), AC motor drives. Recently, the inverters are also playing an important role in various renewable energy applications as these are used for grid connection of Wind Energy System or Photovoltaic System. In addition to this, the control strategies used in the inverters are also similar to those in DC-DC converters. Both current-mode control and voltage-mode control are employed in practical applications [1].

The DC-AC inverters usually operate on Pulse Width Modulation (PWM) technique. The PWM is a very advance and useful technique in which width of the Gate pulses are controlled by various mechanisms [2]. PWM inverter is used to keep the output voltage of the inverter at the rated voltage (depending on the user's choice) irrespective of the output load .In a conventional inverter the output voltage changes according to the changes in the load. To nullify this effect of the changing loads, the PWM inverter correct the output voltage by changing the width of the pulses and the output AC depends on the switching frequency and pulse width which is adjusted according to the value of the load connected at the output so as to provide constant rated output. The inverters usually operate in a pulse width modulated (PWM) way

and switch between different circuit topologies, which means that the inverter is a nonlinear, specifically piecewise smooth system. In addition to this, the control strategies used in the inverters are also similar to those in DC-DC converters. Both current-mode control and voltage-mode control are employed in practical applications.

In the last decade, studies of complex behaviour in switching power converters have gained increasingly more attention from both the academic community and industry. Various kinds of nonlinear phenomena, such as bifurcation, chaos, border collision and coexisting attractors, have been revealed.

1.2 Literature Review:

1.2.1 Voltage Source Inverter and Current Source Inverter

1.2.1.1 Voltage Source Inverter: The type of inverter where the independently controlled ac output is a voltage waveform. The output voltage waveform is mostly remaining unaffected by the load [1]. Due to this property, the VSI have many industrial applications such as adjustable speed drives (ASD) and also in Power system for FACTS (Flexible AC Transmission).

1.2.1.2 Current Source Inverter: The type of inverter where the independently controlled ac output is a current waveform. The output current waveform is mostly remaining unaffected by the load. These are widely used in medium voltage industrial applications, where high quality waveform is required.

1.2.2 Single Phase Half Bridge and Full Bridge VSI Inverter:

1.2.2.1 Single Phase Half Bridge Inverter: It consists of two semiconductor switches T1 and T2. These switches may be BJT, Thyristor and IGBT etc. with a commutation circuit. D1 and D2 are called Freewheeling diode also known as the Feedback diodes as they feedback the load reactive power. T1 is ON during the positive half cycle of the output voltage, which makes Vout=Vo/2 and T2 is ON during

the negative half cycle which makes Vout= -Vo/2. The both switches must operate alternatively otherwise there may be a chance of short circuiting. In case of resistive load, the current waveform follows the voltage waveform but not in case of reactive load. The feedback diode operates for the reactive load when the voltage and current are of opposite polarities.

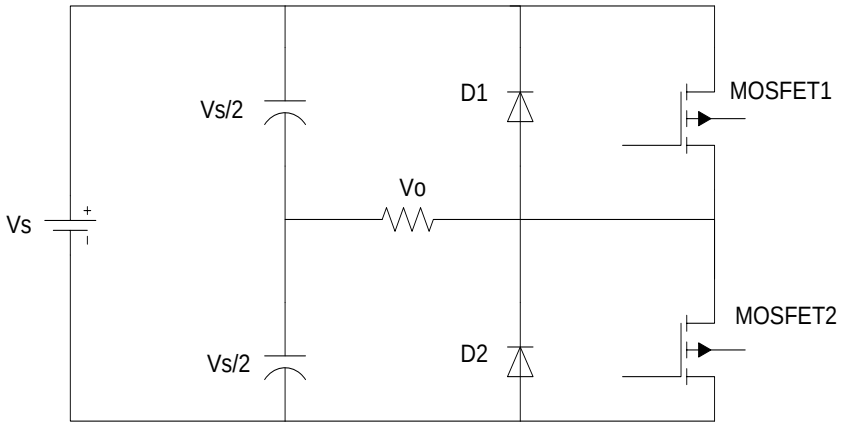

Fig 1.2.2.1: Single Phase Half Bridge Inverter

MOSFET1	MOSFET2	Vo
On	Off	Vs/2
Off	On	-Vs/2

Table 1.2.2.1: Switching States of single phase half bridge inverter

1.2.2.2 Single Phase Full wave Bridge Inverter: It consists of two arms with a two semiconductor switches on both arms with antiparallel freewheeling diodes for discharging the reverse current. In case of resistive-inductive load, the reverse load current flow through these diodes. These diodes provide an alternate path to inductive current which continue so flow during the Turn OFF condition [3].

The switches are T1, T2, T3 and T4. The switches in each branch is operated alternatively so that they are not in same mode (ON /OFF) simultaneously .In practice they are both OFF for short period of time called blanking time, to avoid short circuiting. The switches T1 and T2 or T3 and T4 should operate in a pair to get

the output. These bridges legs are switched such that the output voltage is shifted from one to another and hence the change in polarity occurs in voltage waveform. If the shift angle is zero, the output voltage is also zero and maximal when shift angle is π.

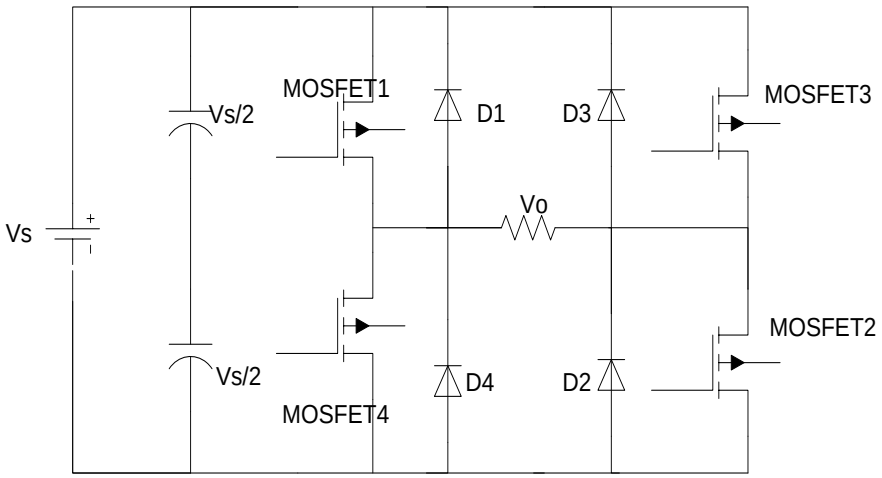

Fig 1.2.2.1: Single Phase Full Bridge Inverter

MOSFET1	MOSFET2	MOSFET3	MOSFET4	Vo
On	Off	Off	On	Vs
Off	On	On	Off	-Vs
On	Off	On	Off	0
Off	On	Off	On	0

Table 1.2.2.1: Switching States of single phase half bridge inverter

1.2.3 Inverter Types:

There are generally three types of inverter for general purpose

1. Square Wave Inverter
2. Modified Square Wave Inverter
3. True Sine Wave Inverter

Square Wave Inverter: This is the basic type of inverter. Its output is a alternating square wave. The harmonic content in this wave is very large. This inverter is not efficient and can give serious damage to some of the electronic equipment. But due to low cost, it has some limited number of applications in household appliances.

True Sine Wave Inverter: This type of inverter provides output voltage waveform which is very similar to the voltage waveform that is received from the Grid. The sine wave has very little harmonic distortion resulting in a very „clean" supply and makes it ideal for running electronic systems such as computers, digital fx racks and other sensitive equipment without causing problems or noise. Things like mains battery chargers also run better on pure sine wave converters.

1.2.4 Benefits of using True Sine Wave Inverter:

1. Most of the electrical and electronic equipment are designed for the sine wave.
2. Some appliances such as variable motor, refrigerator, microwave will not be able to provide rated output without sine wave.
3. Electronic clocks are designed for the sine wave.
4. Harmonic content is less.

1.2.5 Sine Wave Generation:

The most common and popular technique for generating True sine Wave is Pulse Width Modulation (PWM). Sinusoidal Pulse Width Modulation is the best technique for this. This PWM technique involves generation of a digital waveform, for which the duty cycle can be modulated in such a way so that the average voltage waveform corresponds to a pure sine wave. The simplest way of producing the SPWM signal is through comparing a low power sine wave reference with a high frequency triangular wave. This SPWM signal can be used to control switches. Through an LC filter, the output of Full Wave Bridge Inverter with SPWM signal will generate a wave

approximately equal to a sine wave. This technique produces a much more similar AC waveform than that of others. The primary harmonic is still present and there is relatively high amount of higher level harmonics in the signal.

Let the modulating signal is a sinusoidal of amplitude Am, and the amplitude of the triangular carrier is Ac, the ratio m=Am/Ac is known as Modulation Index (MI). Note that controlling the MI controls the amplitude of the applied output voltage. A higher carrier frequency results in large number of switching per cycle and hence increased power loss.

The inverting process works well for m<1 and for m>1, there are periods of the triangle wave in which there is no intersection of carrier and the signal as shown in the fig. However, a certain amount of this "over modulation" is often allowed in the interest of obtaining a large AC voltage magnitude even though the spectral content of the voltage is poor.

Amplitude Modulation Index: This is the ratio of peak voltage of modulating and carrier signal (triangular wave).

$$M_a = \frac{Peak\ value\ of\ Mod.Signal}{Peak\ value\ of\ carrier\ signal}$$

Frequency Ratio: It is defined as ratio of frequency of carrier wave and modulating wave.

$$M_f = \frac{frequency\ of\ Mod.Signal}{frequency\ of\ carrier\ signal}$$

On mathematical analysis, It can be found that only following harmonics are present in output current:

Nw_c+Mw_m such that N+M are odd

For higher order frequencies, current will be very small due to large inductances. When m_a >1: it leads to a situation called over modulation and when it becomes too high, then we just get square wave.

1.2.6 SPWM Harmonic Elimination:

The SPWM waveform has harmonics of several orders in the phase voltage waveform , the dominant ones are the fundamental and other of order of n and n±2

where n=fc/fm. With the method of Selective Harmonic Elimination, only selected harmonics are eliminated with the smallest number of switching. For a single phase-SPWM waveform with odd and half wave symmetry and n chops per cycle.

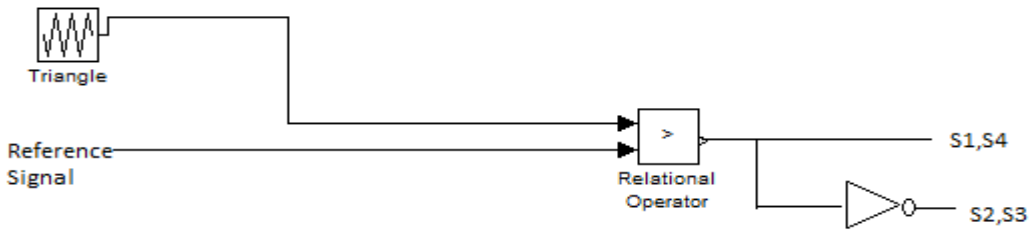

Fig 1.2.6.1: SPWM Control Strategy

SPWM is considered as the best PWM technique for the reasons mentioned below.

Advantages of SPWM:

1. Low power consumption.
2. High energy efficient upto 90%.
3. High power handling capability.
4. No temperature variation-and ageing-caused drifting or degradation in linearity.
5. Easy to implement and control.
6. Compatible with today's digital microprocessors

Disadvantages of SPWM:

1. Attenuation of the wanted fundamental component of the waveform.
2. Drastically increased switching frequencies that leads to greater stresses on associated switching devices and therefore de-rating of those devices.
3. Generation of high-frequency harmonic components.

1.2.7 Hysteresis Current Control (HCC):

In Hysteresis current control two current references are needed with a certain bandwidth. According to this control technique, the switch is turned on when the inductor current goes below the lower reference Iv,ref and turned off when the inductor current above the upper reference Ip,ref. Thus the current is made to oscillate between the two current references. HCC results in variable frequency operation. Also with this control technique the converter works in CICM.

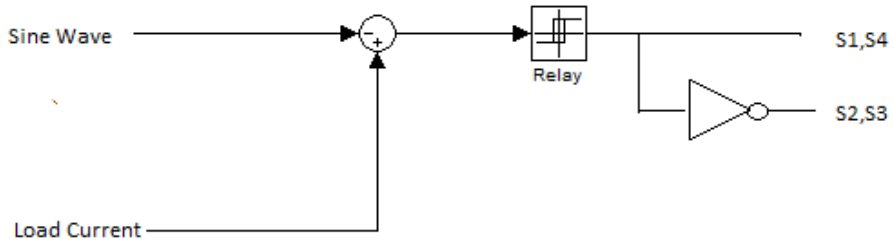

Fig 1.2.7.1: Hysteresis Current Controller Control Strategy

Advantages of HCC:

-no need of compensation ramp;

-low distorted input current waveforms

Disadvantages of HCC:

-variable switching frequency

-dead band near zero crossing due to high switching frequency

1.2.8 Generation of Reference Signal

The reference signal for the Pulse Width Modulation is generated as follows:

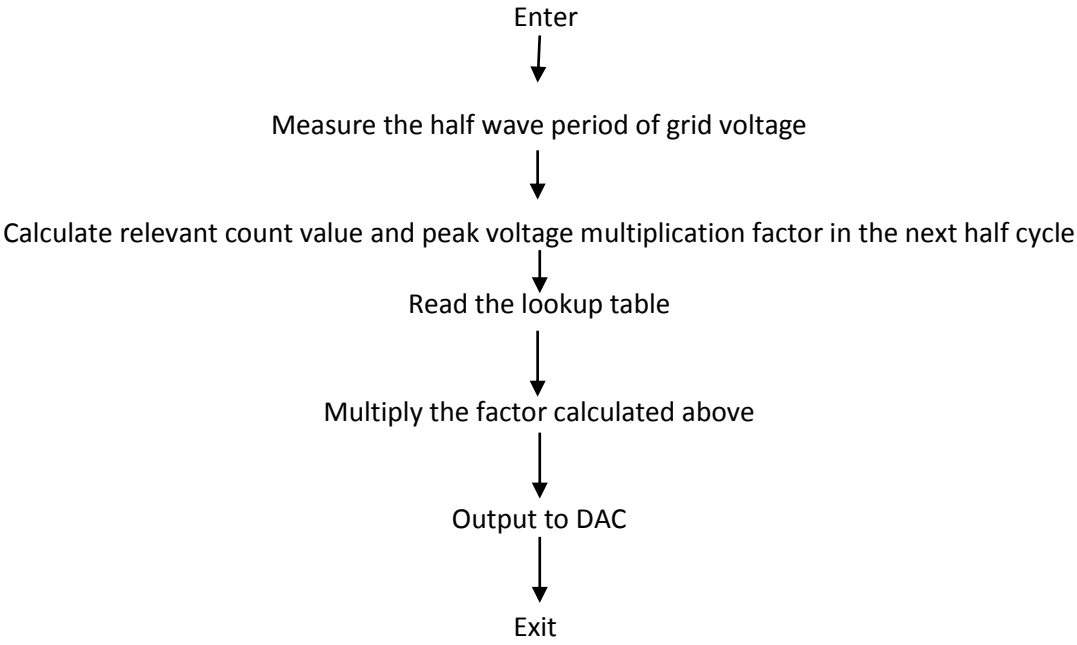

Fig 1.2.8.1: Flow chart for reference signal generation

1.2.9 Control Strategies

The operation power control unit between the source of power generation and the grid depends upon the characteristics of the power generation source. The power control unit can be either a single stage or multi-stage converter. The single stage converters have inherent advantage of higher efficiency, high reliability and compactness.

There are number of strategies for inverters feeding power to the grid based on the different control techniques. Two of the strategies with higher efficiency, necessary isolation between the grid and the source and with minimum harmonic injection into the grid are discussed below:

Transformerless grid tie inverter Transformerless photovoltaic (PV) grid-connected inverters have the advantages of higher efficiency, lower cost, less

complexity, and smaller volume compared to their counterparts with transformer galvanic isolation. High frequency common-mode (CM) voltages must be avoided for a transformerless PV grid-connected inverter because it will lead to a large charge/discharge current partially flowing through the inverter to the ground. This CM ground current will cause an increase in the current harmonics, higher losses, safety problems, and electromagnetic interference (EMI) issues [5][6].

For a grid-connected PV system, energy yield and payback time are greatly dependant on the inverter's reliability and efficiency, which are regarded as two of the most significant characteristics for PV inverters. A number of topologies to control the CM leakage current and to obtain high efficiency with great reliability have been proposed. Some of them are H5, H6 and dual-buck paralled inverter configuration. In order to minimize the ground leakage current and improve the efficiency of the converter system, transformerless PV inverters utilizing unipolar PWM control have been presented.

Fig 1.2.9.1 shows the circuit diagram of the proposed transformerless PV inverter, which is composed of six MOSFETs switches (S1–S6), six diodes (D1–D6), and two split ac-coupled inductors *L*1 and *L*2. The diodesD1–D4 performs voltage clamping functions for active switches S1–S4. The ac-side switch pairs are composed of S5, D5 and S6, D6, respectively, which provide unidirectional current flow branches during the freewheeling phases decoupling the grid from the PV array and minimizing the CM leakage current.

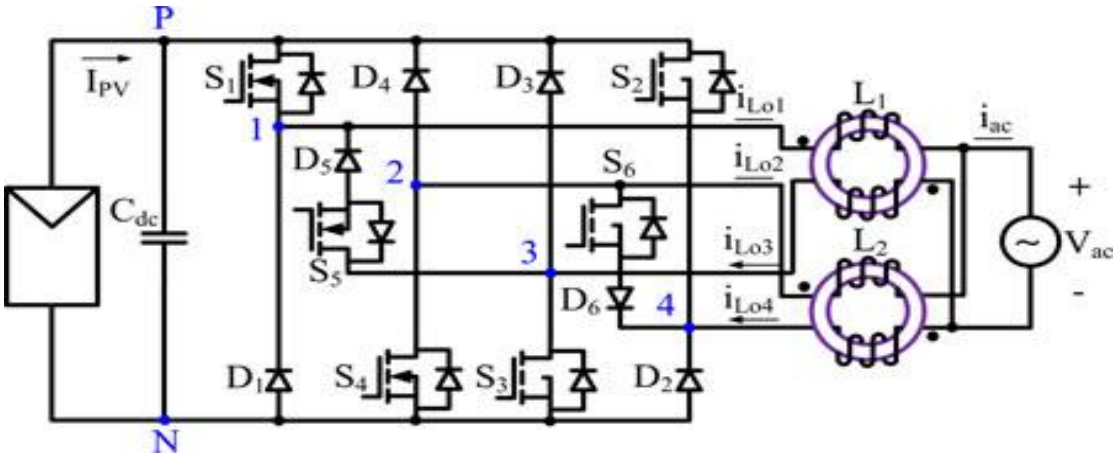

Fig 1.2.9.1: High efficiency and reliability PV transformerless inverter topology

Fig 1.2.9.2 illustrates the PWM scheme for the proposed inverter. When the reference signal control is higher than zero, MOSFETs S1 and S3 are switched simultaneously in the PWM mode and S5 is kept on as a polarity selection switch in the half grid cycle; the gating signals G2, G4, and G6 are low and S2, S4 and S6 are inactive. Similarly, if the reference signal –Vcontrol is higher than zero, MOSFETs S2 and S4 are switched simultaneously in the PWM mode and S6 is on as a polarity selection switch in the grid cycle; the gating signals G1, G3, and G5 are low and S1, S3 , and S5 are inactive.

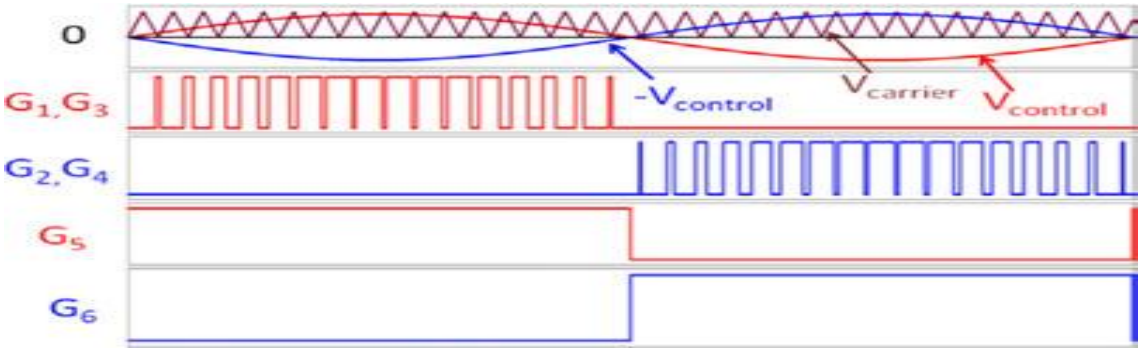

Fig 1.2.9.2: Gating signals of the proposed transformerless PV inverter[5]

In the positive half-line grid cycle, the high-frequency switches S1 and S3 are modulated by the sinusoidal reference signal $V_{control}$ while S5 remains turned ON. When S1 and S3 are ON, diode D5 is reverse-biased, the inductor currents of i_{Lo1} and i_{Lo3} are equally charged, and energy is transferred from the dc source

to the grid; when S1 and S3 are deactivated, the switch S5 and diode D5 provide the inductor current i_{L1} and i_{L3} a freewheeling path decoupling the PV panel from the grid to avoid the CM leakage current coupled-inductor *L*2 is inactive in the positive half-line grid cycle. Similarly, in the negative half cycle, S2 and S4 are switched at high frequency and S6 remains ON. Freewheeling occurs through S6 and D6.

Single Stage Boost/Buck Boost Inverter The operation of a PCU depends upon the voltage magnitude and characteristics of the source being interfaced to the grid. Depending on the voltage level, the PCU may be required to "buck" or "boost" the available dc voltage to meet the grid voltage requirements. In addition to this, it should also condition the available dc power into high quality ac required to perform specific functions such as reactive power control and maximum power point tracking (MPPT).

Buck-Boost Operation These configurations feed sinusoidal power into the grid with lower total harmonic distortion (THD) in the grid current and interface nicely with the grid. They also provide an inherent isolation1 between the source and the grid in the sense that there is an inductor that stores the energy from the source during switch-ON interval and delivers it to the grid during OFF interval without any direct connection between the source and the grid. However, the buck–boost inverter configurations suffer from high peak inductor current stress which is a result of the fact that the entire energy that is transferred to the grid in a switching cycle is stored in the inductor during the ON time of the switching cycle and only this stored energy is supplied to the grid during the OFF time of the switching cycle. This restricts its use to low power applications.

Boost Operation The boost inverter operation renders reduced peak inductor current. Here, the dc source and the boost inductor supply energy to the load when the main switch is OFF. Hence, there is no isolation1 between the source and the grid in case of a boost inverter. It is important to note that the boost operation alone is not feasible for grid connected applications. Boost operation comes into picture only at the instant when grid voltage exceeds the dc source voltage else the converter operates in Buck Boost mode [7].

The proposed configuration is capable of operating with a variety of input sources and is compatible with a wide range of input dc voltage.

Boost	I	ON	OFF	ON	OFF	ON	ON	OFF
	II	ON	ON	OFF	OFF	ON	ON	OFF
	III	X	X	OFF	OFF	X	OFF	OFF
Buck-Boost	I	ON	OFF	ON	OFF	ON	ON	OFF
	II	ON	ON	OFF	OFF	OFF	OFF	ON
	III	X	X	OFF	OFF	OFF	OFF	OFF

Table 1.2.9.1: Here operation in the boost and buck-boost mode is summarised

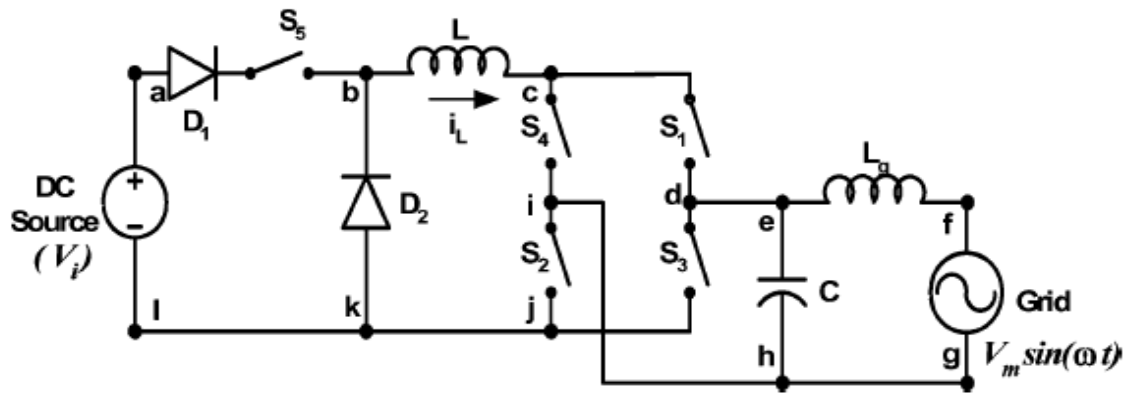

Fig 1.2.9.3: Buck Boost/Boost grid tie inverter

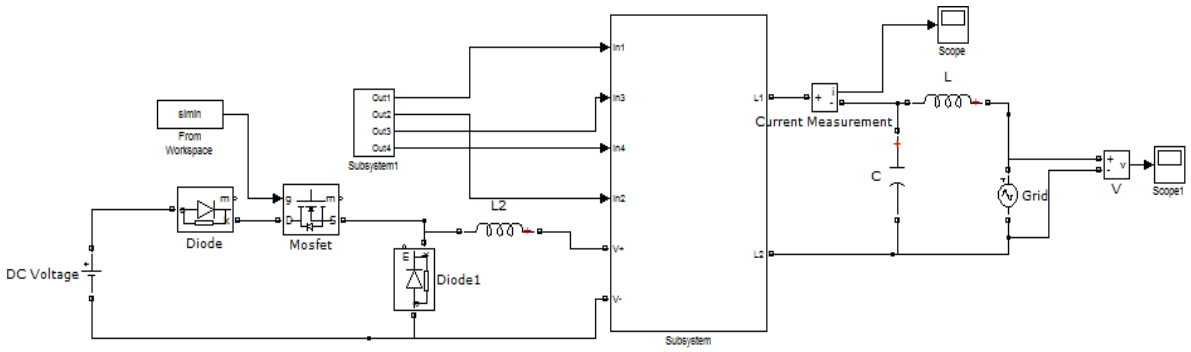

Fig 1.2.9.4(a)

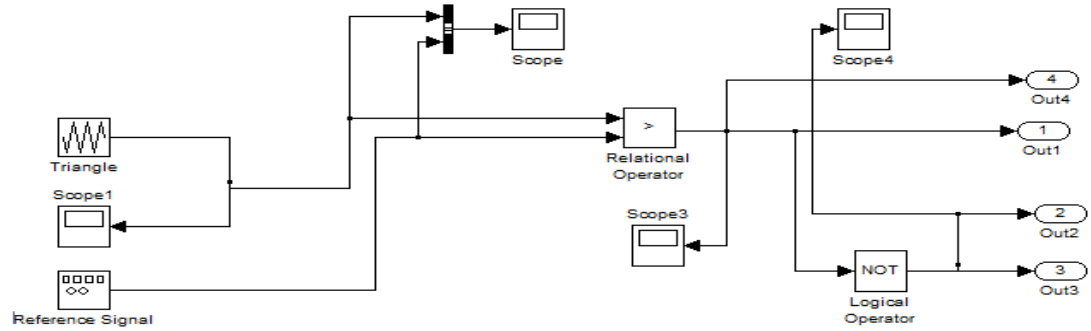

Fig 1.2.9.4(b) Subsystem

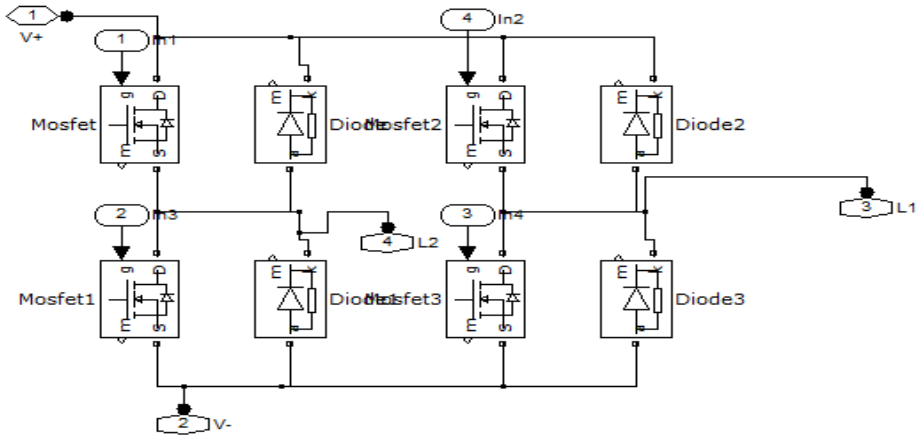

Fig 1.2.9.4(c) Subsystem

Fig 1.2.9.4: Here, Simulink model of transformerless inverter topology is presented

1.3 A Sample PV array used in Industry

The 100-kW PV array as shown below uses 330 SunPower modules (SPR-305). The array consists of 66 strings of 5 series-connected modules connected in parallel (66*5*305.2 W= 100.7 kW). Manufacturer specifications for one module are:

- Number of series-connected cells : 96
- Open-circuit voltage: Voc= 64.2 V
- Short-circuit current: Isc = 5.96 A
- Voltage and current at maximum power : Vmp =54.7 V, Imp= 5.58 A

The characteristics of the SunPower-SPR305 array are reproduced below.

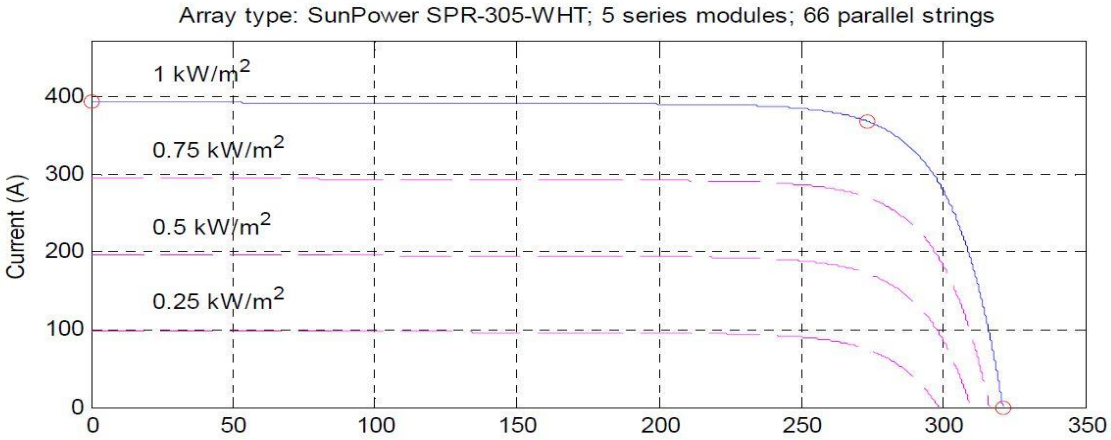

Fig 1.3.1: V-I characteristics of solar panel under different solar insolation [http://www.solardesigntool.com/components/module-panel-solar/Sunpower/52/SPR-305-WHT/specification-data-sheet.html]

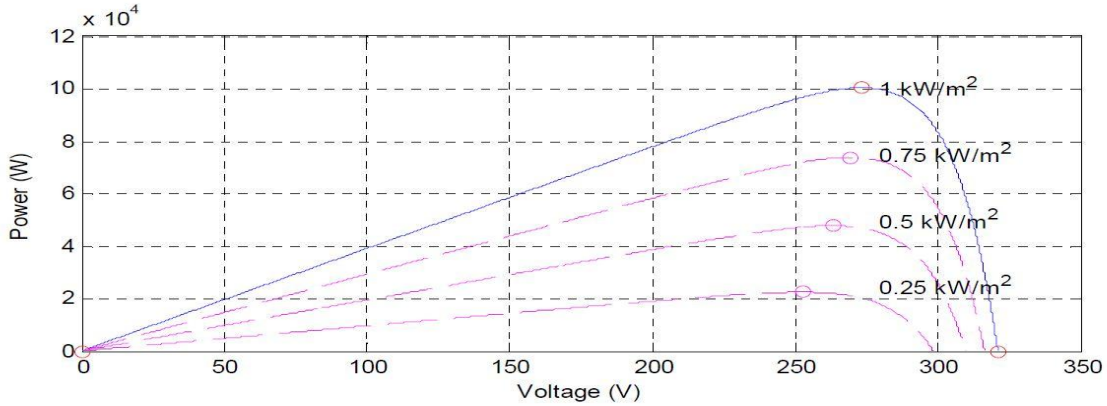

Fig 1.3.2: P-V characteristics of solar panel under different solar insolation [http://www.solardesigntool.com/components/module-panel-solar/Sunpower/52/SPR-305-WHT/specification-data-sheet.html]

In fig 1.3.2 Red dots on blue curves indicate module manufacturer specifications (Voc, Isc, Vmp, Imp) under standard test conditions (25 degrees Celsius, 1000 W/m2). The control circuit contains the maximum power point tracking (MPPT) block, current control, and the synchronizing block. The MPPT mechanism observes the voltage and current output of the PV module, which continuously vary according to the temperature and irradiance level. An incremental conductance algorithm is used, based on the condition that at the point of maximum power, the rate of change of output power to the array voltage is zero, as shown below:-

$$\frac{dP}{dv} = 0$$

$$\frac{dP}{dv} = \frac{d(vi)}{dv} = i + v\frac{di}{dv} = 0$$

$$i + v\frac{di}{dv} = 0$$

$$i + v\frac{\Delta i}{\Delta v} = 0$$

$$\frac{\Delta i}{\Delta v} = -\frac{i}{v}$$

A flowchart of the incremental conductance is given in Figure 1.3.3.

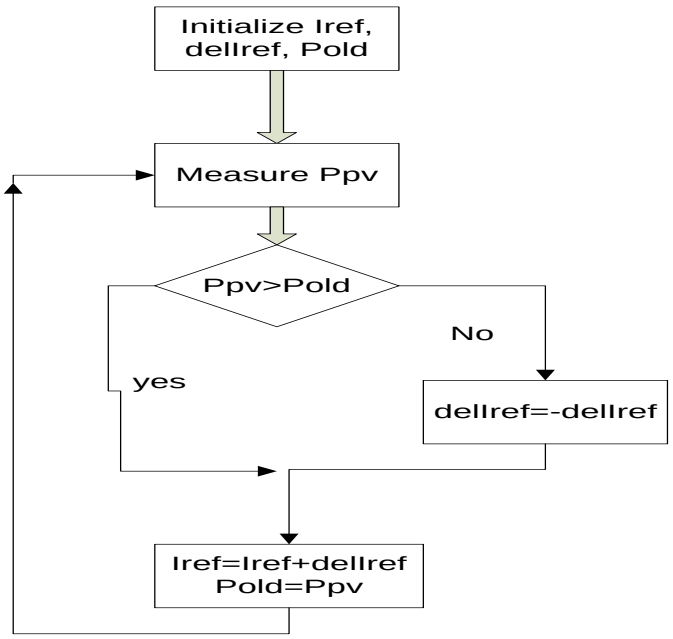

Fig 1.3.3 Flow diagram of MPPT Algorithm

1.4 Project Description:

In Voltage Source Inverters (VSI), there are many mechanisms by which the power flow between GCI and grid can be controlled. The basic mechanism is through the control of switching instance of inverter so as to produce a fundamental 50 Hz voltage in the output of inverter. In this method, the power flow is controlled by adjusting the amplitude and phase of inverter output voltage relative to the line voltage. Since the grid is invariably a rigid voltage source with very low line impedance, power flow from the inverter to the grid, reduces to being simply current flow control and voltage source inverters have been proposed for use as current sources in number of applications. Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse-width modulation control used within an inverter. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. This is the most popular method of controlling the output voltage and this method is

termed as Pulse-Width Modulation (PWM) Control. A high frequency signal is compared with a specific sinusoidal signal with specific frequency. The high-frequency signal is known as carrier or modulator signal. The carrier can be a triangular form generate a train of pulses (PWM) aligned, this minimizes: noises in the system, ripple current, harmonics distortion acoustic noise. In the SPWM the reference signal is a sinusoidal. The comparison of this signal with a triangular generates the system output.

In hysteresis current control, hysteresis band determines the switching frequency of inverter. If fixed hysteresis band current control be used, switching frequency of the inverter will not be constant during a one cycle. Conventional hysteresis current control operates by comparing a current error against fixed hysteresis bands. When the error exceeds the upper hysteresis band, the inverter output is switched low, and when the error falls below the lower hysteresis band, the inverter output switches high. This process is usually implemented using two level switching so that each phase leg output is the mirror image of the other.

CHAPTER 2

METHODOLOGY

2.1 Introduction to Grid Connection

A grid-tie inverter (GTI) or synchronous inverter is a special type of power inverter that converts direct current (DC) electricity into alternating current (AC) and feeds it into an existing electrical grid. GTIs are often used to convert direct current produced by many renewable energy sources, such as solar panels or small wind turbines, into the alternating current used to power homes and businesses.

The increasing concern about the available fossil fuel reserves and the environmental aspects has given a high impetus to the use of renewable energy sources in the present scenario of power generation.

The grid-tied inverter differs from the stand-alone variety in that the control circuit has to be able to operate in the presence of the existing grid voltage and force the grid to accept power instead of providing it. Because the grid is essentially a very low impedance voltage source, the inverter must be able to act as a current source, only allowing the desired amount of current to be sent into the grid. This process requires close control of the inverter output voltage. Generally, the inverter will control its bulk DC input voltage and use this to determine the output power level. The power level signal is then used to determine the output power, and the inverter output will be adjusted upward until this amount of power is delivered to the grid.

Basic Operation Conditions

1. GTI takes DC power and inverts it to AC.
2. The grid tie inverter must synchronize its frequency with that of the grid (e.g. 50 or 60 Hz). A stepped-down voltage from the grid will be sampled and used

to generate the SPWM signal. Thus the frequency of the output voltage from the GTI will have the same frequency as the grid. Another possibility is to generate the sine wave from an analog oscillator or from a micro-controller. Switching/SPWM the control strategy is used to switch the IGBTs/MOSFETs present in the H-Bridge, to convert the DC input to AC.

3. A high-quality GTI should have a close to unity power factor.
4. The output voltage from the GTI should be slightly higher than the grid voltage in order to enable the transmission of power from GTI to the grid.
5. The output from the H-Bridge is not a perfect sine wave, therefore, it is passed on to the Filtering stage. Filtering is done to get a perfect sine wave that can be fed to the load as well as into the Grid. For this purpose, we use a Low Pass LC filter at the output side of the Power Circuit. This filter reduces the Harmonic Content in the Signal and also provides a smoother form of a signal. Anti-Islanding Protection To make our device compliant with the safety requirements of utility companies we plan on adding a mechanism that disconnects the inverter from the grid if the grid shuts down. These protections eliminate the chance that a distributed generation system will inject power into the disconnected utility wires or switchgear and cause a hazard to utility personnel.
6. The total harmonic distortion (THD) should be less than 5%.

ISSUE	IEC61727 [3]	IEEE1547 [5]	EN61000-3-2 [4]
Nominal power	10 kW	30 kW	16 A × 230 V = 3.7 kW
Harmonic currents (Order – h) Limits	(3-9) 4.0% (11-15) 2.0% (17-21) 1.5% (23-33) 0.6%	(2-10) 4.0% (11-16) 2.0% (17-22) 1.5% (23-34) 0.6% (> 35) 0.3%	(3) 2.30 A (5) 1.14 A (7) 0.77 A (9) 0.40 A (11) 0.33 A (13) 0.21 A (15-39) 2.25/h
	Even harmonics in these ranges shall be less than 25% of the odd harmonic limits listed.		Approximately 30% of the odd harmonics -see standard.
Maximum current THD	5.0%		-
Power factor at 50% of rated power	0.90	-	
DC current injection	Less than 1.0% of rated output current.	Less than 0.5% of rated output current.	< 0.22 A -corresponds to a 50 W half-wave rectifier.
Voltage range for normal operation	85% - 110% (196 V – 253 V)	88% - 110% (97 V – 121 V)	-
Frequency range for normal operation	50 ± 1 Hz	59.3 Hz to 60.5 Hz	-

Table 2.1.1: SUMMARY OF THE MOST INTERESTING STANDARDS DEALING WITH INTERCONNECTIONS OF PV SYSTEMS TO THE GRID

2.2 Solar Cell modelling

PV cell are made of semiconductors materials. Semiconductor material absorbs photons and converts photons having sufficiently high energy into hole-electron pairs. A standard electrical circuit model consists of a photon generation current Io proportional to solar irradiation in parallel with a diode. The cell short circuit current Isc is proportional to the number of absorbed photons. The cell open-circuit voltage

Voc depends on the semiconductor diode characteristic. The maximum output power is obtained when the cell operates at the peak power point.

The model of the solar cell can be realized by an equivalent circuit that consist of a current source in parallel with a diode. The current source represents the current generated by photons (often denoted as Iph or IL), and its output is constant under constant temperature and constant incident radiation of light. Rs and Rsh components can be neglected for the ideal model. It can be used to demonstrate the illumination and temperature effect on PV cells and to study and experience the need of MPPT algorithms.

Maximum power point tracking (MPPT) is a technique/ algorithm that grid-tie inverters use to get the maximum possible power from one or more photovoltaic devices, typically solar panels under certain conditions. The voltage at which PV module can produce maximum power is called 'maximum power point' (or peak power voltage). Maximum power varies with solar radiation, ambient temperature and solar cell temperature. Solar cells have a complex relationship between solar irradiation, temperature and total resistance that produces a non-linear output efficiency known as the I-V curve. It is the purpose of the MPPT system to sample the output of the cells and apply the proper resistance (load) to obtain maximum power for any given environmental conditions.

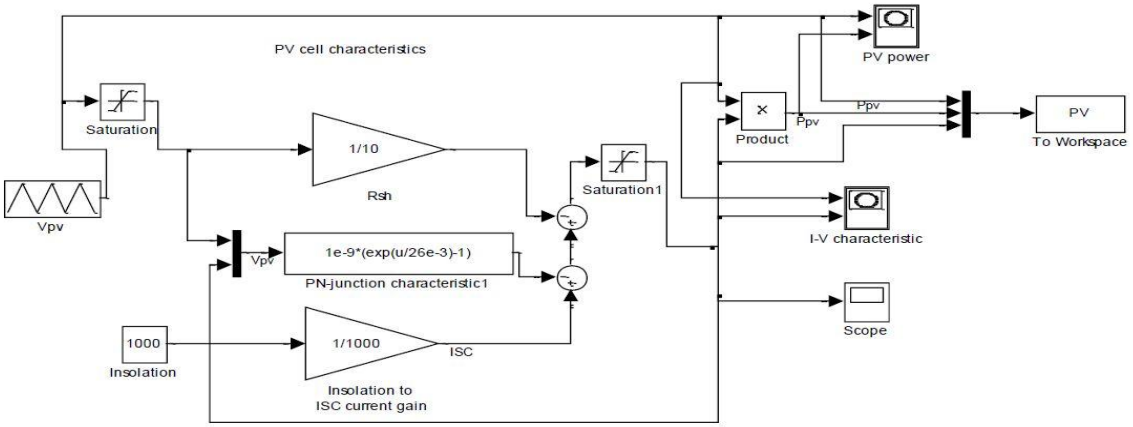

Fig 2.2.1: Simulink model of solar cell

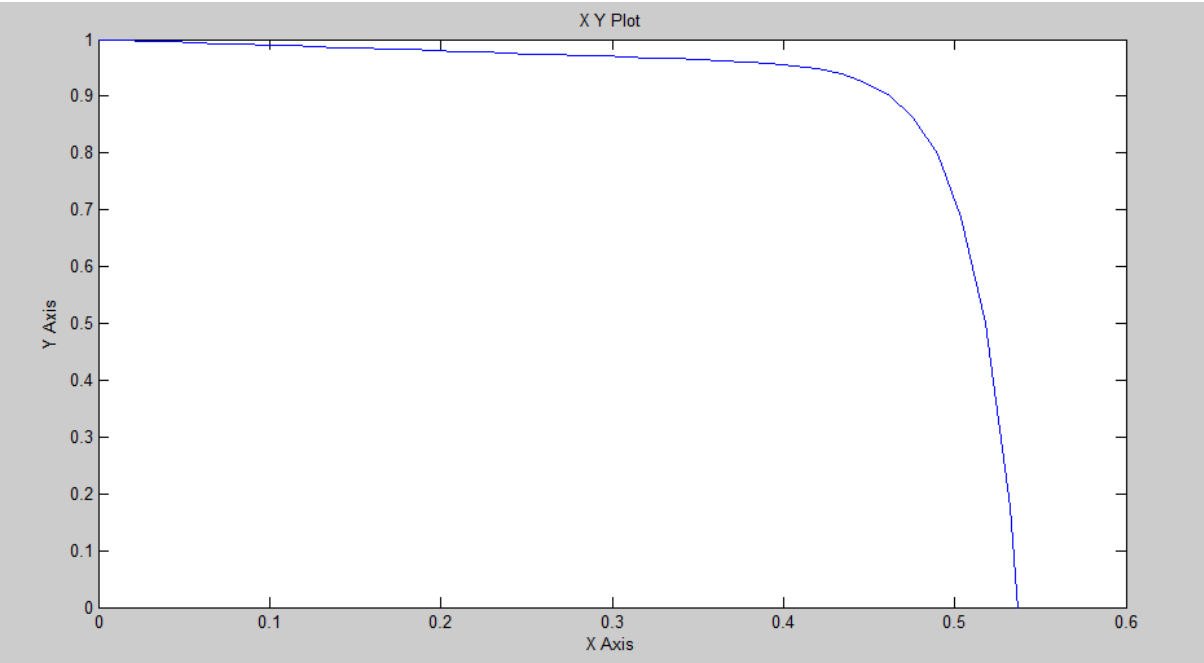

Fig 2.2.2: I-V characteristics Solar cell

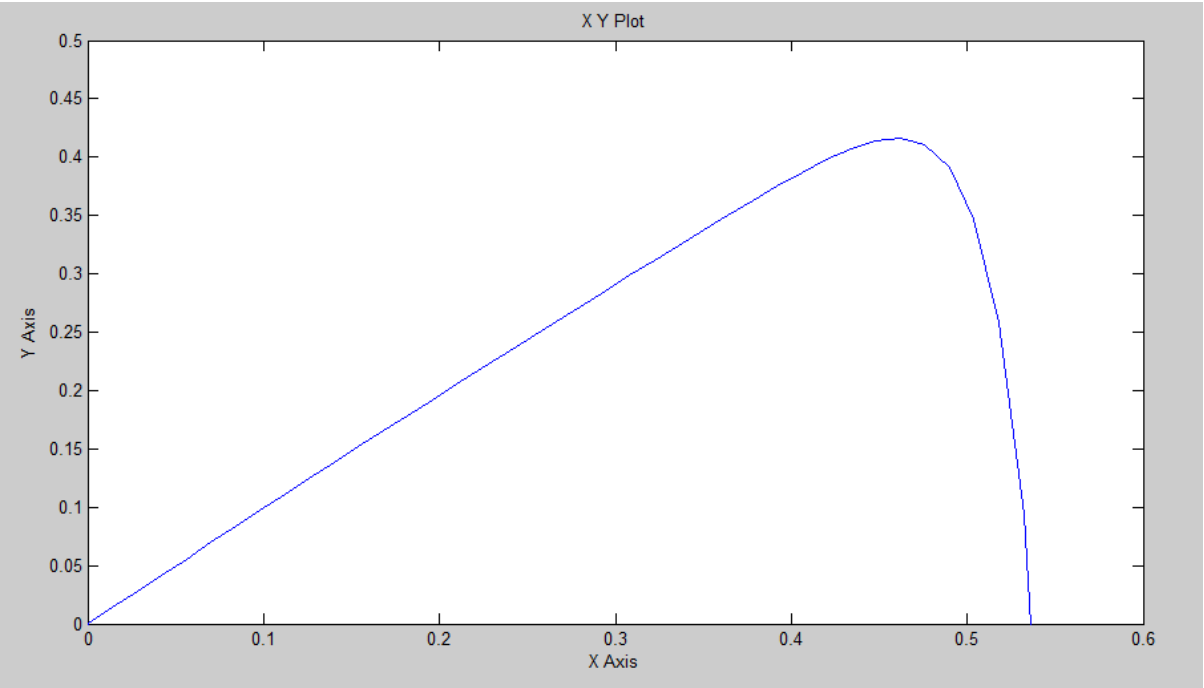

Fig 2.2.2: PV Power- Voltage Curve for solar cell

2.3 Control Strategies

The operation power control unit between the source of power generation and the grid depends upon the characteristics of the power generation source. The power

control unit can be either a single stage or multi-stage converter. The single stage converters have inherent advantage of higher efficiency, high reliability and compactness.

2.3.1 Fundamentals of power feed through GTI

The main specification of the grid-connected solar micro inverter is that current must be drawn from the PV panel and delivered to the utility grid at unity power factor. Consider a grid-connected micro inverter with following properties:

- V_{AC} is the fundamental component of the inverter output
- V_L is the voltage drop across the link inductor (EMI inductor)
- V_{grid} is the utility grid voltage waveform

Assuming that the losses are negligible, it can be observed that

$$\boldsymbol{V_p = V_{grid} + V_L}$$

Where all variables are vectors in the form of $v = V * eJ*\varphi$. Based on this, V_p is then calculated, as shown in Equation 1.

EQUATION 1:

$$\boldsymbol{Vp = Vg + j\omega LI}$$

To achieve the unity Power Factor condition, the current waveform must be in phase from the utility voltage waveform. Figure 7 shows how this waveform appears in vector form.

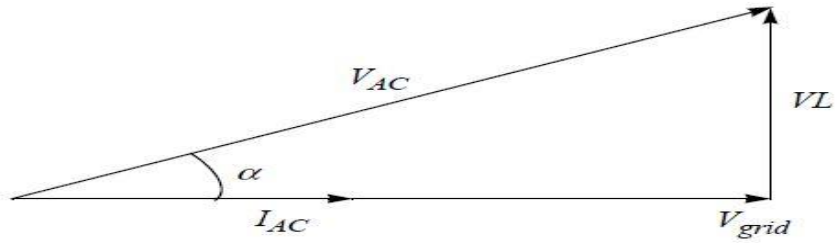

FIG 2.3.1.1: Vector Waveform

The key to controlling this operation is the inverter voltage variable, Vp. From Equation 2, I can be expressed, as shown in Equation 1.

Hence, the magnitude and direction of current flow (and therefore power flow), can be controlled by the phase shift δ and the magnitude of the inverter output voltage waveform.

2.3.2 SPWM Control

We know that in SPWM control mode

$$\mathbf{mV_{dc}=\sqrt{2}\,Vp_1}$$

Where

m: modulation Index

Vdc: DC voltage

Vp1: Fundamental RMS voltage

As power is fed at UPF, we can write that

$$\mathbf{Vp_1 \cos\delta = Vg \quad and \quad Vp_1 \sin\delta = IX}$$

$$\Rightarrow \boldsymbol{m = \frac{\sqrt{2}\,Vg}{Vdc\cos\delta}}$$

Also ,

$$\mathbf{P_{pv} = P_g = V_{dc}I_{dc} = V_gI_g}$$

Where

V_g and I_g are RMS value of grid voltage and current.

$$\mathbf{I_g=\frac{Vp\sin\delta}{X}}$$

On solving above equations, we find that

$$\boldsymbol{m = \frac{\sqrt{2Vg^2 + (\frac{PX}{Vg})^2}}{Vdc}}$$

Thus, by fixing Vdc, X and P we can calculate the modulation Index. Also, X is fixed by design constraints; P and Vdc are fixed by the characteristics of solar panel through MPPT as mentioned above.

2.3.3 Hysteresis Current Control method

In Hysteresis Current Control method,

$$V_p(inst.)= (S_1-S_2)V_{dc}$$

It automatically adjusts the δ value, so as to make the output current waveform follow the required waveform which in our case is grid voltage. Only condition required is that

$$V_{dc} > V_{p1}$$

Also,

$$Vp_1 \sin \delta = IX$$

$$Vp_1 \cos \delta = Vg$$

$$\Rightarrow V_{p1} = \sqrt{(X)^2 + Vg^2} \text{ and } \tan \delta = \frac{IX}{Vg}$$

Clearly, for a fixed X and V_g, **δ** and $\mathbf{V}_{p1}$ increase with current. As discussed above, we will be following two different control strategies. Relevant mathematical analysis has been done above. For power feeding through GTI, following constraints need to be followed

- ⇨ **THD_v < 5%**
- ⇨ **UPF i.e.** current and voltage waveforms should follow each other
- ⇨ **Proper voltage Islanding facilities** which means that in Non GTI mode, there should be no current injection by the inverter.
- ⇨ **Proper freewheeling path for opposite polarity current**

2.4 General Purpose Computations, constraints and constants:

- X = 0.1 Henry
- δ (del)= 10 deg
- For 256 samples per cycle, 10 deg=256*10/360=8(approx.)=$(00001000)_2$
- 200< V_g<250
- $V_{min}<V_{dc}<V_{max}$ where limits are designed by the design constraints of PV cell.
- M_a (modulation index) should be less than 0.85 because best harmonic performance is provided in this range only.

- Thus for V_{min}, a modulation index of 0.9 must be able to produce 250 V rms.
- Selection between HCC and SPWM can be made with the help of a switch (s_c) where

  S_c=1 means SPWM

  0 means HCC

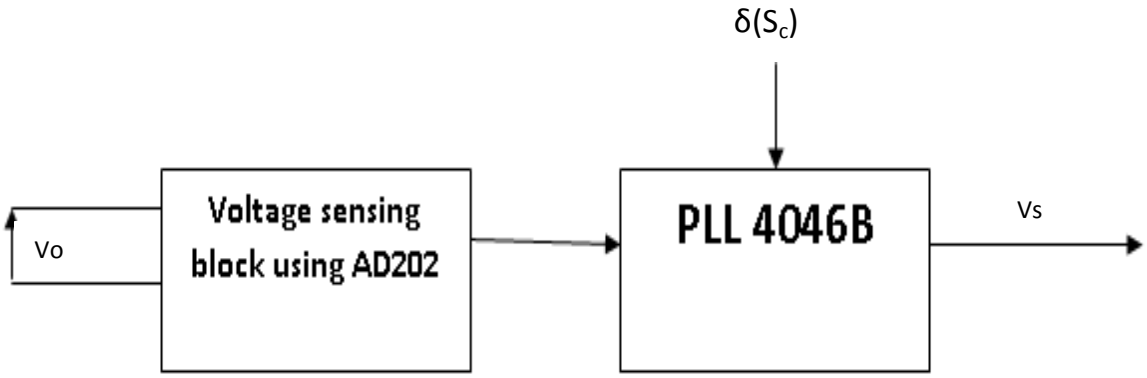

Fig 2.4.1: Generation of unity sine template of required phase delay angle (δ)

Voltage sensing block senses the output voltage using AD202 and output from this block is fed to PLL unit which contains a VCO (Voltage controlled oscillator), A UVEPROM of 256 bytes, A DAC and frequency measurement unit which works on zero crossing detection principle and determines the frequency and phase (Zero angle instant)of input signal which is outputted to VCO which generates a sampling wave of frequency given by (f_o*256) in our case. At every clock pulse of VCO, Address of address bar is incremented by 1 and thus ROM outputs the next value to data bus. Data bus is connected to a DAC0809 which converts the available digital value to an analog signal and thus we obtain a unity sine template.

Now for δ=0, Initial address is 00000000_2

For δ=10deg, Initial address is 00001000_2

Also we require zero delay in case of HCC and a delay of 10deg in SPWM technique. Thus we can connect A3 of address line to S_c which will automatically give required phase shift to sine template.

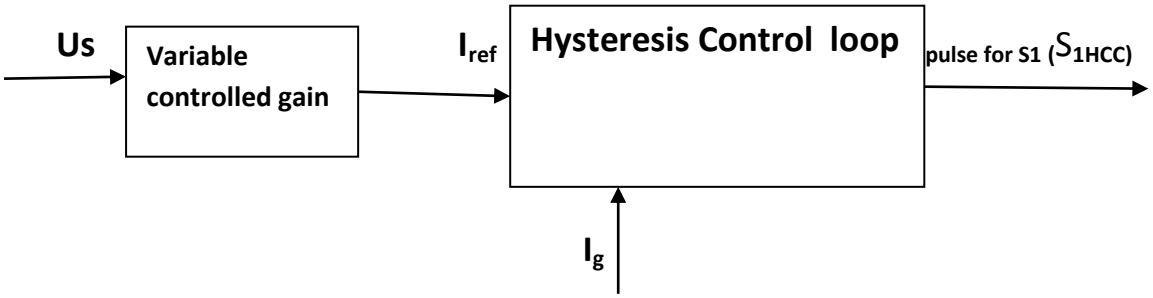

Fig 2.4.2: HCC control Strategy

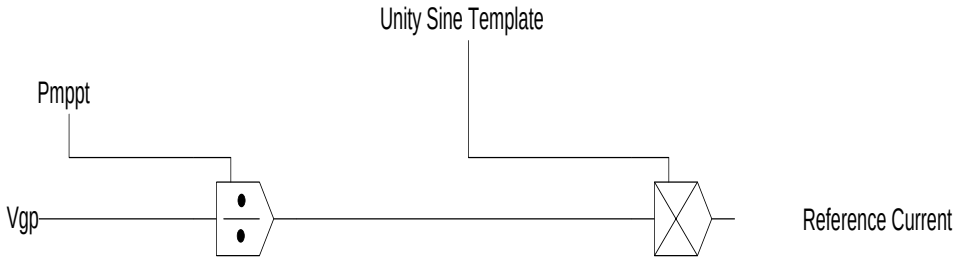

Fig 2.4.3: Generation of reference current for HCC strategy

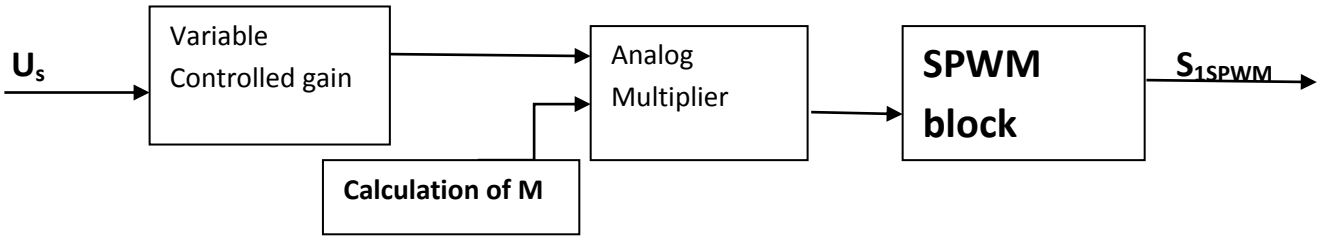

Fig 2.4.4: SPWM control Strategy

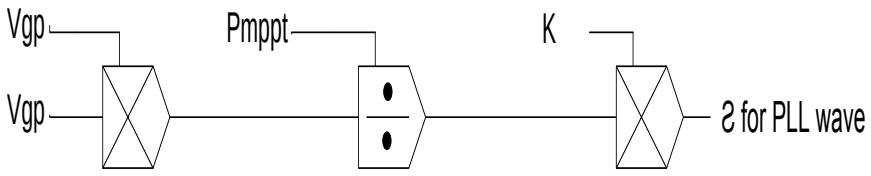

Fig 2.4.5: Calculation of delta for PLL unity sine wave

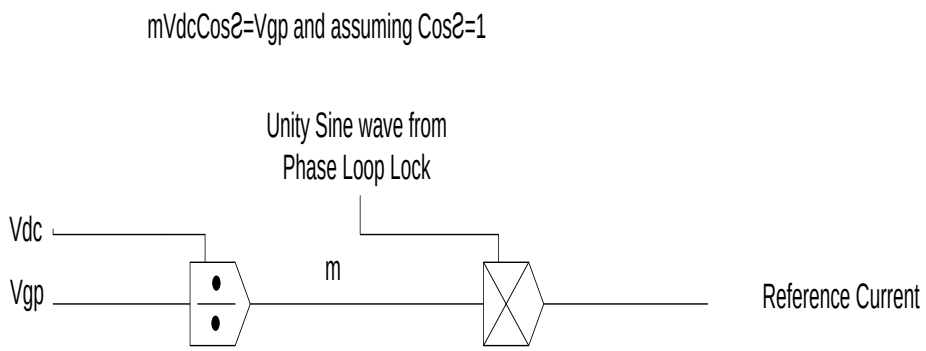

Fig 2.4.6: Generation of reference signal for SPWM strategy

Pulse for S1 can be generated using any of the above techniques. In unipolar switching mode, S1 and S4 have same pulses while S2 and S3 have same pulses. The complete block diagram has been discussed in background section of the report. We also provide a dead band between the switching instants of two devices of same leg. Thus using one pulse we can generate pulse for all the devices. Further, selection between both the strategies can be made using switch S_c.

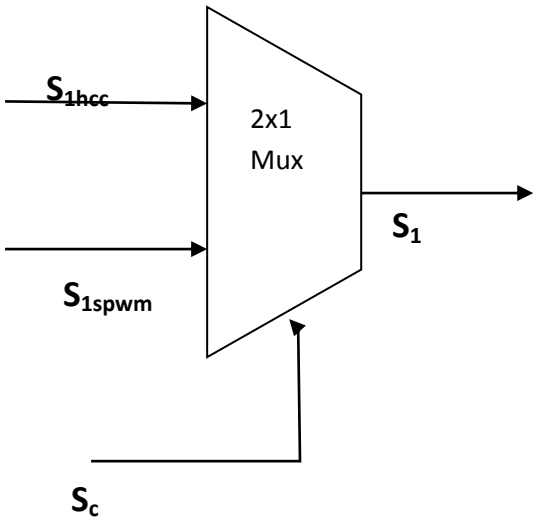

Fig 2.4.7: Selection between two strategies

2.5 Power Circuit

As discussed in background, the power circuit used will be a simple H-bridge with an extra freewheeling circuit connected in parallel to the grid to allow the flow of opposite polarity current. Fig.12 below shows the modified power circuit using H-bridge and freewheeling circuit to avoid the power being fed back to solar panel. Fig 2.5.1 below shows the freewheeling circuit and the control circuit for the same.

2.6 SPWM Topology simulation

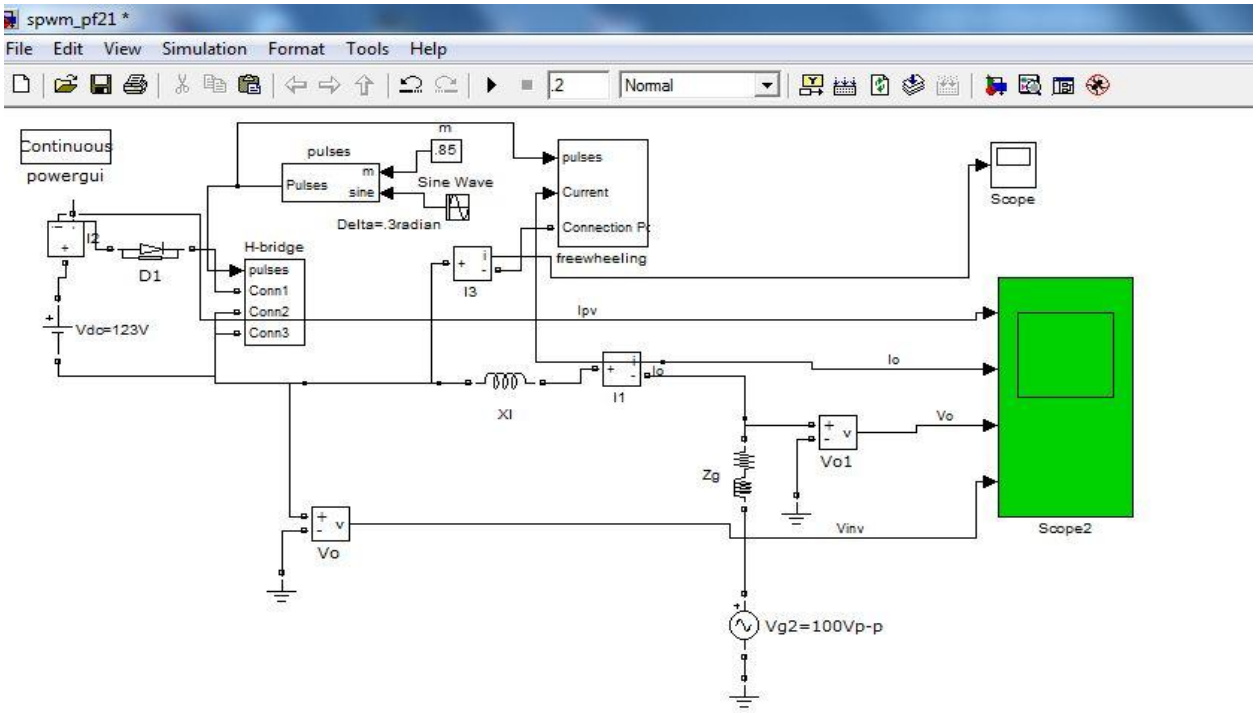

Fig 2.6.1: Power circuit of modified topology of GTI

In above figure, diode D1 blocks the negative current going to the source while freewheeling block allows the flow of negative currents during this time. As clear in figure 2.5.1, MOSFET 1 is switched ON when devices 2 and 3 of H-bridge are conducting. Hence switching ON MOSFET 1 will allow the actual positive polarity currents to flow while other leg is switched ON when devices 1 and 4 are conducting, thus providing the actual negative polarity currents a path to flow as diode has blocked their path.

Simulation results of SPWM strategy has been shown in figures below where in we can clearly see that Inverter is able to feed the power at UPF. This fact is proved by in phase current and voltage.

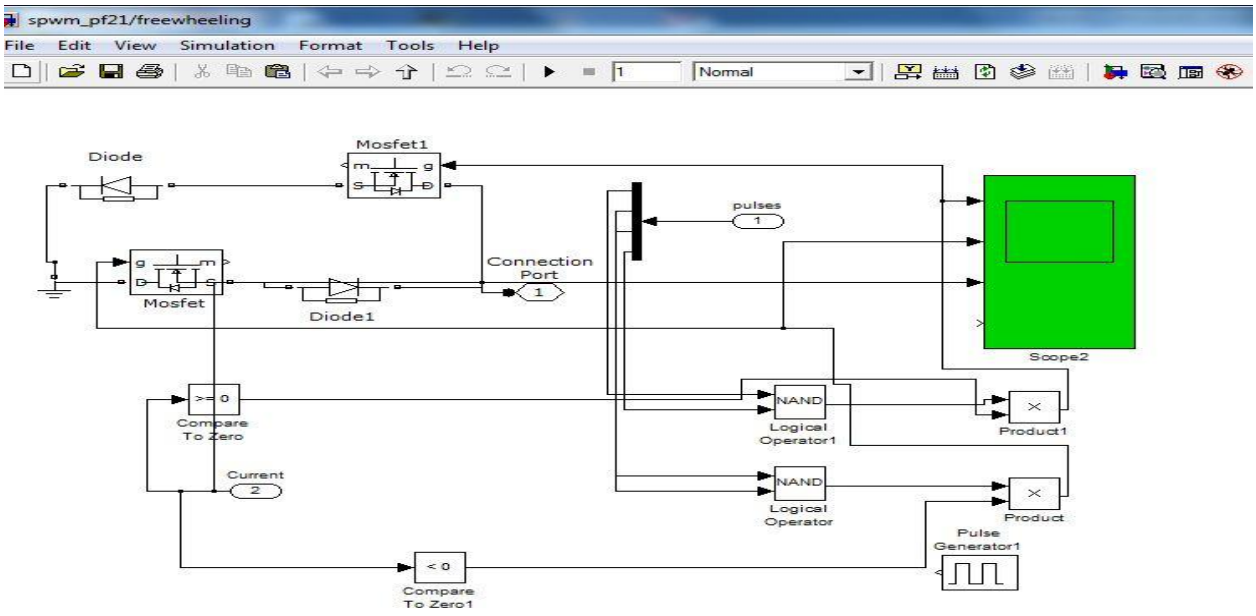

Fig 2.6.2: Freewheeling block for the power circuit

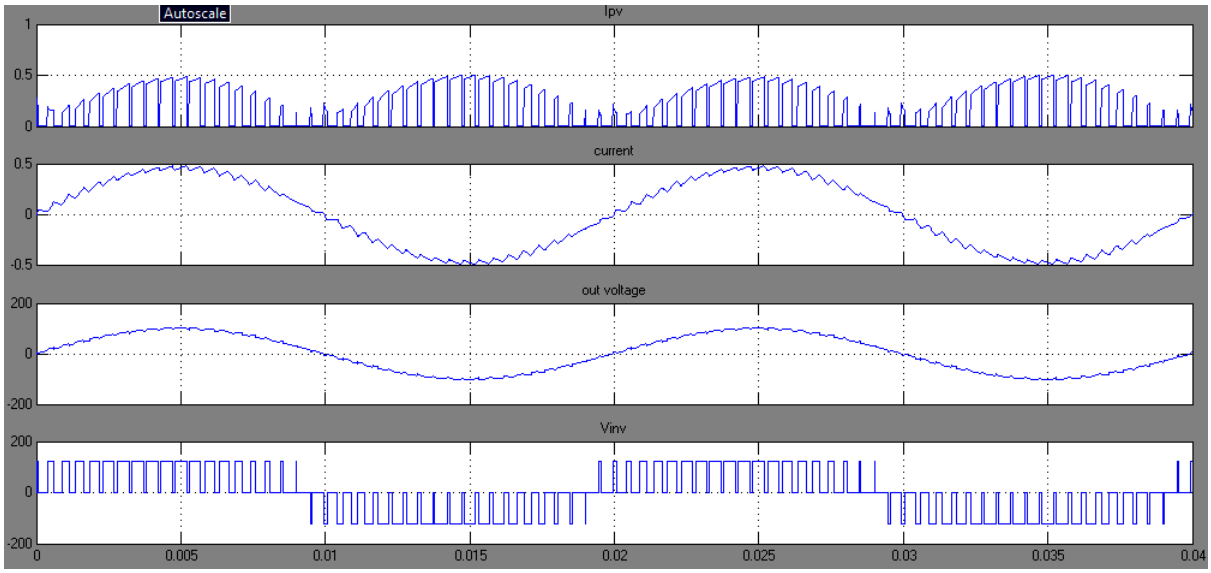

Fig 2.6.3: SPWM topology simulation results(20 kHz switching frequency)

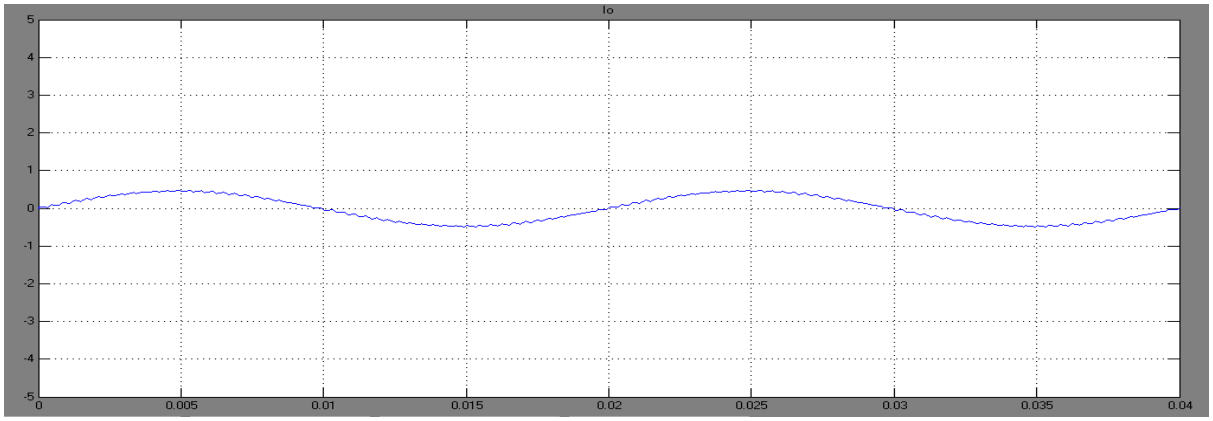

Fig 2.6.4: SPWM topology-Grid Current (20 kHz switching frequency)

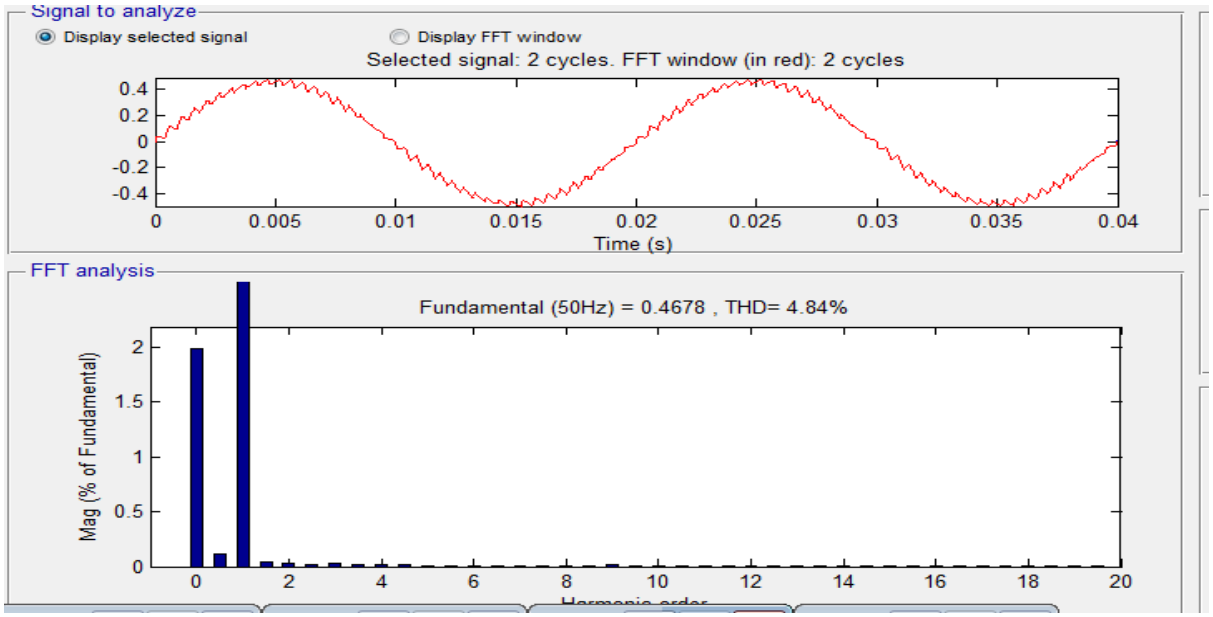

Fig 2.6.5: SPWM topology-Grid Current Harmonics (20 kHz switching frequency)

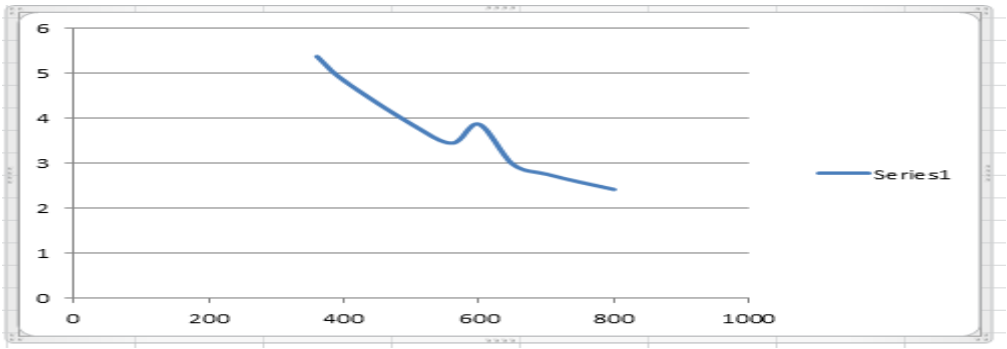

Fig 2.6.6: THD vs mf

2.7 HCC Simulation

Power feed using Current Controlled Voltage Source Inverter:

The inverter current using a hysteresis controller is made to follow the reference current which is 180 out of phase with the grid voltage so that the power is being fed back to the grid at unity power factor. The dc side current thus has a strong second harmonic component which is to be filtered out for implementing MPPT algorithm for feeding power from a solar cell.

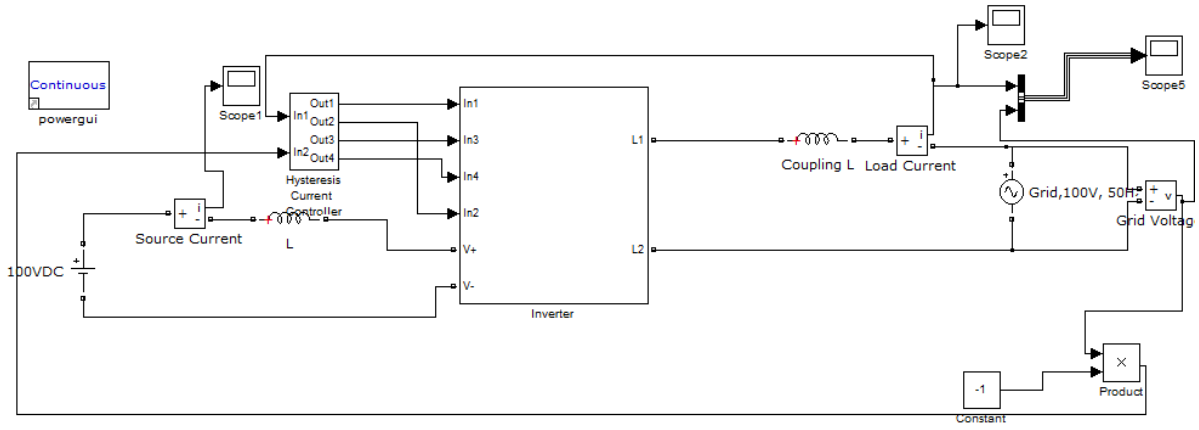

Fig 2.7.1: MATLAB Model for HCC topology

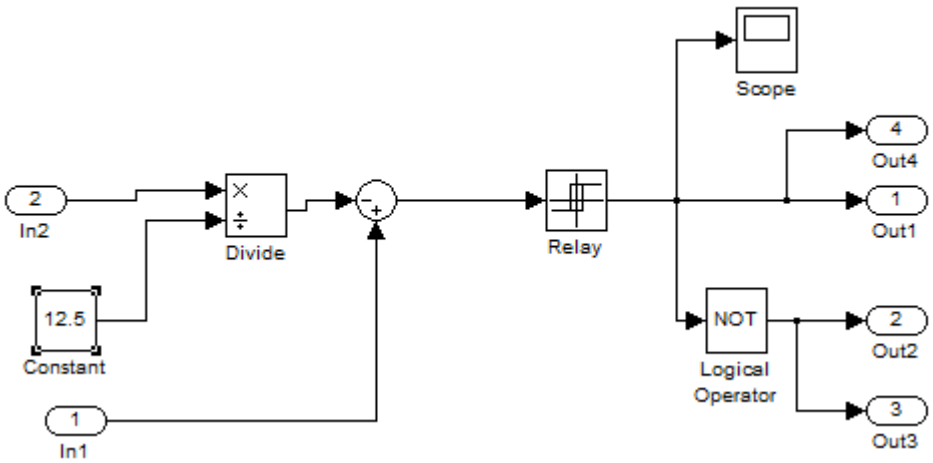

Fig 2.7.2: Hysteresis Current Controller Control strategy

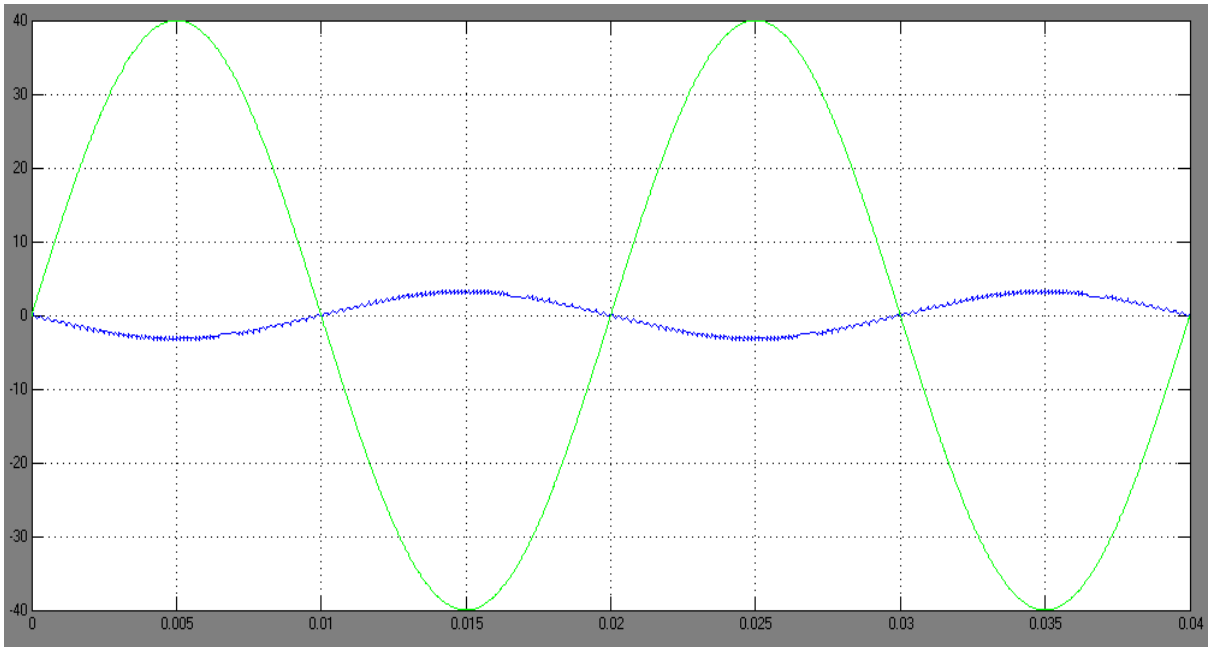

Fig 2.7.3: Grid Voltage and grid current in HCC Simulation

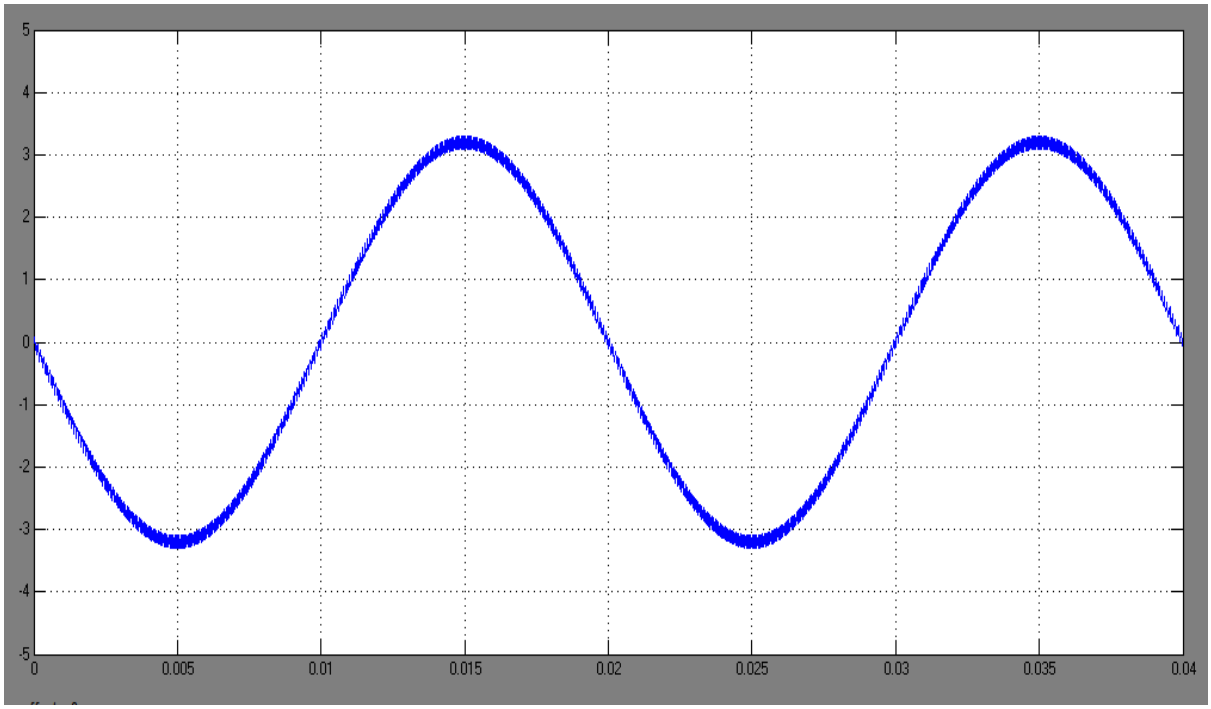

Fig 2.7.4: Grid Current (amplified) in HCC Simulation

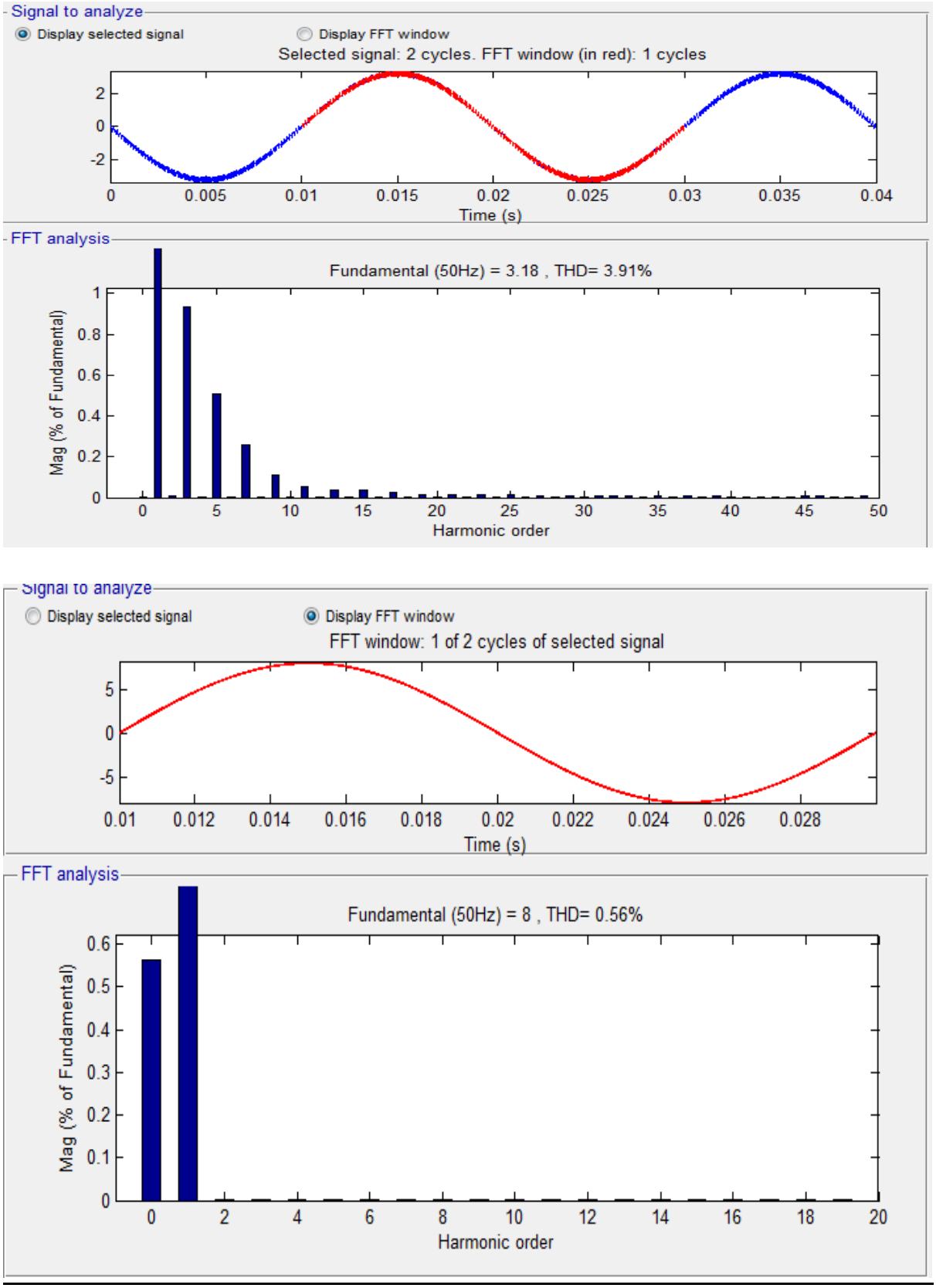

Fig 2.7.5: THD variation (grid current) in HCC Simulation

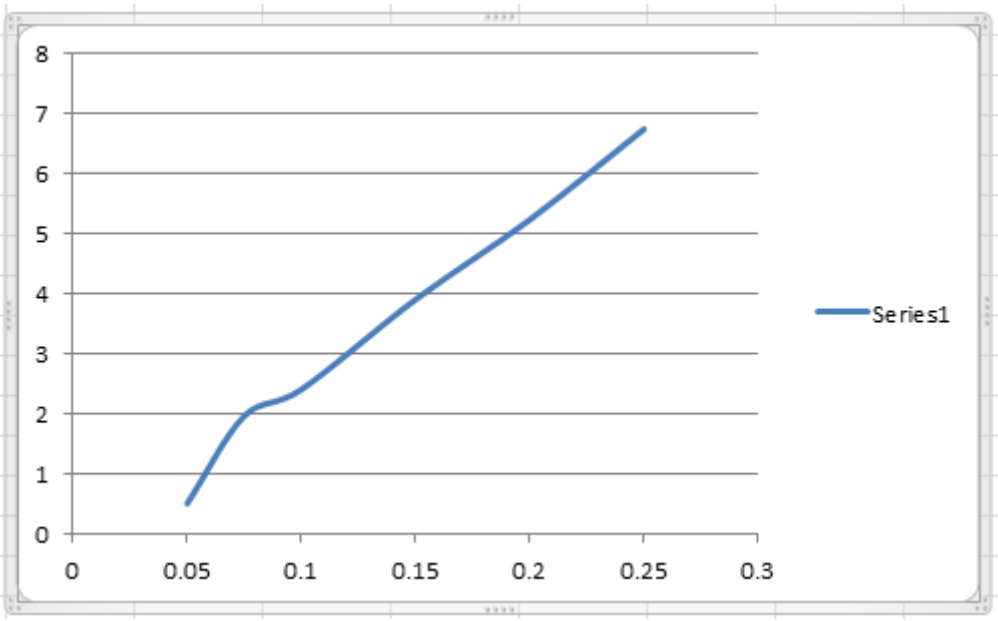

Fig 2.7.6: Grid Current THD with Hysteresis band variation

2.8 Discussions and Comments on simulation results:

- For both SPWM and HCC the power is being fed to the grid at unity power factor and thus the grid current is 180 degrees out of phase with grid voltage.
- For carrier wave frequency greater than 20 kHz the Total Harmonic Distortion in the grid current is less than 5% in accordance with IEEE-519 standard.
- For the THD of the grid current to be less than 5% in HCC strategy the hysteresis band should be of width less than 0.5
- The THD of the grid current decreases with the increase in carrier wave frequency because the devices being considered are ideal devices.
- The THD of the grid current increases with the increase in the hysteresis band as should be expected.

Chapter 3

Hardware Implementation of Single Phase Inverter

3.1 Power Circuit

Power circuit was fabricated using MOSFETs (IRF460) as basic switching devices. As discussed in previous chapters, standard H-bridge has been used. MOSFETs have been fitted on a module which receives the TTL gate pulses from pulse generator circuit and various components as discussed below performs the task of protection and isolation of devices.

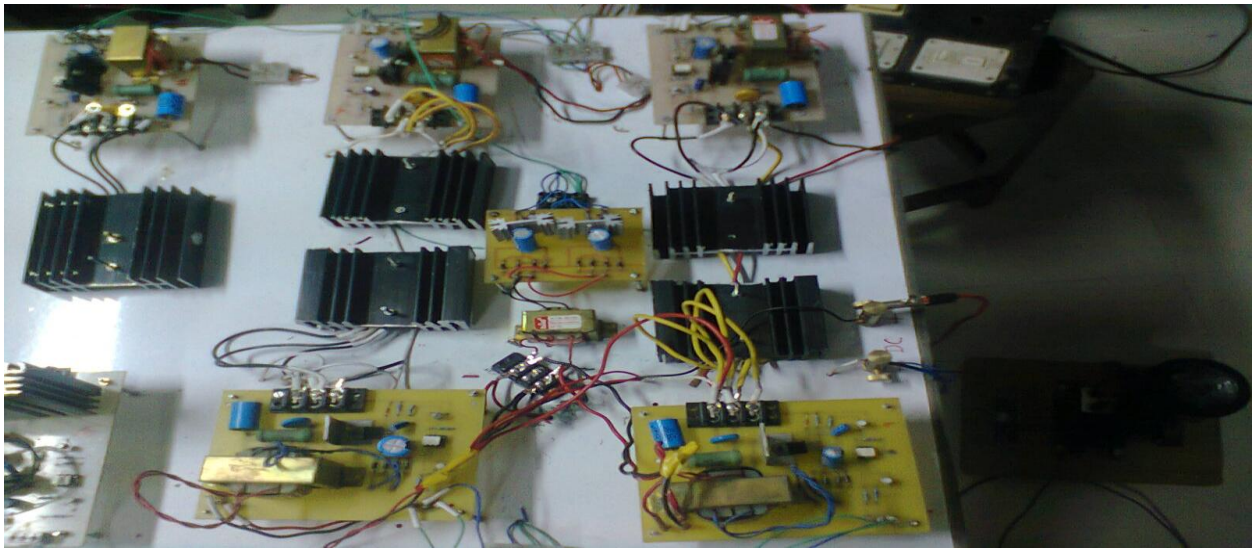

Fig 3.1.1: Voltage source inverter circuit with snubber circuit and freewheeling path

3.1.1 **Snubber Circuit:**

It protects semiconductor devices by:

- Limiting device voltages during turn-off transients
- Limiting device currents during turn-on transients
- Limiting rate of rise of currents through semiconductor device at device turn-on

- Limiting rate of rise of voltages through semiconductor device at device turn-off

- Shaping the switching trajectory of the device as it turns on/off

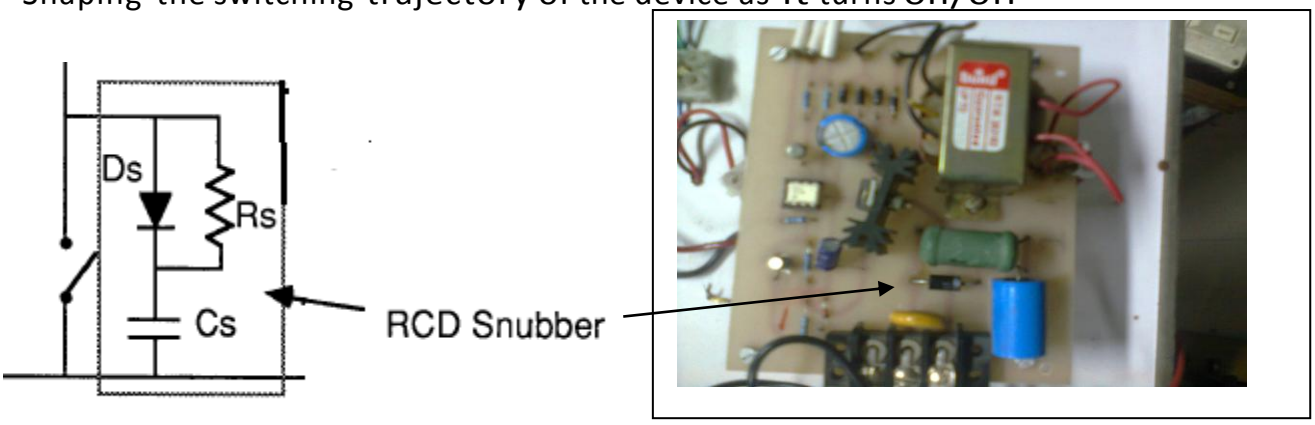

Fig 3.1.1.1: Snubber Circuit Diagram schematics and actual implementation

Values of capacitance to be used can be calculated as under

$Cs=I_{max} * T_{off(min)}/V_{in}= 27*168*10^{-9}/24=0.1\mu F$

3.1.2 **Pulse Amplification and Isolation Circuit**

Pulse amplification and isolation circuits first isolate the pulses coming from TTL sources from the power circuits and then pulses are amplified. Whole process of amplifying and isolation is carried out by **MCT2E** along with **npn** transistors and separate DC supply created using standard 12-0-12 transformer and voltage regulator-7812. Separate DC supply is must for each module as the pulses have to be given with respect to the source of each mosfet, hence we need separate ref. point for each pulse.

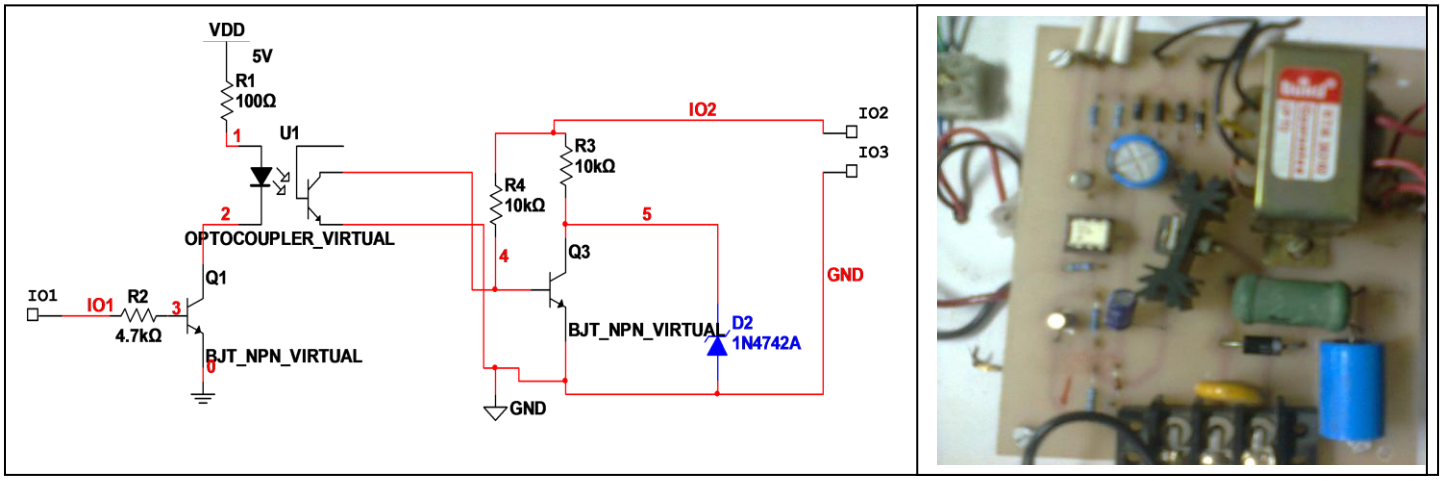

Fig 3.1.2.1: Pulse Amplification Circuit schematic and its actual implementation

3.2 Control Circuits

Control Circuit has been made up of different components fabricated as separate PCB's. Each PCB is a unique module in itself which performs a unique function. Various Components of control circuit have been discussed as under:

3.2.1 Voltage sensing circuit

Voltage sensing was performed using a standard AD-202 circuit as shown in figure below.AD-202 performs the task of isolation and stepping down of input signal. It was ensured that peak of voltage reaching the input terminals of AD202 is less than 5 volts.This was ensured by using a stepping down circuit using resistors.

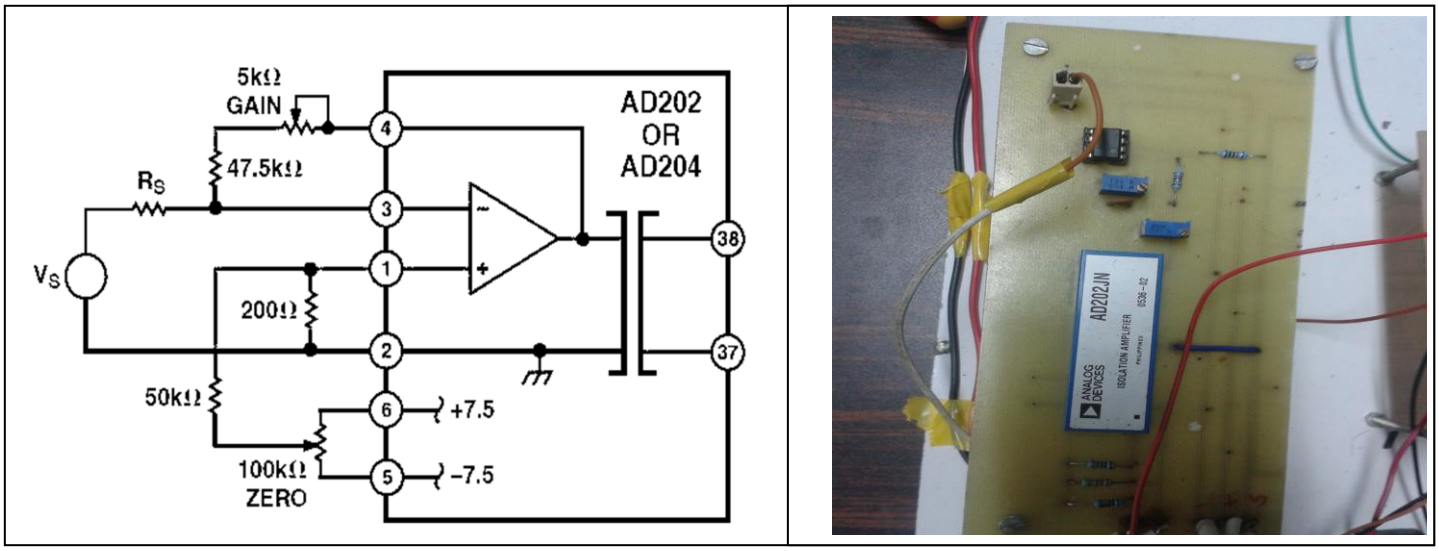

Fig. 3.2.1.1 : Volatge sensing circuit using AD202 schematic and actual implemenation

3.2.2 Voltage Phase and Frequency Locking Circuit

A PLL module was designed and fabricated on a single PCB .The module receives the output of voltage sensing block. This input is rectified by a diode circuit and LM339 circuit converts the rectified input signal into a square wave of same frequency and phase as of source signal. This is given as input to

CD4046BE which contains a voltage controlled oscillator and has a facility of either locking in phase to the input signal or in quadrature to input signal. Here in phase locking strategy was followed and a square wave of frequency;f=256*f_i is generated. This clock pulse is given to a 8-bit counter fabricated using two SN74LS93 IC's and output serves as address lines (A0-A7)to the 8KB UVEPROM(M27C64A).ROM contains look up table of sine wave. Other 5 addresses(A8-A12) are operated by addresses provided by MPPT module to provide the required phase lead in the ref. signal i.e. sine wave. Output of ROM drives the standard DAC0808 circuit to produce the required sine wave.

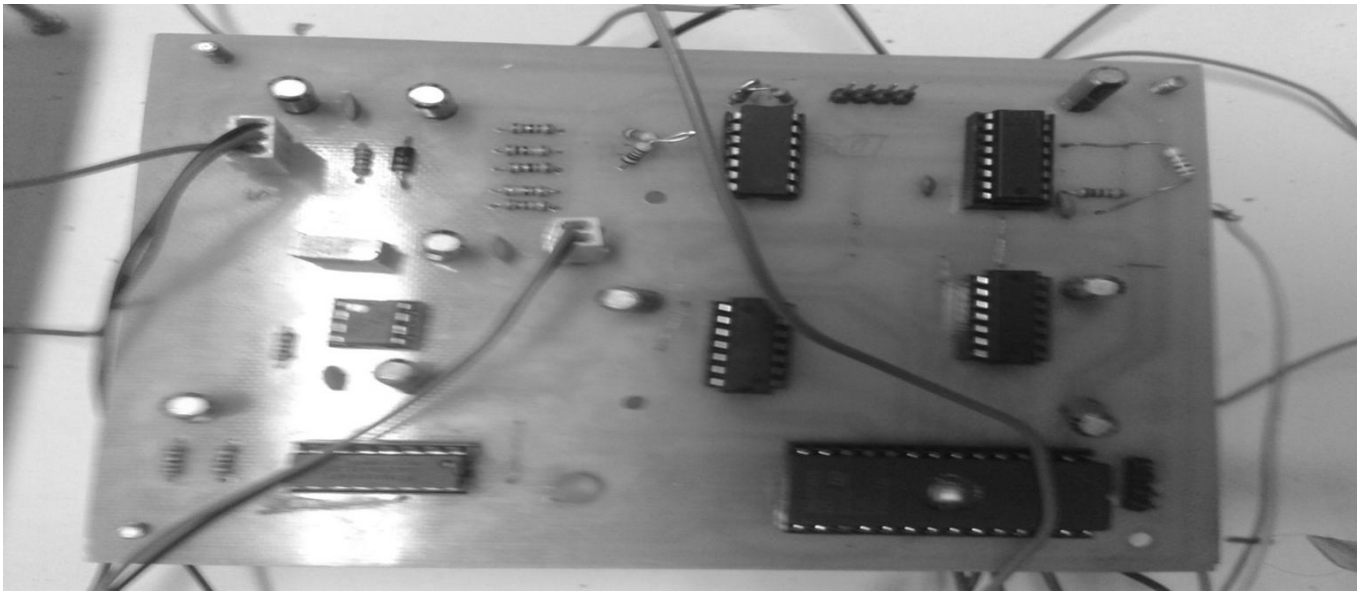

Fig 3.2.2.1 : PLL implementation

3.2.3 MPPT Module

MPPT module has been implemented using the standard dividing and multiplication circuits using AD633 as discussed in Appendix. It takes AD202 output , DC voltage and current as input and performs various operations as discussed in previous chapters. It calculates modulation index(m), δ(power angle) for SPWM strategy and grid current peak for HCC strategy which are then multiplied with the unity template of ref. sine wave with the help of AD633 only. "δ" is properly calibrated and given as input to ADC0809 which

generates four address for the UVEPROM in PLL module to obtain the desired phase lead.

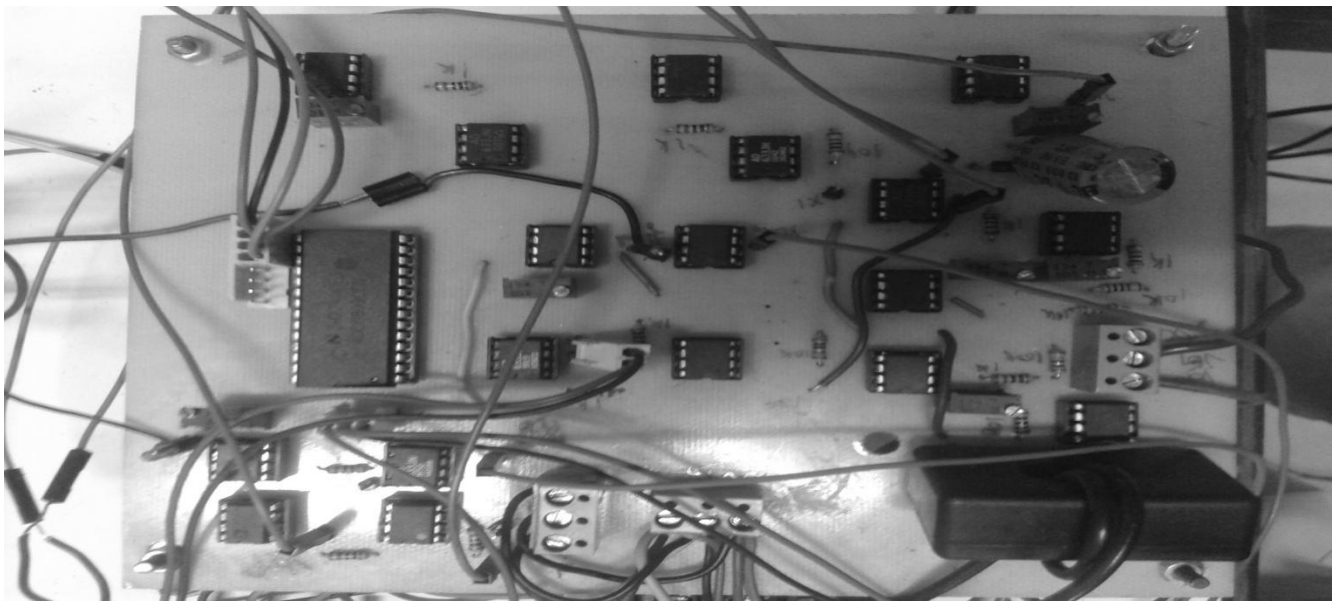

Fig.3.2.3.1: MPPT module implementation

3.2.4 SPWM Pulses Generation and deadband Module

This module has the function of generating uses following sub-modules:

- Triangular wave generation
- SPWM core circuit
- Deadband Circuit

3.2.4.1 Triangular Wave Generator

Since the required frequency has to be greater than 18Khz as per IEEE standards as mentioned in previous chapters, a minimum slew rate of 50V/us is required. Hence the op-amp used is a quad-opamp LF347n and a standard triangular wave generation circuit was followed to obtain a unity triangular wave of frequency 25 KHz.The circuit, schematic.and output has been shown in below figures.

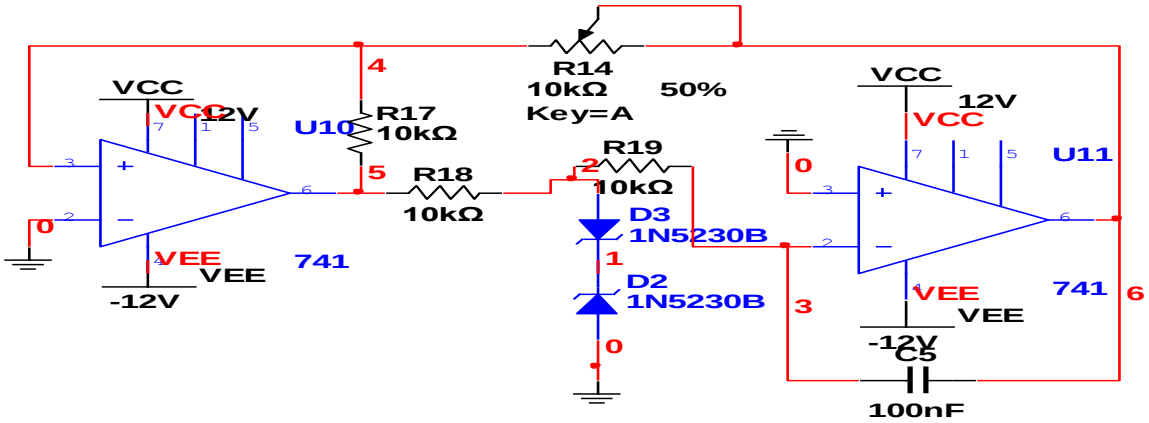

Fig.3.2.4.1.1: Triangular wave generation schematic

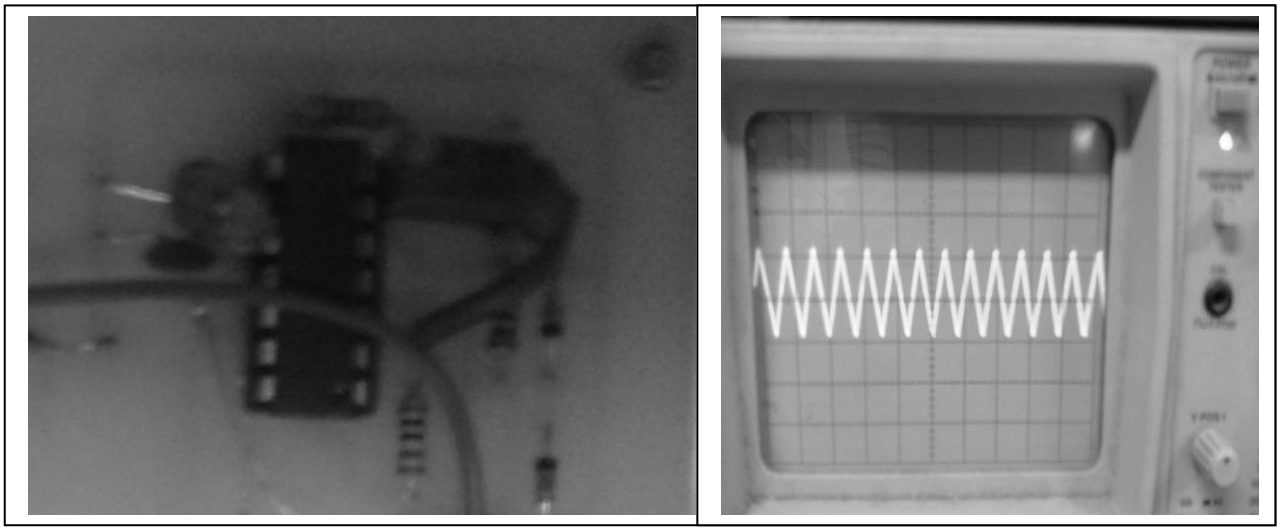

Fig.3.2.4.1.2: Triangular wave generation implementation and output wave

Peak to peak voltage output=(2*R14/R17)*Vsat

Frequency=R17/(R14*4*(R18+R19)*C5)

3.2.4.2 SPWM Core

It compares the ref. and carrier signal to produce a CMOS logic output as per the switching strategy (unipolar or bipolar) as discussed in previous chapters. CMOS logics were converted to TTL logics using LM339.

3.2.4.3 Deadband Circuit

Deadband circuit was fabricated as discussed in previous chapters using 7404 and 7408. It takes as input the output of HCC and SPWM pulse selection switch and produces four pulses for the devices.

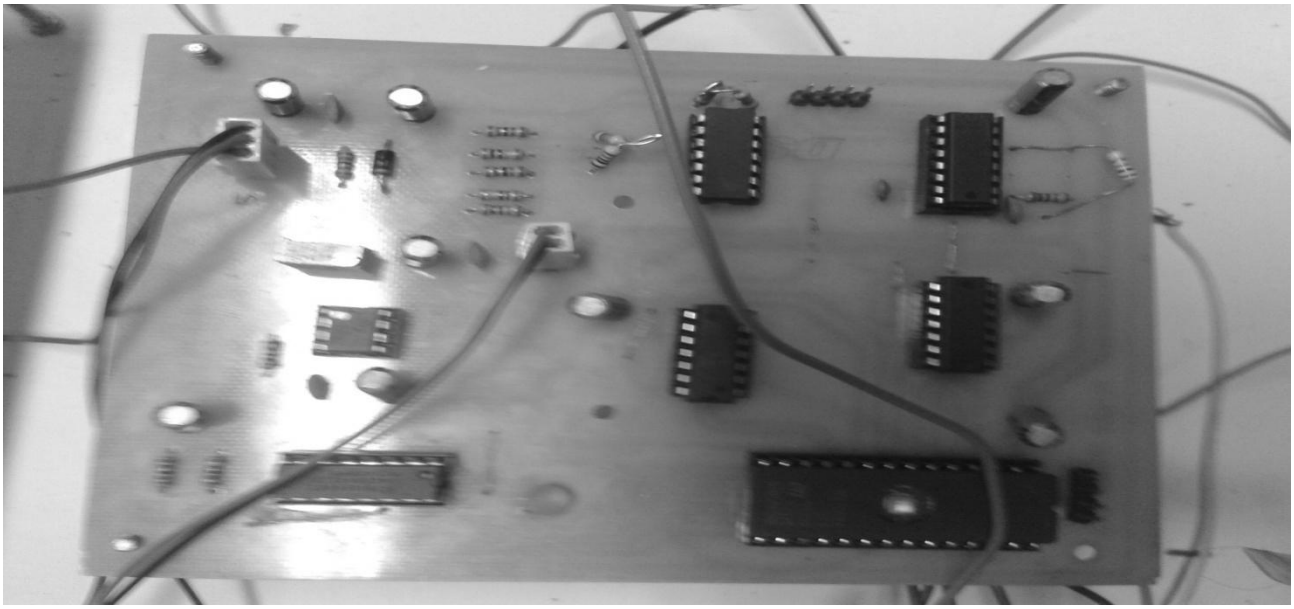

Fig 3.2.4.3.1: Deadband and SPWM core implementation

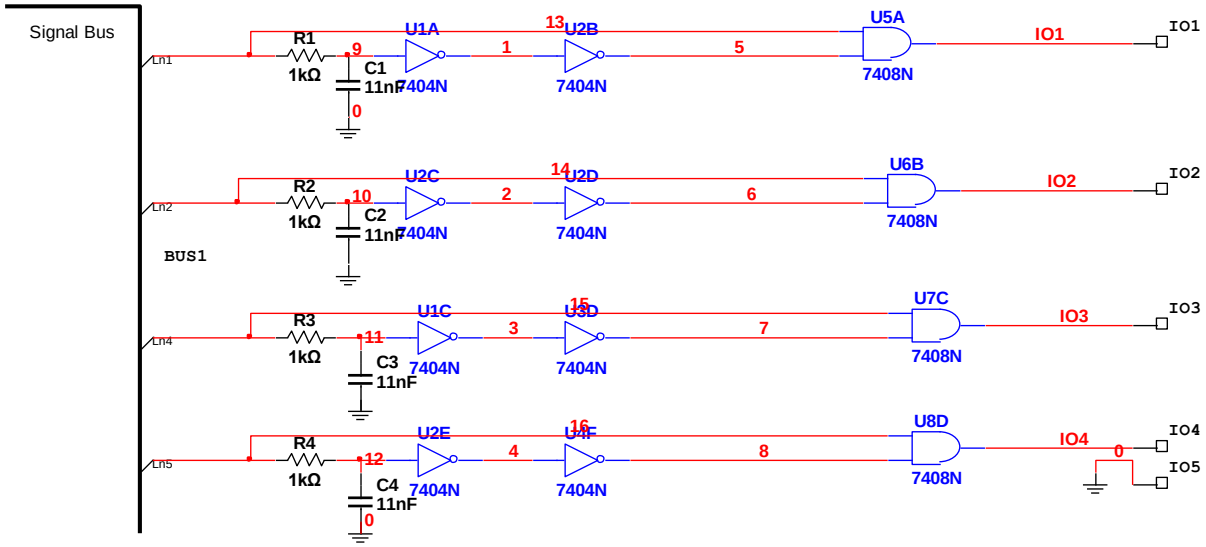

Fig 3.2.4.3.2: Deadband schematic

3.2.5 HCC Control Module

Hysteresis current control module produces the gate pulses by comparing the load current with the reference current. As IEEE standard requires pf to be unity, voltage output of PLL with zero lead multiplied with peak grid current is used as ref. current. It primarily consists of following:

3.2.5.1 Current Sensing Circuit

Current sensing circuit is fabricated using HALL Effect sensor and buffer.

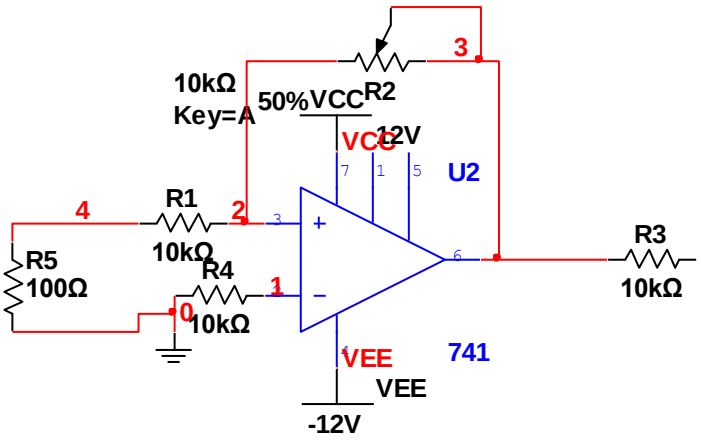

fig. 3.2.5.1 : current sensing circuit schematic

3.2.5.2 HCC Core Block

HCC core block was fabricated using opamp-741 and LM339.

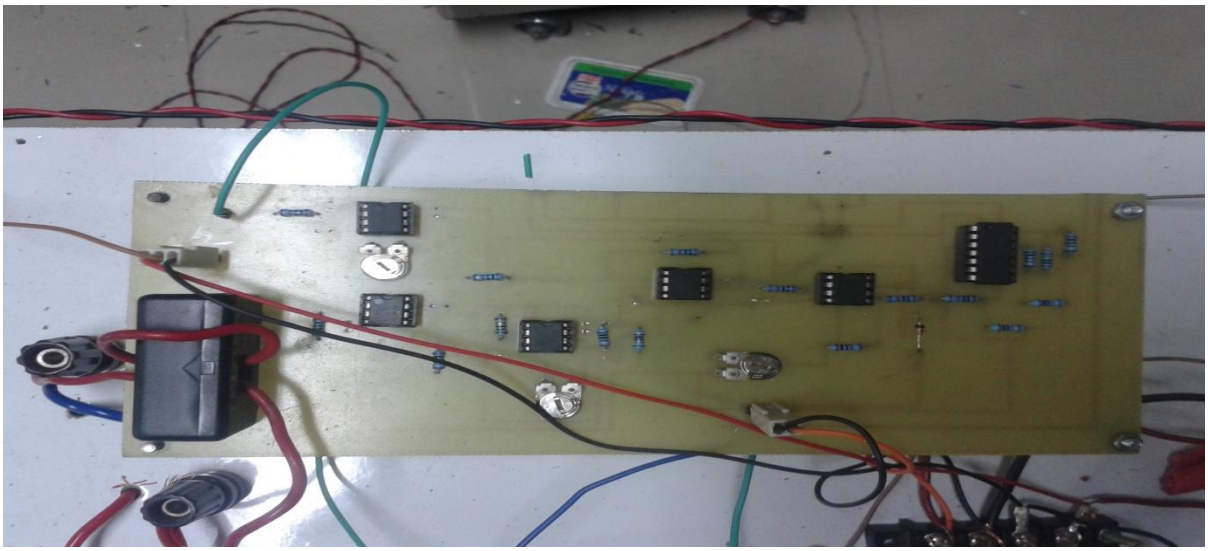

Fig 3.2.5.2 : HCC and Current sensing circuit implementation

3.3 Power Supplies

Here is the standard dual power supply using the Positive and Negative Voltage regulator ICs. It can give +12 volt and – 12 volt DC with a common ground. This power supply is ideal to power amplifier circuits that require well regulated dual power supply. It can give 1 ampere current to the circuit. 14-0-14 volt 1 Ampere step down transformer is used to drop 230 volt AC to 14 volt DC which is then rectified using the standard full wave bridge rectifier comprising D1 through D4.Smoothing capacitors C1 and C2 remove the ripples from low volt AC. Two regulator ICs are used

to generate + 12 volt and – 12 volt DC. IC1 is 7812 positive regulator giving +12 volt regulated output.IC2 is 7912 negative regulator and its pins are slightly different from 7812. See the connection in the diagram. Regulated outputs from the regulator ICs are available from pin 3 which can be used to power the circuit. Capacitors (C3 and C4) act as noise filters to give clean DC.

7805 is a 5V fixed three terminal positive voltage regulator IC. The IC has features such as safe operating area protection, thermal shut down, internal current limiting which makes the IC very rugged. Output currents up to 1A can be drawn from the IC provided that there is a proper heat sink. A 9V transformer steps down the main voltage, 1A bridge rectifies it and capacitor C1 filters it and 7805 regulates it to produce a steady 5Volt DC. The circuit schematic is given below.

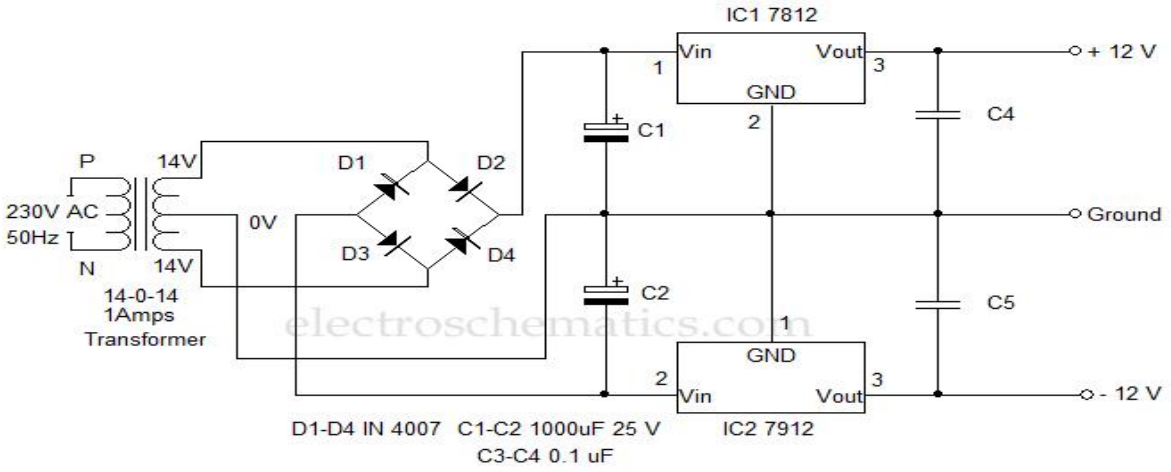

Fig 3.3.1: ±12 Supply Circuit schematic [8]

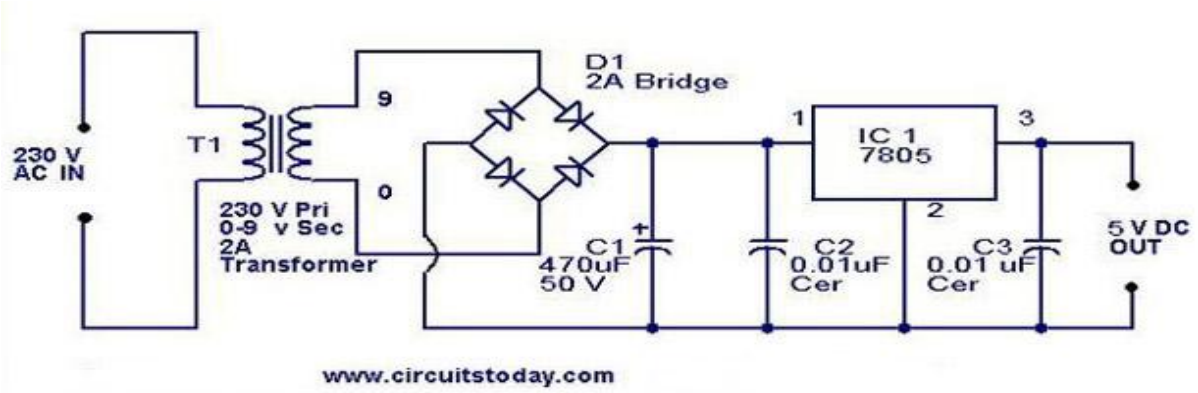

Fig 3.3.2: +5 Volt Supply schematic

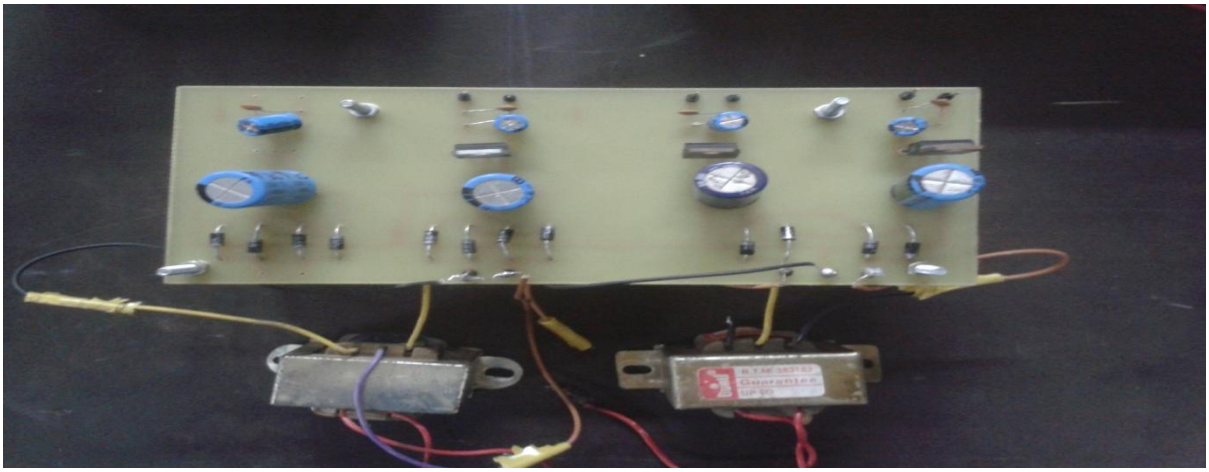

Fig 3.3.3: Power Supply implementation

3.4 Coupling Inductors

For implementation of HCC strategy, coupling inductor is required on both AC and DC side so as to control the sharp variation in current and limit the switching frequency. Two machine model used for power feed also requires a coupling inductor between DC and AC sided. Value of inductor is fixed on the basis of maximum power that is supposed to be fed through the strategy.

CHAPTER 4

EXPERIMENTAL SETUP AND RESULTS

Whole project was setup as per the strategies discussed in previous chapters. A connection diagram of overall project has been shown as under.

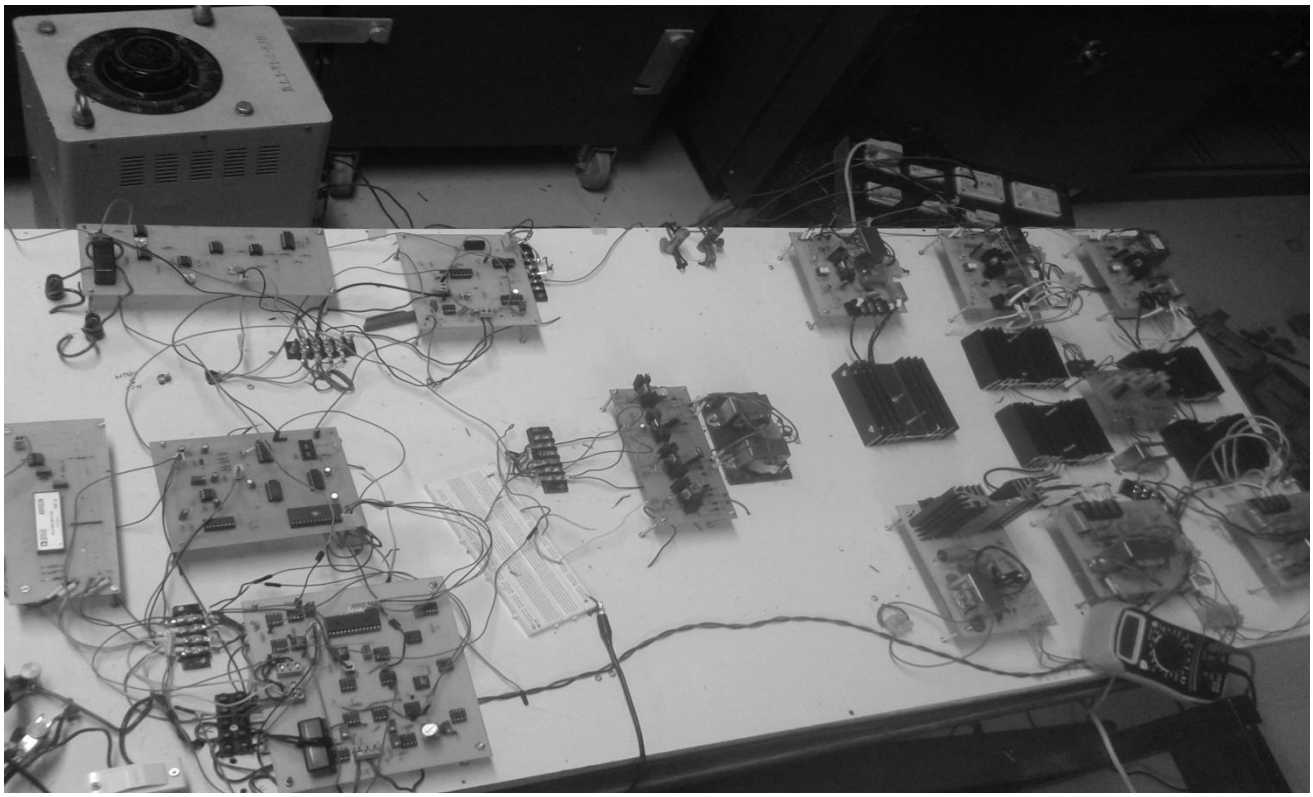

Fig. 4.1: Full experimental setup for grid tied inverter

4.1 Voltage sensing module

Voltage sensing module was directly supplied with 230V RMS AC supply and following waveform was obtained as output which was then used as input signal to MPPT module and PLL module.

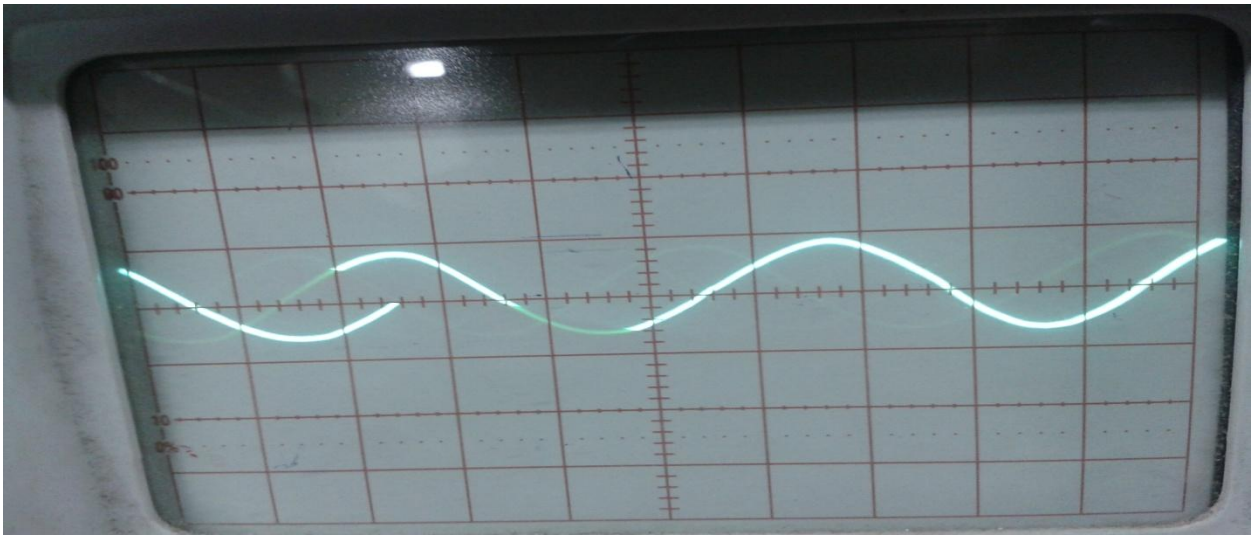

Fig. 4.1.1 : Voltage sensing module output

4.2 Phase Locked Loop and MPPT module Setup

Phase locked loop was provided with the output of voltage sensing module and following signals were obtained at different terminals.

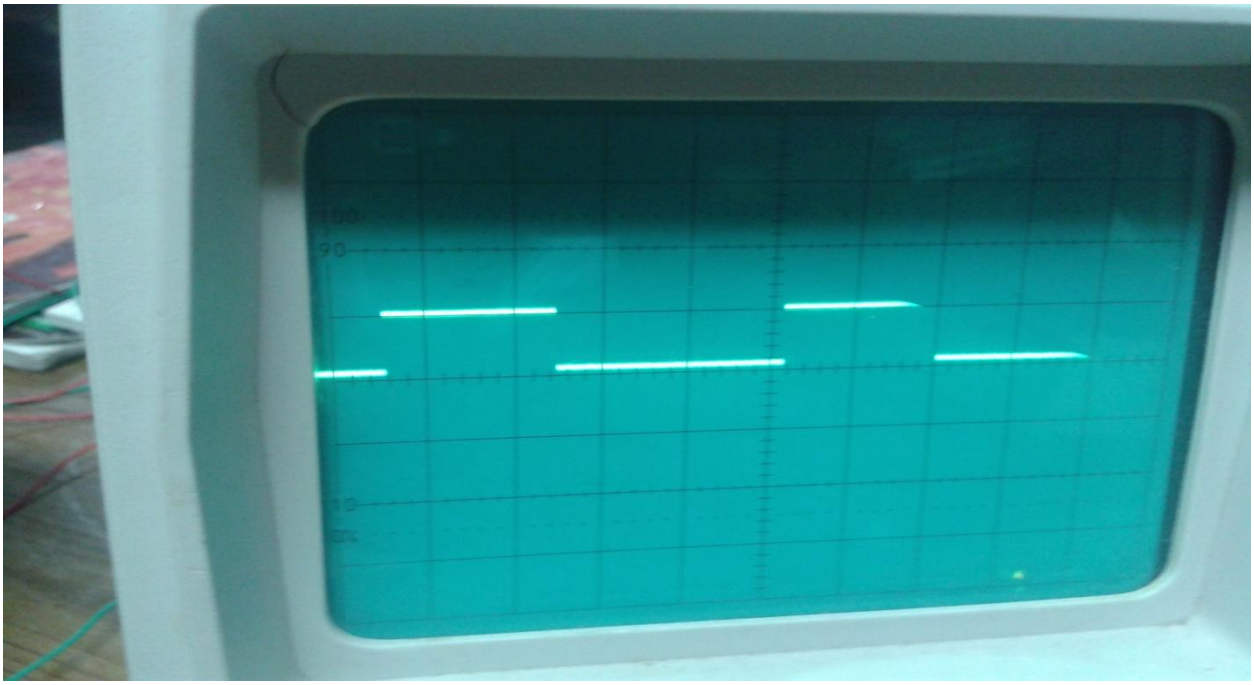

Fig. 4.2.1: Locking signal input to 4046

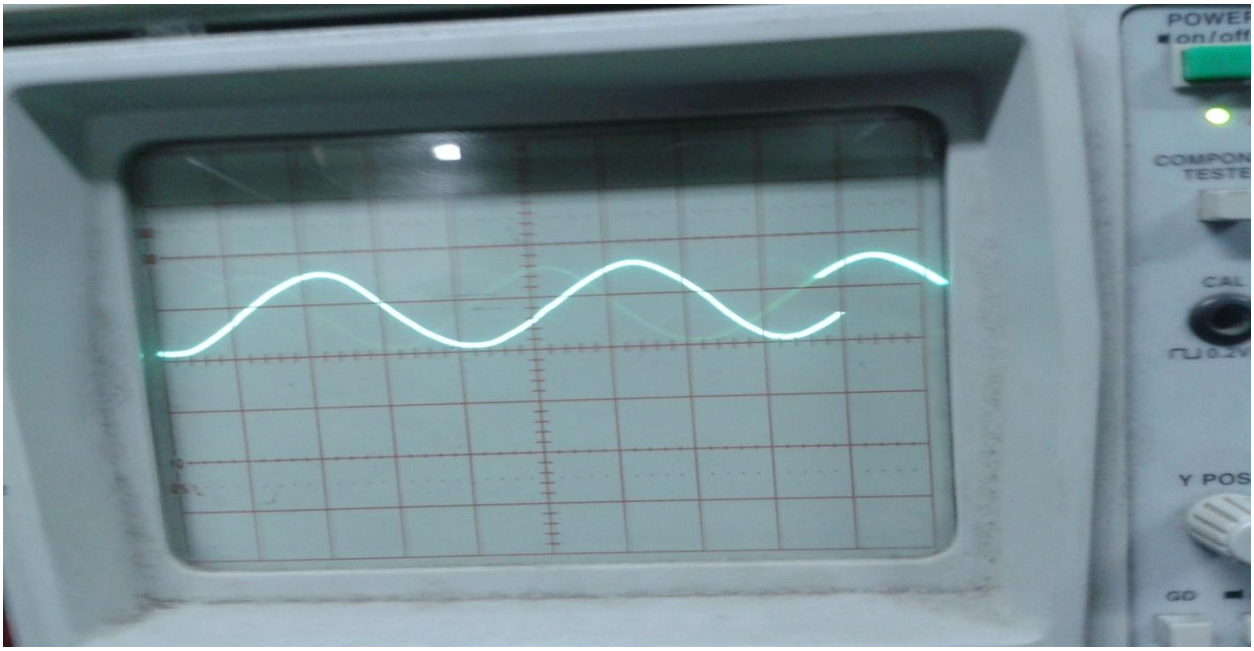

Fig. 4.2.2 : DAC0808 output without offset removal

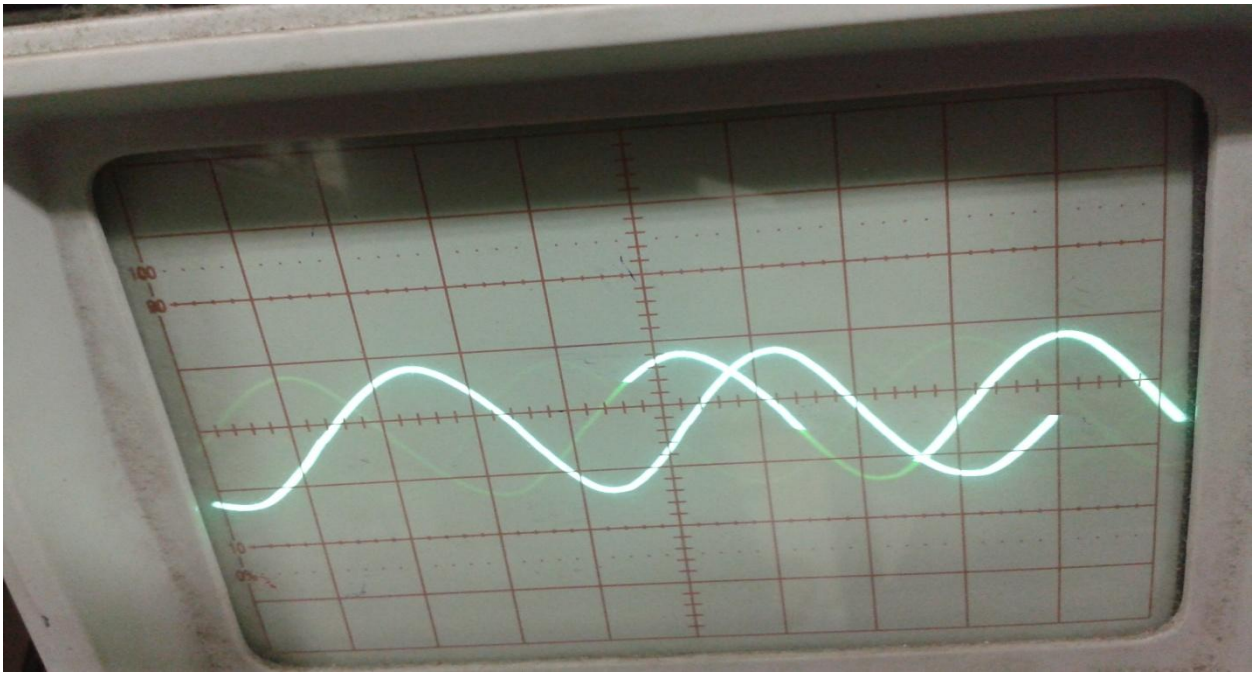

Fig. 4.2.3 : PLL output without offset to be fed to MPPT module

4.3 Grid Tie setup

Inverter was tied to grid using both the strategies with following settings.

4.3.1 SPWM Strategy

V_{dc} = 40V

V_g = 25V rms

L_i= 1mH

L_o=1mH

With above setup inverter was tied to the grid and following measurements and observations were made :

m= 0.80 while the expected value was **0.81.**

I_{dc}= 1.6 A

P_{dc}= 40*1.6=64 W

Ig=2.16 A rms

P_{ac}= 25.54*2.16=55 W

Loss= 9 W

Expected loss= 4*1.6*1.6*.44= 4.5W

THD_v(at PCC)= 2.3%

THD_v(at Inverter terminals)= 28 %

THD_i = 15%

Following waveforms were obtained at PCC.

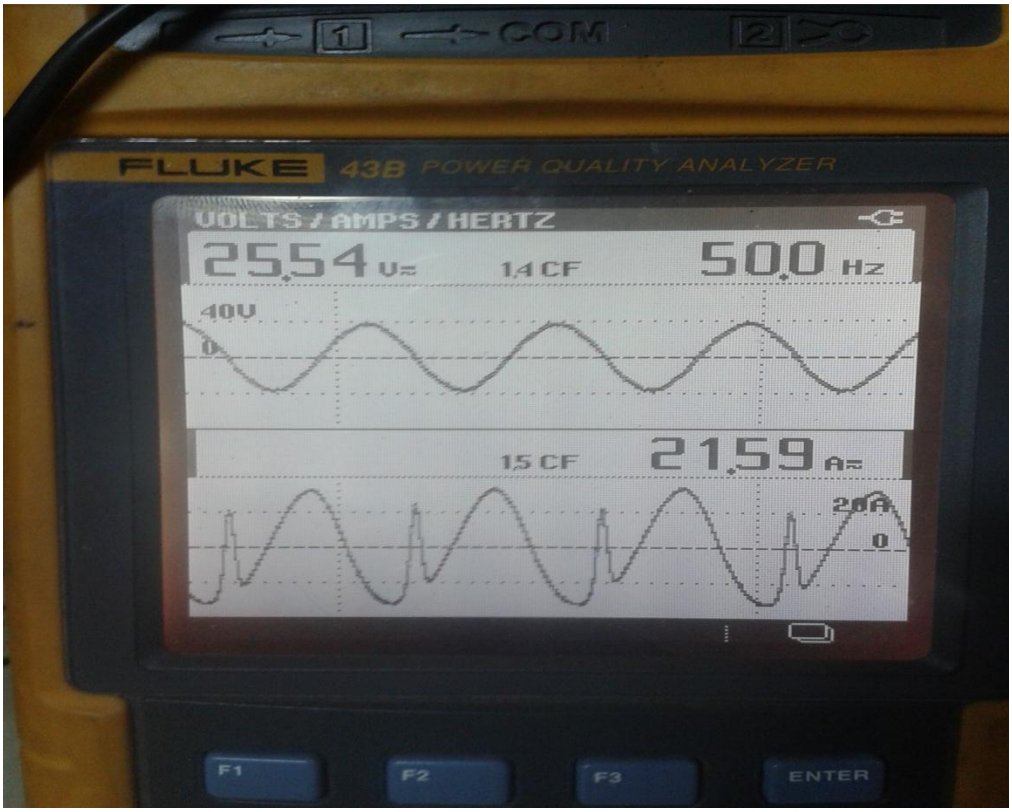

Fig. 4.3.1.1 : Voltage and Current Waveforms at PCC

Fig. 4.3.1.2 : Voltage and current waveforms at lower voltage at inverter terminals

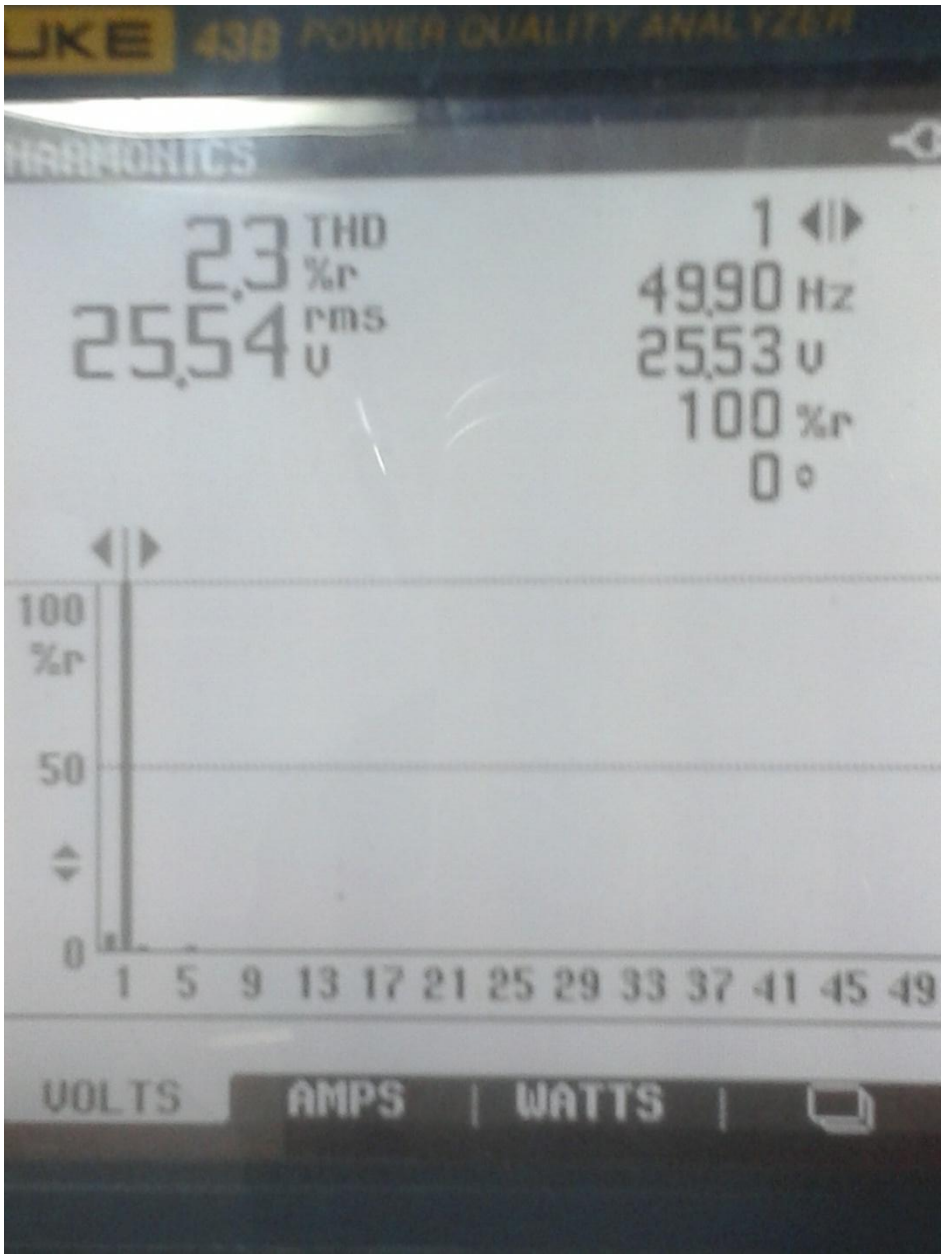

Fig. 4.3.1.3 : Voltage harmonic spectrum at PCC

4.3.2 Discussion

Using SPWM technique with high frequency switching it was expected to feed current at UPF. Power factor was very close to unity. This was possible due to

proper choice of modulation index and power angle. Current harmonics were quite above the standards and should be removed using appropriate filters

4.3.3 HCC Setup

V_{dc} = 40V

V_g = 25V rms

L_i= 1mH

L_o=1mH

With above setup inverter was tied to the grid and following measurements and observations were made :

I_{dc}= 1.5 A

P_{dc}= 40*1.5=60 W

Ig=1.96 A rms

P_{ac}= 25.54*1.96=50 W

Loss= 10 W

Expected loss= 4*1.5*1.5*.44= 3.96W

THD_v(at Inverter terminals)= 38 %

THD_i = 7.5%

Following waveforms were obtained at PCC.

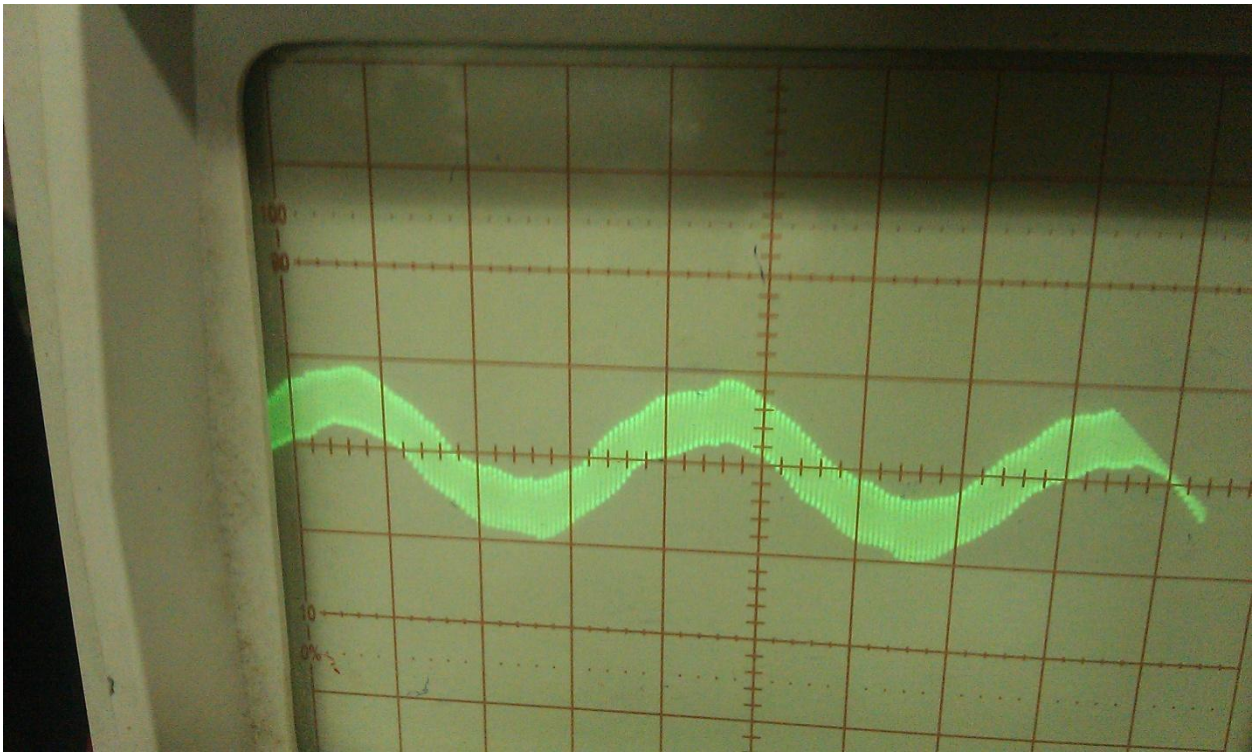

Fig. 4.3.2.1 : Load Current waveform using HCC Strategy

4.3.4 Discussion about HCC strategy

Using HCC technique it was attempted that injected current follows the path of grid voltage. Thus, the UPF standard was easily achieved as clear from the figure 4.3.2.1 .HCC strategy has the capability of working for a very small range of voltages only. Also, it requires DC voltage to be always more than grid voltage while SPWM technique offers flexibility in terms working range on DC side and AC side.

4.4 Comparison between HCC and SPWM techniques

Table 4.4.1 : Comparison between HCC and SPWM techniques

Topics	**HCC**	**SPWM**
THD_v(at PCC)	small	small
THD_v(Inv. terminals)	Very high	Average
THD_i	Very small	More than HCC
Working Range	small	large
Flexibility in operation	small	large
Control Strategies	Simple	Complex

CHAPTER 5

Future Scope

The fabricated inverter feeds a fixed amount of power to the grid.

- A MPPT block is to be included in the inverter so as to change the power being drawn as per the insolation during the particular time of the day. The MPPT block can be implemented as follows:

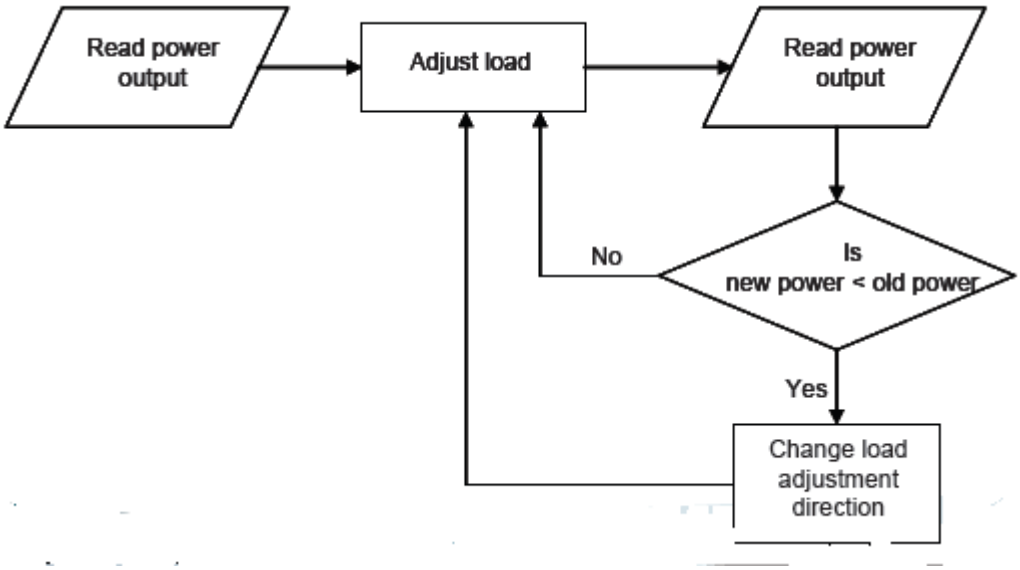

Fig 5.1: MPPT implementation for grid tie PV inverter

- The inverter also has to be provided with protection against the faults in the power systems.
- The inverter though feeds power to the grid but the voltage flicker and the THD are greater than that in the IEEE standards for grid connection. So the inverter has to be equipped with necessary filters etc. to bring the THD and the flicker as per the recommended IEEE standards.

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APPENDIX-A

A.1 IRFP-460 MOSFET specifications

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 9 A		0.22	0.27	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 10V	18.4			A

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				18.4	A
I_{SDM} (2)	Source-drain Current (pulsed)				73.6	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 18.4A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 20A, di/dt = 100A/µs, V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		480		ns
Q_{rr}	Reverse Recovery Charge			5		µC
I_{RRM}	Reverse Recovery Current			21		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

A.2 AD-202, Isolation Amplifier Specifications

AD202/AD204—SPECIFICATIONS (Typical @ 25°C and V_S = 15 V unless otherwise noted.)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1 V/V–100 V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20 ppm/°C typ (±45 ppm/°C max)	*	*	*
vs. Time	±50 ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1 V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	±5 V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60 Hz, Continuous	750 V rms	1500 V rms	750 V rms	1500 V rms
Continuous (AC and DC)	±1000 V Peak	±2000 V Peak	±1000 V Peak	±2000 V Peak
Isolation-Mode Rejection Ratio (IMRR) @ 60 Hz				
R_S ≤ 100 Ω (HI and LO Inputs) G = 1 V/V	110 dB	110 dB	105 dB	105 dB
G = 100 V/V	130 dB	*	*	*
R_S ≤ 1 kΩ (Input HI, LO, or Both) G = 1 V/V	104 dB min	104 dB min	100 dB min	100 dB min
G = 100 V/V	110 dB min	*	*	*
Leakage Current Input to Output @ 240 V rms, 60 Hz	2 µA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1 V/V)	10^{12} Ω	*	*	*
Common-Mode	2 GΩ|4.5 pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ 25°C	±30 pA	*	*	*
vs. Temperature (0°C to 70°C)	±10 nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ 25°C	±5 pA	*	*	*
vs. Temperature (0°C to 70°C)	±2 nA	*	*	*

A.3 AD-633, Analog Multiplier Specifications

T_A = 25°C, V_S = ±15 V, $R_L \geq 2$ kΩ.

Table I.

Parameter	Conditions	AD633J, AD633A Min	Typ	Max	Unit
TRANSFER FUNCTION			$W = \frac{(X1 - X2)(Y1 - Y2)}{10\ V} + Z$		
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	±2[1]	% full scale
T_{MIN} to T_{MAX}			±3		% full scale
Scale Voltage Error	SF = 10.00 V nominal		±0.25%		% full scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% full scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	±1[1]	% full scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	±0.4[1]	% full scale
X Feedthrough	Y nulled, X = ±10 V		±0.3	±1[1]	% full scale
Y Feedthrough	X nulled, Y = ±10 V		±0.1	±0.4[1]	% full scale
Output Offset Voltage			±5	±50[1]	mV
DYNAMICS					
Small Signal Bandwidth	V_O = 0.1 V rms		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/µs
Settling Time to 1%	ΔV = 20 V		2		µs
OUTPUT NOISE					
Spectral Density			0.8		µV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		µV rms
OUTPUT					
Output Voltage Swing		±11[1]			V
Short Circuit Current	R_L = 0 Ω		30	40[1]	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	±10[1]			V
	Common mode	±10[1]			V
Offset Voltage (X, Y)			±5	±30[1]	mV
CMRR (X, Y)	V_{CM} = ±10 V, f = 50 Hz	60[1]	80		dB
Bias Current (X, Y, Z)			0.8	2.0[1]	µA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		±8[1]		±18[1]	V
Supply Current	Quiescent		4	6[1]	mA

[1] This specification was tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All minimum and maximum specifications are guaranteed; however, only this specification was tested on all production units.

A.4 4046B, Single Phase PLL, Specifications

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
VCO Section											
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	Term. 4 driving CMOS	0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
		0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	e.g. Term.3	0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
		0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA
Phase Comparator Section											
Total Device Current, I_{DD} Max. Term. 14 open, Term. 5 = V_{DD}	–	0,5	5	0.2				–	0.1	0.2	mA
	–	0,10	10	1				–	0.5	1	
	–	0,15	15	1.5				–	0.75	1.5	
	–	0,20	20	4				–	2	4	
Term. 14 = V_{SS} or V_{DD}, Term. 5 = V_{DD}	–	0,5	5	20				–	10	20	µA
	–	0,10	10	40				–	20	40	
	–	0,15	15	80				–	40	80	
	–	0,20	20	160				–	80	160	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
DC Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level V_{IL} Max.	0.5,4.5	–	5			1.5		–	–	1.5	V
	1,9	–	10			3		–	–	3	
	1.5,13.5	–	15			4		–	–	4	
High Level V_{IH} Min.	0.5,4.5	–	5			3.5		3.5	–	–	
	1,9	–	10			7		7	–	–	
	1.5,13.5	–	15			11		11	–	–	

Appendix-B

B.1 PLL Schematic and PCB

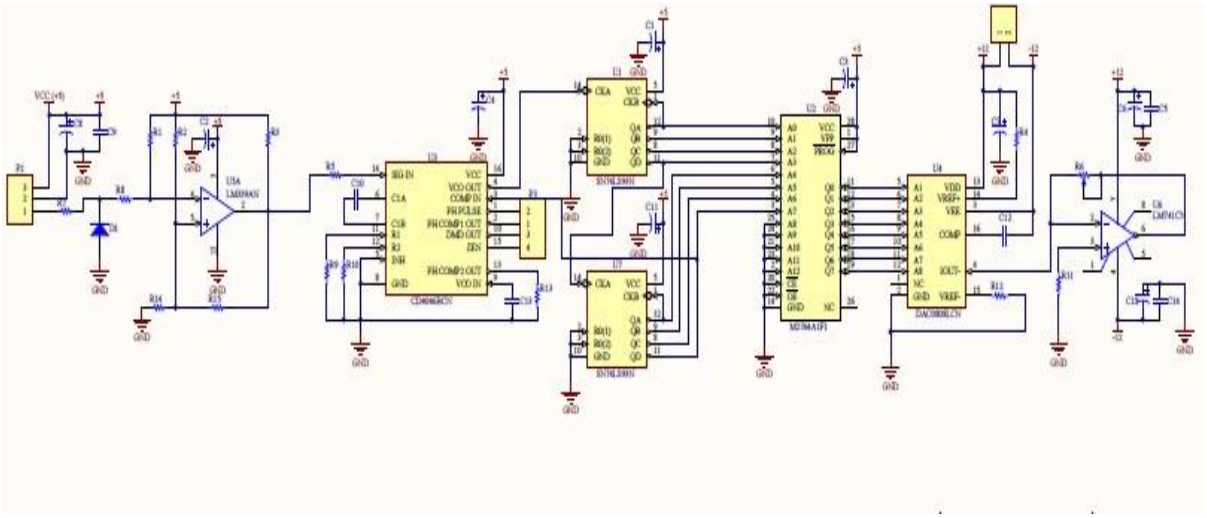


Fig B.1.1: PLL Schematic

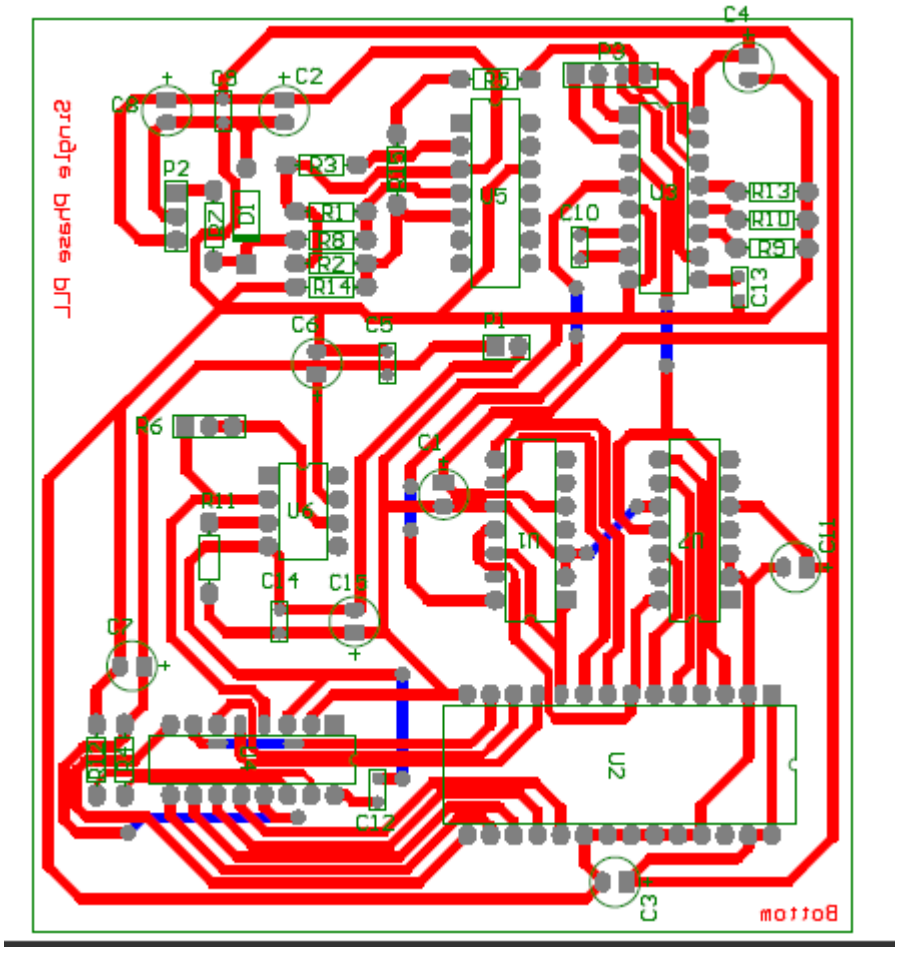
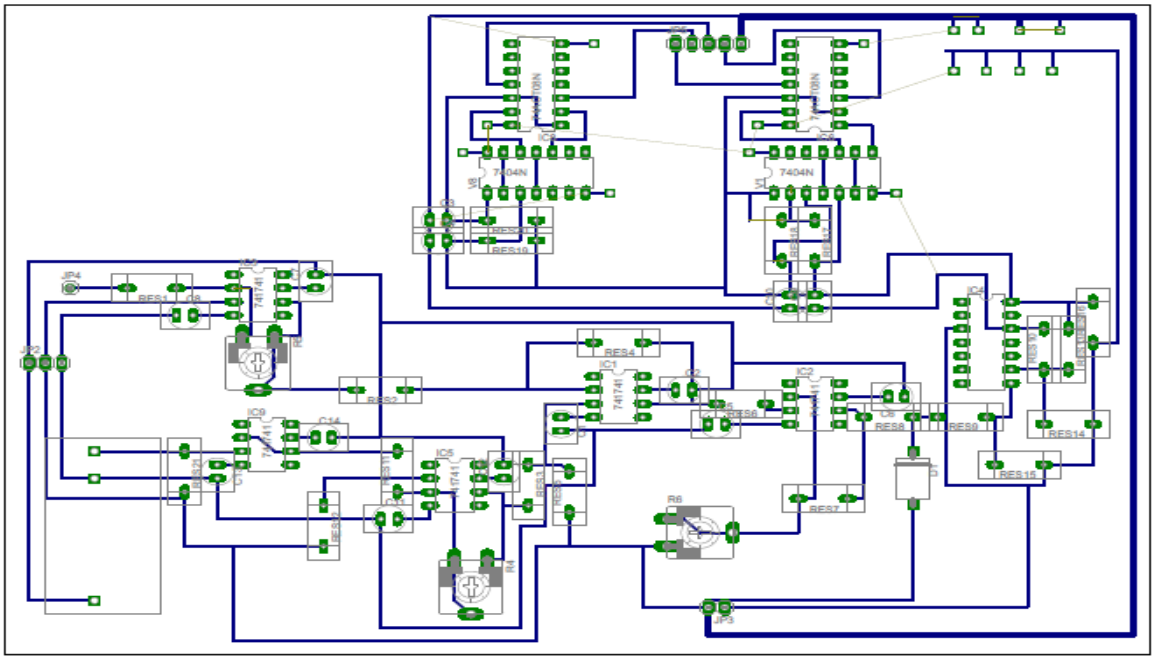
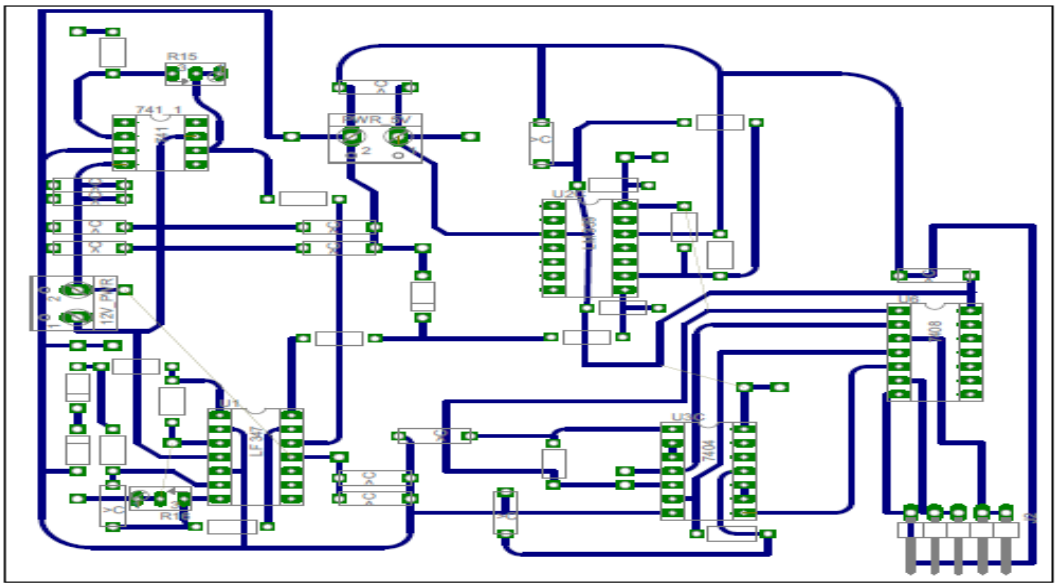


Fig B.1.2: PLL PCB

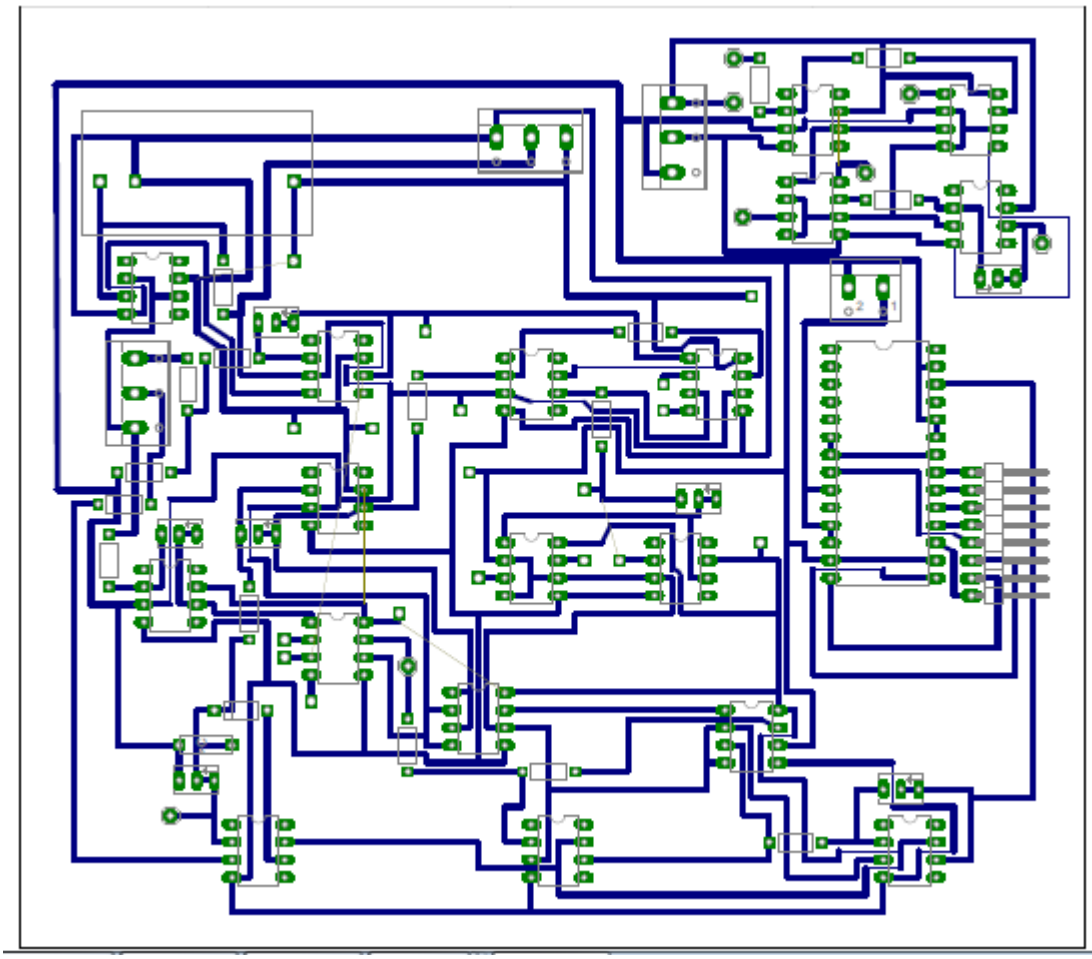
B.2 HCC PCB



B.2 SPWM PCB



B.3 Control Block PCB



Appendix-C

MATLAB code for simulation of solar cell with MPPT tracking:

```
function y = MPPtrackIref(P)

global Pold;
global Iref;
global Increment;

IrefH = 5; % upper limit for the reference current
IrefL = 0; % lower limit for the reference current
DeltaI = 0.02; % reference current increment

if (P < Pold)
   Increment = -Increment; % change direction if P decreased
end

% increment current reference
Iref=Iref+Increment*DeltaI;

% check for upper limit
if (Iref > IrefH)
   Iref = IrefH;
end

% check for lower limit
if (Iref < IrefL)
   Iref = IrefL;
end

% save power value
Pold = P;
% output current reference
y = Iref;
```

Appendix-D

EPROM-2764 data values for the generation of sine wave with different phases leads:

```
CPU     "8051.TBL"
HOF     "INT8"
ORG    0000H
DFB    001H,041H,0A1H,011H,0D1H,071H,089H,029H,069H,059H,0B9H,005H,0C5H,065H,095H
DFB    035H,0F5H,04DH,0ADH,01DH,0DDH,07DH,003H,0C3H,063H,013H,0D3H,0B3H,00BH,04BH
DFB    02BH,0EBH,09BH,0DBH,0BBH,0FBH,087H,0C7H,0A7H,0E7H,097H,0D7H,0B7H,077H,0F7H
DFB    08FH,04FH,02FH,0AFH,06FH,0EFH,01FH,09FH,05FH,0DFH,0DFH,03FH,0BFH,0BFH,07FH
DFB    07FH,07FH,07FH,0FFH,0FFH,0FFH,07FH,07FH,07FH,07FH,0BFH,0BFH,03FH,0DFH,0DFH
DFB    05FH,09FH,01FH,0EFH,06FH,0AFH,02FH,04FH,08FH,0F7H,077H,0B7H,0D7H,097H,0E7H
DFB    0A7H,0C7H,087H,0FBH,0BBH,0DBH,09BH,0EBH,02BH,04BH,00BH,0B3H,0D3H,013H,063H
DFB    0C3H,003H,07DH,0DDH,01DH,0ADH,04DH,0F5H,035H,095H,065H,0C5H,005H,0B9H,059H
DFB    069H,029H,089H,071H,0D1H,011H,0A1H,041H,0FEH,0DEH,01EH,0AEH,04EH,0F6H,036H
DFB    096H,066H,046H,0FAH,03AH,09AH,06AH,0CAH,00AH,072H,0D2H,012H,0A2H,042H,0FCH
DFB    0BCH,05CH,0ECH,0ACH,04CH,00CH,0B4H,0D4H,094H,064H,024H,044H,004H,078H,038H
DFB    058H,018H,068H,028H,048H,088H,0F0H,070H,030H,0D0H,090H,010H,0E0H,060H,0A0H
DFB    020H,0C0H,0C0H,040H,040H,040H,080H,080H,080H,080H,000H,000H,000H,000H,080H
DFB    080H,080H,080H,040H,040H,040H,0C0H,0C0H,020H,020H,0A0H,060H,0E0H,010H,090H
DFB    0D0H,030H,070H,0F0H,088H,048H,028H,068H,018H,058H,038H,078H,004H,044H,024H
DFB    064H,094H,0D4H,0B4H,00CH,04CH,0ACH,0ECH,05CH,0BCH,0FCH,042H,0A2H,012H,0D2H
DFB    072H,00AH,0CAH,06AH,09AH,03AH,0FAH,046H,066H,096H,0B6H,08EH,02EH,0EEH,0DEH
DFB    0FEH
```