Mohit Bagade

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Education

University of Southern California Aug 2022 - May 2025
Masters of Science in Computer Engineering *Los Angeles, CA*

Vishwakarma Institute of Technology (Pune University) Aug 2017 - Jun 2021
Bachelor of Technology in Electronics Engineering *Pune, India*

Experience

USC Center for Advanced Manufacturing | *Graduate Student Researcher* | *Los Angeles* June 2024 - Present
- Designed and developed a compact, flexible PCB using Eagle CAD to wirelessly collect real-time data from flexible sensors for robotic performance monitoring.
- Developed a Bluetooth-enabled system to wirelessly transmit real-time sensor data to a computer for monitoring robot movements.

USC Core Centre for Excellence in Nano Imaging | *Student Worker* | *Los Angeles* May 2024 - Dec 2024
- Developed a secure authentication system integrating ESP32 microcontroller and Raspberry Pi, enabling real-time validation using college ID cards through custom firmware.
- Designed and implemented custom digital circuits and communication interfaces using I2C protocol to ensure seamless and encrypted data transfer between components during the authentication process.

PrimeNumerics Consulting Pvt. Ltd. | *Intern* | *Pune, India* Jan 2021 - May 2021
- Applied deep learning for image recognition using CNNs with Keras and TensorFlow, improving prediction accuracy to 98.1%.
- Deployed the model on H2O.ai for simplifying workflow and automating training

Korea Institute of Science and Technology (KIST) | *Research Assistant* | *Seoul, S. Korea* Jun 2019 - Jul 2019
- Synthesized Lead Sulphide (PbS) Quantum Dots using the Hot Injection method, optimizing reaction parameters to control particle size and uniformity.
- Performed photovoltaic efficiency analysis on quantum dot solar cells by characterizing absorption spectra and optimizing material processing for improved conversion efficiency.

Projects

Cardinal Bidirectional Torus NoC Router Jan 2024 - May 2024
- Developed a 4x4 torus NoC router using source routing, 64-bit packets, and virtual cut-through switching with dual virtual channels.
- Integrated clock gating techniques into the processor design to reduce dynamic power consumption by 12% without sacrificing performance.
- Implemented a dedicated forwarding unit to optimize data flow and reduce overall processor latency.

Memory System Performance Analysis and Cache Hierarchy Optimization Aug 2023 - Dec 2023
- Implemented and simulated multiple memory configurations including no-cache, single-level, two-level, and three-level cache hierarchies using gem5.
- Evaluated system performance for each configuration using matrix multiplication benchmarks, measuring impacts on MIPS and memory latency.
- Integrated LPDDR-based low-power memory, analyzed power-performance trade-offs, and reported architectural recommendations for energy-efficient designs.

512-bit SRAM Design Jan 2024 - May 2024
- Designed and simulated a 512-bit SRAM using Cadence Virtuoso, focusing on read/write stability, access time, and power efficiency.
- Optimized layout and performance to improve overall memory subsystem reliability.

Microarchitecture Analysis and Enhancement using gem5 Aug 2023 - Dec 2023
- Designed dynamic scheduling techniques to improve system throughput, leveraging out-of-order execution and instruction-level parallelism, optimizing performance while staying within area and transistor budgets.
- Tuned architectural parameters such as machine width, branch predictors, ALU resources, and memory hierarchy to maximize MIPS performance across control-flow and memory-intensive benchmarks.

Skills

Programming: Verilog, C, C++, Python, Java, PHP, Matlab, MySQL
Computer Architecture: Microarchitecture design, Dynamic scheduling, Out-of-order execution, Instruction-level parallelism, Memory hierarchy optimization, Advanced branch predictors
Hardware Design and Development: Cadence Virtuoso, Autodesk Eagle

Certifications

Digital IC Design Fundamentals v2.0: Cadence Design Systems
Semiconductor 101: Cadence Design Systems