# Mohit Bagade

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## University of Southern California

Masters of Science in Computer Engineering

Vishwakarma Institute of Technology (Pune University)

Aug 2022 - May 2025

Aug 2017 - Jun 2021

Bachelor of Technology in Electronics Engineering

Pune, India

Los Angeles, CA

Experience

EDUCATION

USC Center for Advanced Manufacturing | Graduate Student Researcher | Los Angeles

June 2024 - Present

- Designed a compact, flexible PCB using Eagle CAD for wireless data collection from flexible sensors, enabling real-time robotic performance monitoring.
- Developed a Bluetooth-enabled system to wirelessly transmit real-time sensor data to a computer for monitoring robot joint stress and performance optimization.

USC Core Centre for Excellence in Nano Imaging | Student Worker | Los Angeles

May 2024 - Dec 2024

- Developed a secure authentication system integrating ESP32 microcontroller and Raspberry Pi, enabling real-time validation using college ID cards through custom firmware.
- Designed and implemented custom digital circuits and communication interfaces using I2C protocol to ensure seamless and encrypted data transfer between components during the authentication process.

PrimeNumerics Consulting Pvt. Ltd. | Intern | Pune, India

Jan 2021 - May 2021

- Applied Deep Learning for image recognition and classification using CNNs with Keras and TensorFlow
- Deployed the model on H2O.ai for simplifying workflow and automating training
- Improved the prediction accuracy rates from 84.4% to 95.2% and 98.1%

Korea Institute of Science and Technology (KIST) | Research Assistant | Seoul, S. Korea Jun 2019 - Jul 2019

- Synthesized Lead Sulphide (PbS) Quantum Dots using the Hot Injection method, optimizing reaction parameters to control particle size and uniformity.
- Performed photovoltaic efficiency analysis on quantum dot solar cells by characterizing absorption spectra and optimizing material processing for improved conversion efficiency.

Projects

## Microarchitecture Analysis and Enhancement using gem5

Aug 2023 - Dec 2023

• Designed dynamic scheduling techniques to improve system throughput, leveraging out-of-order execution and instruction-level parallelism. Enhanced microarchitecture designs using gem5 for performance optimization.

# Cardinal Bidirectional Torus NoC Router

Jan 2024 - May 2024

- Developed a torus NoC router using source routing, 64-bit packets, and virtual cut-through switching with dual virtual channels.
- Integrated clock gating techniques into the processor design to minimize dynamic power consumption without sacrificing performance.
- Implemented a dedicated forwarding unit to optimize data flow and reduce overall processor latency.

#### Memory System Performance Analysis

Aug 2023 - Dec 2023

- Implemented and analyzed various memory system configurations using gem5 simulation framework
- Optimized performance metrics by adjusting memory hierarchy structures, cache sizes, and associativity

## Parallel Matrix Multiplication on a 4-core 4-thread Processor (CMP)

- Implemented parallel matrix multiplication on a 4-core 4-thread processor architecture, exploiting thread-level parallelism for accelerated computation
- Enhanced system performance by architectural decisions through analysis of simulation results and identifying bottlenecks by 20%

## 512-bit SRAM Design

Jan 2024 - May 2024

• Designed a 512-bit SRAM using Cadence Virtuoso. Developed and simulated the layout, ensuring optimal performance and minimal power consumption. Analyzed read/write stability and access times to enhance the overall efficiency of the SRAM module

# SKILLS

Programming Languages: Verilog, C, C++, Python, Java, PHP, Matlab, MySQL

Computer Architecture: Microarchitecture design, Dynamic scheduling, Out-of-order execution, Instruction-level parallelism, Memory hierarchy optimization, Advanced branch predictors

Hardware Design and Development: Cadence Virtuoso, Autodesk Eagle

Simulation and Modeling: gem5, AutoML

#### Certifications

Digital IC Design Fundamentals v2.0: Cadence Design Systems

Semiconductor 101: Cadence Design Systems