Jodhpur Institute of Engineering & Technology
SYLLABUS
III - Semester
Branch: CSE (AI and ML)
3AIML4- 23 : Digital Electronics Lab

Credit: 1 **Max. Marks: 50 (IA: 30, ETE: 20)**

0L+0T+2P **End Term Exam: 2 Hours**

Sr. No.	Experiments
1	Introduction to Digital Electronics Lab- Nomenclature of Digital Ics, Specifications, Concept of V_{cc} and Ground.
2	Verify the truth tables of basic logic gates: AND, OR, NOT, NAND, NOR and Ex-OR.
3	Realize OR, AND, NOR, Ex-OR, Ex-NOR using Universal gates.
4	To realize an SOP and POS expression.
5	To verify the truth table of Half adder / Half Subtractor using universal gate.
6	To verify the truth table of Full adder / Full Subtractor.
7	Design 2 bit binary adder, subtractor and adder-subtractor circuit.
8	To verify the truth table of 2-to-1 Multiplexer and 1-to-2 Demultiplexer. Realize the multiplexer using basic gates only.
9	Study of 4 x 1 multiplexer and 1x 4 Demultiplexer circuit and verify the truth table.
10	Study of seven segment led display, perform an experiment to realize 0-9 on seven segment display.
11	To realize and verify the truth table of R-S flip flops with and without clock signal using basic logic gates.

Tools/ software/ language : Hardware kits