

MICROPROCESSOR AND COMPUTER ARCHITECTURE-LAB

UE22CS251B

MPCA-LAB-7

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Question 1:-Caches are important to provide a high performance memory hierarchy to processors.Below is a list of 16-bit memory address references, given as word addresses.

a. 1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221

b. 6, 214, 175, 214, 6, 84, 65, 174, 64, 105, 85, 215

i. For each of the references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one word

blocks. Also, list if each reference is a hit or a miss, assuming the cache is initially empty.

SOLUTION:-(a)For direct mapped cache in *FIRST* case

The screenshot shows the ParaCache software interface with the following sections:

- ParaCache** header with navigation links: Direct Mapped Cache, Fully Associative Cache, 2-Way SA, 4-Way SA, Cache Type Analysis, Virtual Memory, Knowledge Base.
- Write Policies**: Write Back (selected), Write Through, Write On Allocate, Write Around.
- Cache Size (power of 2)**: 16, **Memory Size (power of 2)**: 2048, **Offset Bits**: 1.
- Instruction Breakdown**: Address 0100010 (7 bit), Offset 000 (3 bit), Tag 1 (1 bit).
- Memory Block**: Contains memory locations B. 10B W. 0 through B. 110 W. 1.
- Cache Table** (8 entries):

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0100010	BLOCK 110 WORD 0 - 1	0
1	1	0000000	BLOCK 1 WORD 0 - 1	0
2	1	0000100	BLOCK 22 WORD 0 - 1	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
- Information**: The cycle has been completed. Please submit another instructions.
- Buttons**: Next, Fast Forward.
- Statistics**: Hit Rate : 25%, Miss Rate : 75%.
- List of Previous Instructions** (yellow background):
 - Load 1 [Miss]
 - Load 134 [Miss]
 - Load 212 [Miss]
 - Load 1 [Hit]
 - Load 135 [Hit]
 - Load 213 [Hit]
 - Load 162 [Miss]
 - Load 161 [Miss]
 - Load 2 [Miss]
 - Load 44 [Miss]
 - Load 41 [Miss]
 - Load 221 [Miss]

(b)For direct mapped cache in *SECOND* case

Write Policies

Write Back Write Through
 Write On Allocate Write Around

Cache Size (power of 2)	16
Memory Size (power of 2)	65536
Offset Bits	0

Reset Submit

Instruction

Load (in hex)
List of next 10 Instructions

Gen Random Submit

Information

The cycle has been completed.
Please submit another instructions

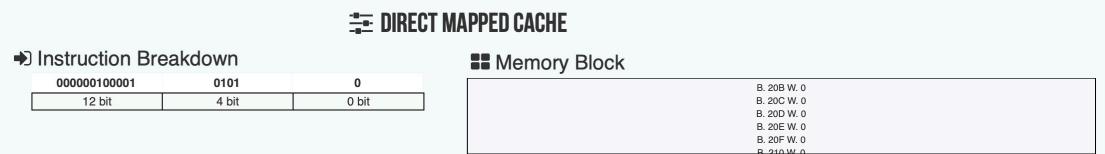
Next Fast Forward

Statistics

Hit Rate : 17%
Miss Rate : 83%

List of Previous Instructions :

- Load 6 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Hit]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Miss]
- Load 64 [Miss]
- Load 105 [Miss]
- Load 85 [Miss]
- Load 215 [Miss]

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	1	000000000110	BLOCK 64 WORD 0 - 0	0
5	1	000000100001	BLOCK 215 WORD 0 - 0	0
6	1	000000000000	BLOCK 6 WORD 0 - 0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0

ii. Repeat the exercise mentioned in case (i) with 2 word blocks and a total size of eight blocks for set associative and fully associative cache mapping.

SOLUTION:-(a)For Fully associative mapped cache
FIRST case

Replacement Policies

 FIFO LRU Random

Write Policies

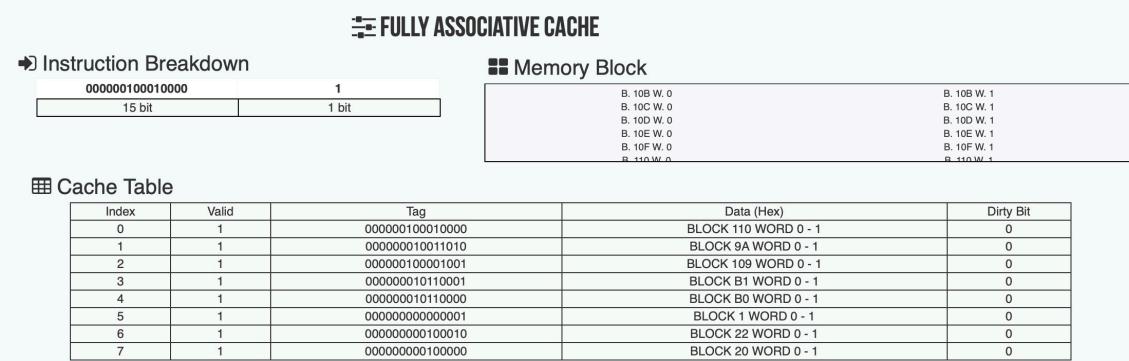
 Write Back Write Through
 Write On Allocate Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Instruction
 (in hex)

List of next 10 Instructions

Information
The cycle has been completed.
Please submit another instructions



Statistics
Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Miss]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

Next Index: 1
Last Index: 0

(b)For Fully associative mapped cache SECOND case

Statistics
Hit Rate : 42%
Miss Rate : 58%

List of Previous Instructions :

- Load 3 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Miss]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Hit]
- Load 64 [Hit]
- Load 105 [Miss]
- Load 85 [Hit]
- Load 215 [Hit]

Next Index: 7
Last Index: 6

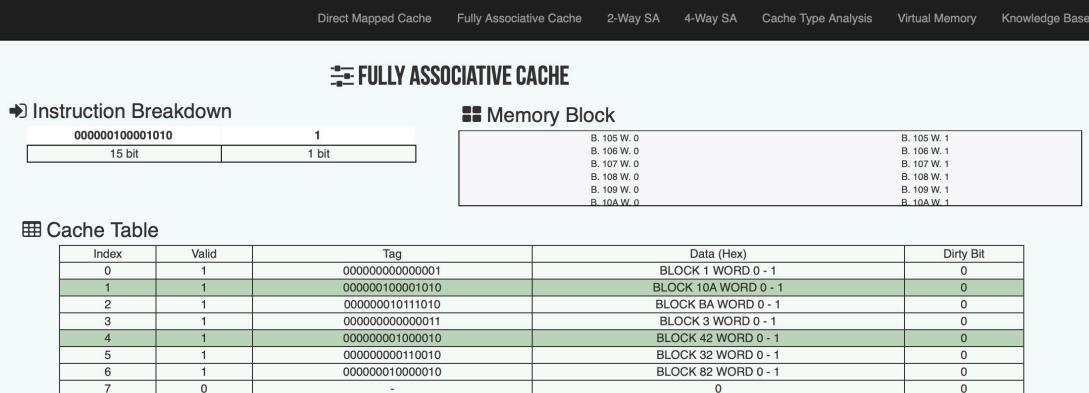
Information
The cycle has been completed.
Please submit another instructions

Statistics
Hit Rate : 42%
Miss Rate : 58%

List of Previous Instructions :

- Load 3 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Miss]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Hit]
- Load 64 [Hit]
- Load 105 [Miss]
- Load 85 [Hit]
- Load 215 [Hit]

Next Index: 7
Last Index: 6



(c)For 2-way set associative mapped cache **FIRST** case

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Reset	Submit
-------	--------

Instruction
 |
List of next 10 Instructions

Information
The cycle has been completed.
Please submit another instructions

Next	Fast Forward
------	--------------

Statistics
Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Miss]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00000010000100	00	1
13 bit	2 bit	1 bit

Memory Block

B. 10B W. 0 B. 10C W. 0 B. 10D W. 0 B. 10E W. 0 B. 10F W. 0 B. 110 W. 0	B. 10B W. 1 B. 10C W. 1 B. 10D W. 1 B. 10E W. 1 B. 10F W. 1 B. 110 W. 1
--	--

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	BLOCK 20 WORD 0 - 1	0
1	1	0	BLOCK 1 WORD 0 - 1	0
2	1	26	B. 9A W. 0 - 1	0
3	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	44	BLOCK 110 WORD 0 - 1	0
1	1	2c	BLOCK B1 WORD 0 - 1	0
2	1	8	BLOCK 22 WORD 0 - 1	0
3	0	-	0	0

(d)For 2-way set associative mapped cache **SECOND** case

Replacement Policies

 FIFO LRU Random

Write Policies

 Write Back Write Through
 Write On Allocate Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Reset	Submit
-------	--------

Instruction
 (in hex) #
List of next 10 Instructions

Information

The cycle has been completed.
Please submit another instructions

Next	Fast Forward
------	--------------

Statistics

Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 6 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Hit]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Miss]
- Load 64 [Hit]
- Load 105 [Miss]
- Load 85 [Miss]
- Load 215 [Miss]

2-WAY SET ASSOCIATIVE CACHE**Instruction Breakdown**

0000001000010	10	1
13 bit	2 bit	1 bit

Memory Block

B. 10A W. 0	B. 10A W. 1
B. 10B W. 0	B. 10B W. 1
B. 10C W. 0	B. 10C W. 1
B. 10D W. 0	B. 10D W. 1
B. 10E W. 0	B. 10E W. 1
B. 10F W. 0	B. 10F W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	10	BLOCK 42 WORD 0 - 1	0
3	1	0	B. 3 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	42	BLOCK 10A WORD 0 - 1	0
3	0	-	0	0

(e)For 4-way set associative mapped cache FIRST case

Replacement Policies

 FIFO LRU Random

Write Policies

 Write Back Write Through
 Write On Allocate Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Reset	Submit
-------	--------

Instruction
 (in hex) #
List of next 10 Instructions

Information

The cycle has been completed.
Please submit another instructions

Next	Fast Forward
------	--------------

Statistics

Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Miss]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

4-WAY SET ASSOCIATIVE CACHE**Instruction Breakdown**

000000100001000	0	1
14 bit	1 bit	1 bit

Memory Block

B. 110 W. 0	B. 110 W. 1
B. 111 W. 0	B. 111 W. 1
B. 112 W. 0	B. 112 W. 1
B. 113 W. 0	B. 113 W. 1
B. 114 W. 0	B. 114 W. 1
B. 115 W. 0	B. 115 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	10	B. 20 W. 0 - 1	0
1	1	84	B. 109 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	88	B. 110 W. 0 - 1	0
1	1	58	B. B1 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	11	B. 22 W. 0 - 1	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	11	B. 22 W. 0 - 1	0

(f) For 4-way set associative mapped cache FIRST case

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2) 16

Memory Size (power of 2) 65536

Offset Bits 1

Instruction

Load |

List of next 10 Instructions

Information
The cycle has been completed.
Please submit another instructions

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00000010000101	0	1
14 bit	1 bit	1 bit

Memory Block

B. 10A W. 1
B. 10B W. 0
B. 10C W. 0
B. 10D W. 0
B. 10E W. 0
B. 10F W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	41	B. 82 W. 0 - 1	0
1	1	1	B. 3 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	85	B. 10A W. 0 - 1	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	21	B. 42 W. 0 - 1	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	19	B. 32 W. 0 - 1	0
1	0	-	0	0

Statistics

- Hit Rate : 42%
- Miss Rate : 58%

List of Previous Instructions :

- Load 6 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Hit]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Hit]
- Load 64 [Hit]
- Load 105 [Miss]
- Load 85 [Hit]
- Load 215 [Miss]

Question 2:-Calculate the total number of bits required for the cache listed in the table, assuming a 16-bit address. Given that total size of the closest fully associative mapped cache with 64 word blocks.

SOLUTION:- (a)For closest associative mapped cache for FIRST case

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Reset **Submit**

Instruction
Load (in hex)
List of next 10 Instructions
Gen Random **Submit**

Information
The cycle has been completed.
Please submit another instructions

Next **Fast Forward**

FULLY ASSOCIATIVE CACHE

Instruction Breakdown
0000001000100000 1
15 bit 1 bit

Memory Block

B. 110 W. 0	B. 110 W. 1
B. 111 W. 0	B. 111 W. 1
B. 112 W. 0	B. 112 W. 1
B. 113 W. 0	B. 113 W. 1
B. 114 W. 0	B. 114 W. 1
B. 115 W. 0	B. 115 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000001000100000	BLOCK 110 WORD 0 - 1	0
1	1	000000010011010	BLOCK 9A WORD 0 - 1	0
2	1	000000100001001	BLOCK 109 WORD 0 - 1	0
3	1	000000010110001	BLOCK B1 WORD 0 - 1	0
4	1	000000010110000	BLOCK B0 WORD 0 - 1	0
5	1	000000000000001	BLOCK 1 WORD 0 - 1	0
6	1	000000000100010	BLOCK 22 WORD 0 - 1	0
7	1	000000000100000	BLOCK 20 WORD 0 - 1	0

Statistics
Hit Rate : 25%
Miss Rate : 75%

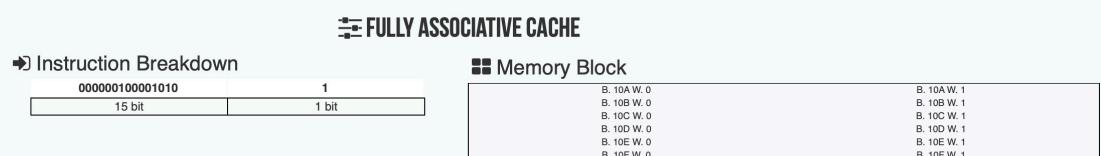
List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Miss]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

Next Index: 1
Last Index: 0

(b)For closest associative mapped cache for SECOND case

Replacement Policies		
<input checked="" type="radio"/> FIFO	<input type="radio"/> LRU	<input type="radio"/> Random
Write Policies		
<input checked="" type="radio"/> Write Back	<input type="radio"/> Write Through	
<input checked="" type="radio"/> Write On Allocate	<input type="radio"/> Write Around	
Cache Size (power of 2)	16	
Memory Size (power of 2)	65536	
Offset Bits	1	
<input type="button" value="Reset"/>		<input type="button" value="Submit"/>
Instruction		
<input type="button" value="Load"/> <input type="text" value="I"/>		
List of next 10 Instructions		
<input type="button" value="Gen. Random"/>	<input type="button" value="Submit"/>	
Information		
The cycle has been completed. Please submit another instructions		
<input type="button" value="Next"/> <input type="button" value="Fast Forward"/>		
Statistics Hit Rate : 50% Miss Rate : 50%		
List of Previous Instructions : <ul style="list-style-type: none"> • Load 6 [Miss] • Load 214 [Miss] • Load 175 [Miss] • Load 214 [Hit] • Load 6 [Hit] • Load 84 [Miss] • Load 65 [Miss] • Load 174 [Hit] • Load 64 [Hit] • Load 105 [Miss] • Load 85 [Hit] • Load 215 [Hit] 		
Next Index: 6		
Last Index: 5		

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000000000000011	BLOCK 3 WORD 0 - 1	0
1	1	000000100001010	BLOCK 10A WORD 0 - 1	0
2	1	000000010111010	BLOCK BA WORD 0 - 1	0
3	1	000000001000010	BLOCK 42 WORD 0 - 1	0
4	1	000000000110010	BLOCK 32 WORD 0 - 1	0
5	1	000000010000010	BLOCK B2 WORD 0 - 1	0
6	0	-	0	0
7	0	-	0	0

Question 3:-Calculate the total number of bits required for the cache listed in the table, assuming a 16-bit address. Given that total size of the closest set associative mapped cache with 32 word blocks.

SOLUTION:-(a)For closest associative mapped cache for FIRST case

(I)For 2-way set associative mapped cache

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2) 16 **Memory Size (power of 2)** 65536 **Offset Bits** 1

Instruction Breakdown
0000001000100 00 1
13 bit 2 bit 1 bit

Memory Block

B.110 W. 0	B.110 W. 1
B.111 W. 0	B.111 W. 1
B.112 W. 0	B.112 W. 1
B.113 W. 0	B.113 W. 1
B.114 W. 0	B.114 W. 1
B.115 W. 0	B.115 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	BLOCK 20 WORD 0 - 1	0
1	1	0	BLOCK 1 WORD 0 - 1	0
2	1	26	B. 9A W. 0 - 1	0
3	0	-	0	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	44	BLOCK 110 WORD 0 - 1	0
1	1	2c	BLOCK B1 WORD 0 - 1	0
2	1	8	BLOCK 22 WORD 0 - 1	0
3	0	-	0	0

Information
The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics
Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Miss]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

(II)For 4-way set associative mapped cache

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2) 16 **Memory Size (power of 2)** 65536 **Offset Bits** 1

Instruction Breakdown
00000010001000 0 1
14 bit 1 bit 1 bit

Memory Block

B.110 W. 0	B.110 W. 1
B.111 W. 0	B.111 W. 1
B.112 W. 0	B.112 W. 1
B.113 W. 0	B.113 W. 1
B.114 W. 0	B.114 W. 1
B.115 W. 0	B.115 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	10	B. 20 W. 0 - 1	0
1	1	84	B. 109 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	88	B. 110 W. 0 - 1	0
1	1	58	B. B1 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	58	B. B0 W. 0 - 1	0
1	1	0	B. 1 W. 0 - 1	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	11	B. 22 W. 0 - 1	0
1	0	-	0	0

Information
The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics
Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Miss]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

(b) For closest associative mapped cache for SECOND case

(I) For 2-way set associative mapped cache

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

FIFO LRU Random

Write Policies

Write Back Write Through
 Write On Allocate Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Reset	Submit
-------	--------

Instruction
Load
List of next 10 Instructions

Information
The cycle has been completed.
Please submit another instructions

Next	Fast Forward
------	--------------

Statistics
Hit Rate : 25%
Miss Rate : 75%

List of Previous Instructions :

- Load 6 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Hit]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Miss]
- Load 64 [Hit]
- Load 105 [Miss]
- Load 85 [Hit]
- Load 215 [Miss]

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown
0000001000010 10 1
13 bit 2 bit 1 bit

Memory Block

B. 10A W. 0	B. 10A W. 1
B. 10B W. 0	B. 10B W. 1
B. 10C W. 0	B. 10C W. 1
B. 10D W. 0	B. 10D W. 1
B. 10E W. 0	B. 10E W. 1
B. 10F W. 0	B. 10F W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	10	BLOCK 42 WORD 0 - 1	0
3	1	0	B. 3 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	42	BLOCK 10A WORD 0 - 1	0
3	0	-	0	0

(II) For 4-way set associative mapped cache

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

FIFO LRU Random

Write Policies

Write Back Write Through
 Write On Allocate Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 65536
Offset Bits 1

Reset	Submit
-------	--------

Instruction
Load
List of next 10 Instructions

Information
The cycle has been completed.
Please submit another instructions

Next	Fast Forward
------	--------------

Statistics
Hit Rate : 42%
Miss Rate : 58%

List of Previous Instructions :

- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Hit]
- Load 6 [Hit]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Miss]
- Load 64 [Hit]
- Load 105 [Miss]
- Load 85 [Hit]
- Load 215 [Miss]

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown
0000001000010 0 1
14 bit 1 bit 1 bit

Memory Block

B. 10A W. 0	B. 10A W. 1
B. 10B W. 0	B. 10B W. 1
B. 10C W. 0	B. 10C W. 1
B. 10D W. 0	B. 10D W. 1
B. 10E W. 0	B. 10E W. 1
B. 10F W. 0	B. 10F W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	41	B. 82 W. 0 - 1	0
1	1	1	B. 3 W. 0 - 1	0
0	1	85	B. 10A W. 0 - 1	0
1	0	-	0	0
0	1	21	B. 42 W. 0 - 1	0
1	0	-	0	0
0	1	19	B. 32 W. 0 - 1	0
1	0	-	0	0

Question 3:-Try using PARACACHE SIMULATOR for the above exercise and also for the following configuration .

- a. Cache Size: 32 words
- b. Memory Size: 131072 words[main memory].
- c. Block Size: 4 words.
- d. Use Write back policy
- e. Also, repeat the exercise for Write through policy.
- f. Sequence of memory addresses as given above.

SOLUTION:-(a)Calculate the total number of bits required for the cache listed in the table, assuming a 16-bit address. Given that total size of the closest direct-mapped cache with 16 word blocks.

Write Policies

Write Back Write Through

Write On Allocate Write Around

Cache Size (power of 2)	32
Memory Size (power of 2)	131072
Offset Bits	2

Instruction

(in hex)
List of next 10 Instructions

Information

The cycle has been completed.
Please submit another instructions

Statistics

Hit Rate : 33%
Miss Rate : 67%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Hit]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

000000010001	000	01
12 bit	3 bit	2 bit

Memory Block

B. 88 W. 0	B. 88 W. 1	B. 88 W. 2	B. 88 W. 3
B. 89 W. 0	B. 89 W. 1	B. 89 W. 2	B. 89 W. 3
B. 8A W. 0	B. 8A W. 1	B. 8A W. 2	B. 8A W. 3
B. 8B W. 0	B. 8B W. 1	B. 8B W. 2	B. 8B W. 3
B. 8C W. 0	B. 8C W. 1	B. 8C W. 2	B. 8C W. 3
B. 8D W. 0	B. 8D W. 1	B. 8D W. 2	B. 8D W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000010001	BLOCK 88 WORD 0 - 3	0
1	1	0000000000010	BLOCK 11 WORD 0 - 3	0
2	0	-	0	0
3	0	-	0	0
4	1	000000010000	BLOCK 84 WORD 0 - 3	0
5	1	000000001001	BLOCK 4D WORD 0 - 3	0
6	0	-	0	0
7	0	-	0	0

(b) Calculate the total number of bits required for the cache listed in the table, assuming a 16-bit address. Given that total size of the closest fully associative mapped cache with 64 word blocks.

Replacement Policies

FIFO LRU Random

Write Policies

Write Back Write Through

Write On Allocate Write Around

Cache Size (power of 2)	32
Memory Size (power of 2)	131072
Offset Bits	2

Instruction

(in hex)
List of next 10 Instructions

Information

The cycle has been completed.
Please submit another instructions

Statistics

Hit Rate : 42%
Miss Rate : 58%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Hit]
- Load 2 [Hit]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

Next Index: 7
Last Index: 6

FULLY ASSOCIATIVE CACHE

Instruction Breakdown

000000010001000	01
15 bit	2 bit

Memory Block

B. 88 W. 0	B. 88 W. 1	B. 88 W. 2	B. 88 W. 3
B. 89 W. 0	B. 89 W. 1	B. 89 W. 2	B. 89 W. 3
B. 8A W. 0	B. 8A W. 1	B. 8A W. 2	B. 8A W. 3
B. 8B W. 0	B. 8B W. 1	B. 8B W. 2	B. 8B W. 3
B. 8C W. 0	B. 8C W. 1	B. 8C W. 2	B. 8C W. 3
B. 8D W. 0	B. 8D W. 1	B. 8D W. 2	B. 8D W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000000000000000	BLOCK 0 WORD 0 - 3	0
1	1	0000000001001101	BLOCK 4D WORD 0 - 3	0
2	1	0000000010001000	BLOCK 84 WORD 0 - 3	0
3	1	0000000001001100	BLOCK 58 WORD 0 - 3	0
4	1	000000000000010001	BLOCK 84 WORD 0 - 3	0
5	1	000000000000010000	BLOCK 10 WORD 0 - 3	0
6	1	000000000100010000	BLOCK 88 WORD 0 - 3	0
7	0	-	0	0

(c) Calculate the total number of bits required for the cache listed in the table, assuming a 16-bit address. Given that total size of the closest set associative mapped cache with 32 word blocks

(I) 2-way set associative mapped cache

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

- FIFO
- LRU
- Random

Write Policies

- Write Back
- Write Through
- Write On Allocate
- Write Around

Cache Size (power of 2) 32 **Memory Size (power of 2)** 131072 **Offset Bits** 2

Instruction (in hex)
List of next 10 Instructions

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	BLOCK 10 WORD 0 - 3	0
1	1	13	B. 4D W. 0 - 3	0
2	0	-	0	0
3	0	-	0	0

Memory Block

B. 88 W. 0	B. 88 W. 1	B. 88 W. 2	B. 88 W. 3
B. 89 W. 0	B. 89 W. 1	B. 89 W. 2	B. 89 W. 3
B. 8A W. 0	B. 8A W. 1	B. 8A W. 2	B. 8A W. 3
B. 8B W. 0	B. 8B W. 1	B. 8B W. 2	B. 8B W. 3
B. 8C W. 0	B. 8C W. 1	B. 8C W. 2	B. 8C W. 3
B. 8D W. 0	B. 8D W. 1	B. 8D W. 2	B. 8D W. 3

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0000000100010	00	01
13 bit	2 bit	2 bit

Information
The cycle has been completed.
Please submit another instructions

Statistics
Hit Rate : 33%
Miss Rate : 67%
List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Hit]
- Load 213 [Hit]
- Load 162 [Miss]
- Load 161 [Hit]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Miss]
- Load 221 [Miss]

Next Fast Forward

(II) 4-way set associative mapped cache

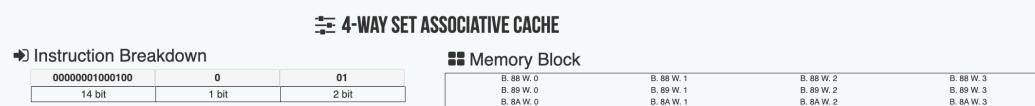
Replacement Policies		
<input checked="" type="radio"/> FIFO	<input type="radio"/> LRU	<input type="radio"/> Random
Write Policies		
<input checked="" type="radio"/> Write Back	<input type="radio"/> Write Through	
<input checked="" type="radio"/> Write On Allocate	<input type="radio"/> Write Around	
Cache Size (power of 2)	32	
Memory Size (power of 2)	131072	
Offset Bits	2	
Reset	Submit	

Instruction	Load	(in hex) 00000001000100
List of next 10 Instructions		
Run Simulation		Submit

Information
The cycle has been completed.
Please submit another instructions

Next | Fast Forward

Statistics			
Hit Rate :	42%		
Miss Rate :	58%		
List of Previous Instructions :			
<ul style="list-style-type: none"> • Load 1 [Hit] • Load 1 [Miss] • Load 212 [Miss] • Load 1 [Hit] • Load 135 [Hit] • Load 213 [Hit] • Load 162 [Miss] • Load 161 [Hit] • Load 2 [Hit] • Load 44 [Miss] • Load 41 [Miss] • Load 221 [Miss] 			

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	44	B. 88 W. 0 - 3	0
1	1	26	B. 4D W. 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	42	B. 84 W. 0 - 3	0
1	1	8	B. 11 W. 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2c	B. 58 W. 0 - 3	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	B. 10 W. 0 - 3	0
1	0	-	0	0

Disclaimer:

- The programs and output submitted is duly written,

verified and executed by me.

- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

A handwritten signature in black ink, appearing to read "V V Mohith".

Name:V V Mohith

SRN:PES2UG22CS641

Section: K

Date:22-03-2024