

Microprocessor and Computer Architecture

UE22CS251B

LAB-5

4th Semester, Academic Year 2023-2024

Date:15-02-2024

Name: V V Mohith	SRN:-PES2UG22CS641	Section:-K
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Week#____5_____

PROGRAM :- 1

Write an ALP to multiply 2 matrices. (3X3)

COMMANDS:-

.data

A: .word 1,2,3,4,5,6,7,8,9

B: .word 1,1,2,2,3,3,4,4,5

C: .space 40

.TEXT

LDR R0, =A

LDR R1, =B

LDR R2, =C

MOV R5, #0

MOV R3, #0

MOV R4, #0

MOV R10, #3

LOOP1:

MLA R6, R3, R10, R4

MOV R6, R6, LSL #2

MLA R7, R3, R10, R5

MOV R7, R7, LSL #2

MLA R8, R5, R10, R4

MOV R8, R8, LSL #2

MOV R11, R6

LDR R6, [R2, R6]

LDR R7, [R0, R7]

LDR R8, [R1, R8]

MLA R9, R7, R8, R6

STR R9, [R2, R11]

ADD R5, R5, #1

```
CMP R5, #3
BNE LOOP1
MOV R5, #0
ADD R4, R4, #1
CMP R4, #3
BNE LOOP1
MOV R4, #0
MOV R5, #0
ADD R3, R3, #1
CMP R3, #3
BNE LOOP1
SWI 0x011
```

OUTPUT SCREENSHOT:

ARMSim# - The ARM Simulator

File View Cache Deb

MemoryView0

Word Size: 8Bit 16Bit 32Bit

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00001000
R1 : 00000000
R2 : 00001048
R3 : 00000003
R4 : 00000000
R5 : 00000000
R6 : 00000045
R7 : 00000009
R8 : 00000005
R9 : 00000072
R10 (s1) : 00000003
R11 (fp) : 00000020
R12 (ip) : 00000000
R13 (sp) : 00011400
R14 (lr) : 00000000
R15 (pc) : 00011400

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : System

0x600000df

MemoryView0

00001048	00000011	0000002F	0000001C	00000026	00000051	00000045	0000003D
00001064	0000008A	00000072	00000000	E59F0078	E59F1078	E59F2078	E3A05000
00001080	E3A03000	E3A04000	E3A0A003	E0264A93	E1A06106	E0275A93	E1A07107
0000109C	E0284A95	E1A08108	E1A0B006	E7926006	E7907007	E7918008	E0296897
000010B8	E782900B	E2855001	E3550003	1AFFFFF0	E3A05000	E2844001	E3540003
000010D4	1AFFFFEC	E3A04000	E3A05000	E2833001	E3530003	1AFFFFE7	EF000011
000010F0	00001000	00001024	00001048	81818181	81818181	81818181	81818181
0000110C	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001128	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001144	81818181	81818181	81818181	81818181	81818181	81818181	81818181
00001160	81818181	81818181	81818181	81818181	81818181	81818181	81818181
0000117C	81818181	81818181	81818181	81818181	81818181	81818181	81818181

OutputView

Console: stdin/stdout/stderr

Loading assembly language file C:\Users\V V Mohith\Downloads\mulmatrix.s
Execution starting ...
Location 113FC: Control transfer to illegal address 00011400
Location 113FC: Control transfer to illegal address 00011400
Execution ending, Instruction Count:17072 Elapsed Time:00:00:00.0962902
Instructions per second:177297

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PROGRAM :-2

Write an ALP using conditional ARM instructions to sort an array of numbers using Bubble Sort Algorithm.

Commands:-

.data

ARRAY: .word 12, 10, 3, 8, 7, 4, 1

.text

.global _start

_start:

MOV r3, #6

LOOP1:

LDR r1, =ARRAY

MOV r2, r1

MOV r7, r3

LOOP2:

LDR r4, [r1]

ADD r6, r1, #4

LDR r5, [r6]

CMP r4, r5

BLE NO_SWAP

STR r5, [r1]

STR r4, [r6]

NO_SWAP:

SUBS r7, r7, #1

ADD r1, r1, #4

BNE LOOP2

SUBS r3, r3, #1

BNE LOOP1

SWI 0x11

OUTPUT SCREENSHOT:

The screenshot displays the ARMSim# - The ARM Simulator interface. The main window is titled "ARMSim# - The ARM Simulator Dept. of Computer Science". The interface includes a menu bar (File, View, Cache, Debug, Watch, Help) and a toolbar with various simulation controls.

The **RegistersView** panel on the left shows the state of the ARM registers. The **General Purpose** tab is selected, and the **Hexadecimal** format is chosen. The registers R0 through R15 are listed, with their values in hexadecimal. The **CPSR Register** is also shown, with fields for Negative (N), Zero (Z), Carry (C), Overflow (V), IRQ Disable, FIQ Disable, Thumb (T), and CPU Mode (System).

The **MemoryView0** panel displays a memory dump starting at address 00001008. The dump shows a sequence of instructions and data, including a loop structure. The instructions are listed in hexadecimal, and the data is shown in a structured format.

The **OutputView** panel at the bottom shows the console output. It displays the loading of the assembly file "C:\Users\V V Mohith\Downloads\bubblesort.s" and the execution starting. The output indicates a control transfer to an illegal address (00011400) at location 113FC. The execution ends with the instruction count (16859) and elapsed time (00:00:00.0857778).

The Windows taskbar at the bottom shows the system clock (9:06 PM, 2/14/2024) and various system icons.

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(assignment question)PROGRAM:-1

Write a program to swap the first and last character of a given string.

COMMANDS:-

```
.data
input_str: .asciz "dog"
.text
.global main
main:
    ldr r0,=input_str
    bl swap_characters
    bl print_string
    mov r7,#1
    svc 0
swap_characters:
```

```
ldrb r1,[r0]
```

```
ldr r2,#2
```

```
add r2,r0,r2
```

```
ldrb r3,[r2]
```

```
strb r1,[r2]
```

```
strb r3,[r0]
```

```
bx lr
```

```
print_string:
```

```
mov r0,r7
```

```
ldr r1,#input_str
```

```
bl strlen
```

```
mov r2,r0
```

```
mov r7,#4
```

```
svc 0
```

```
bx lr
```

```
strlen:
```

```
mov r2,#0
```

```
loop:
```

ldrb r3,[r1],#1

cmp r3,#0

addne r2,r2,#1

bne loop

mov r0,r2

bx lr

OUTPUTSCREENSHOT:-

The screenshot displays the ARMSim - The ARM Simulator interface. The main window is divided into several panes:

- RegistersView:** Shows the state of 16 registers. R0 is 3, R1 is 4208, R2 is 3, R3 is 0, R4 is 0, R5 is 0, R6 is 0, R7 is 4, R8 is 0, R9 is 0, R10 (s1) is 0, R11 (fp) is 0, R12 (ip) is 0, R13 (sp) is 70656, R14 (lr) is 4156, and R15 (pc) is 4164. The CPSR Register shows Negative (N) as 0, Zero (Z) as 1, Carry (C) as 1, Overflow (V) as 0, IRQ Disable as 1, FIQ Disable as 1, Thumb (T) as 0, and CPU Mode as System. The PC value is 0x600000df.
- MemoryView0:** Displays memory addresses and their corresponding values. The address 00001008 is highlighted. The memory contains various values, including 00001008, 00001024, 00001040, 0000105C, 00001078, 00001094, 000010B0, 000010CC, 000010E8, 00001104, 00001120, 0000113C, 00001014, 00001018, 0000101C, 00001020, 00001024, 00001028, 0000102C, 00001030, 00001034, 00001038, 0000103C, 00001040, 00001044, 0000113E4, 0000113E8, 0000113EC, 0000113F0, 0000113F4, 0000113F8, 0000113FC, 000011400, 000011404, 000011408, 00001140C, 000011410, 000011414, 000011418, and 00001141C.
- Assembly Code:** Shows the assembly code being executed. The code includes instructions like `ldrb r1,[r0]`, `ldr r2,#2`, `add r2,r0,r2`, `ldrb r3,[r2]`, `strb r1,[r2]`, `strb r3,[r0]`, `bx lr`, `print_string:`, `mov r0,r7`, `ldr r1,=input_str`, `bl strlen`, `mov r2,r0`, and `mov r7,#4`.
- OutputView:** Shows the output of the program. The console output includes "Loading assembly language file C:\Users\V V Mohith\Downloads\doggyquestion.s" and "Execution starting ...".

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(assignment question)PROGRAM:-2

Given a c Code convert it in its equivalent Arm Code.

a)x = (a + b) - c;

LDR r1, [a]

LDR r2, [b]

ADD r3, r1, r2

LDR r4, [c]

SUB r0, r3, r4

STR r0, [x]

b) $z = (a \ll 2) | (b \& 15);$

```
LDR r5, [a]
LSL r5, r5, #2
LDR r6, [b]
AND r6, r6, #15
ORR r0, r5, r6
STR r0, [z]
```

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

A handwritten signature in black ink, appearing to be 'V V Mohith', written over a horizontal line.

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