1. What is CPI of following code fragment?

(1) LD R1, 24(R2)
(2) LD R2,48(R2)
(3) DADD R3, R2, R1
(4) DADDI R4, R3, #5999
(5) XORI R3, R3, #-1

Comments	1	2	3	4	5	6	7	8	9	10
	(1)	(1)	(1)	(1)	(1)					
		(2)	(2)	(2)	(2)	(2)				
Stall for RAW			(3)	S	(3)	(3)	(3)	(3)		
R3 Forwarded					(4)	(4)	(4)	(4)	(4)	
R3 Forwarded						(5)	(5)	(5)	(5)	(5)

In total, this code fragment takes 10 clock cycles

CPI = $\frac{Clock\ cycles\ taken}{Total\ number\ of\ instructions} = \frac{10}{5} = 2$

2. Identify whether following statements are True or False
   a. Both DRAM and SRAM must be refreshed periodically using dummy read/write operation

   FALSE: Memory latency is calculated suing two measures: Access time and Cycle time.
   Access Time is the time difference between read request and when it is processed.
   Cycle time is time difference between unrelated memory request.
   SRAM as the name suggests is static, it uses more transistors in order to prevent data loss while reading. Thus, the access time and cycle time of SRAM is almost equal.
   DRAM on the other hand is dynamic in the sense that bit data is lost as soon as it is read. Therefore, it must be restored. To prevent the loss of information the bits must be refreshed periodically to prevent data loss.

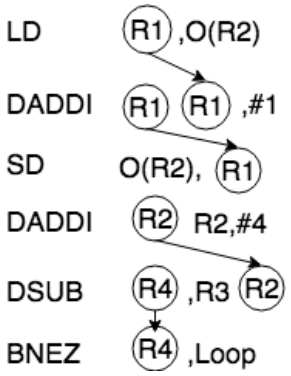
   b. Cache performance is of less importance in faster processors because the processor speed compensates for high access time.

   FALSE:
   Only increase in processor speed will not contribute towards increase in performance of overall system. If the processor speed is increased and memory speed is not considered then it will create instruction stalls. An instruction needs data which is fetched from memory. If memory access time is low then high processor speed is of no use.

3. For following code fragment:

```
Loop:  LD      R1, O(R2)
       DADDI   R1,R1, #1
       SD      O(R2), R1
       DADDI   R2, R2, #4
       DSUB    R4, R3, R2
       BNEZ    R4, Loop
```

a. List all data dependencies in the code above



b. Pipeline timing chart of above instruction for a 5-stage pipeline.

i. No Forwarding

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD	F	D	Ex	M	W													
DADDI		F	S	S	D	Ex	M	W										
SD					F	S	S	D	Ex	M	W							
DADDI								F	D	Ex	M	W						
DSUB									F	S	S	D	Ex	M	W			
BNEZ												F	S	S	D	Ex	M	W
Outside															F	S	S	
Loop																	F	

Number of cycles required for single iteration of loop is **16 cycles**

ii. With Full Forwarding

	1	2	3	4	5	6	7	8	9	10	11
LD	F	D	Ex	M	W						
DADDI		F	S	D	Ex	M	W				
SD				F	D	Ex	M	W			
DADDI					F	D	Ex	M	W		
DSUB						F	D	Ex	M	W	
BNEZ							F	D	Ex	M	W
Outside								F	S	S	
Loop										F	

Number of cycles required for single iteration of loop is **9 cycles.**

4. Consider three branch instructions which are executed in following order

Branch Instruction	B1	B2	B1	B2	B1	B2	B3	B1	B2	B1	B2	B3	B2
Action	NT	T	NT	T	T	NT	T	NT	T	T	NT	NT	NT

a. Prediction result with a **local predictor** using (2,1) prediction

B2 Execution	Local History	Prediction	Action	New Prediction State			
				NT, NT	NT, T	T, NT	T, T
1	NT, NT	NT	T	T	NT	NT	NT
2	NT, T	NT	T	T	T	NT	NT
3	T, T	NT	NT	T	T	NT	NT
4	T, NT	NT	T	T	T	T	NT
5	NT, T	T	NT	T	NT	T	NT
6	T, NT	T	NT	T	NT	NT	NT

b. Prediction result with a **global predictor** using (2,1) prediction

B2 Execution	Global History	Prediction	Action	New Prediction State			
				NT, NT	NT, T	T, NT	T, T
1	NT, NT	NT	T	T	NT	NT	NT
2	T, NT	NT	T	T	NT	T	NT
3	T, T	NT	NT	T	NT	T	NT
4	T, NT	T	T	T	NT	T	NT
5	T, T	NT	NT	T	NT	T	NT
6	NT, NT	T	NT	NT	NT	T	NT

REFERENCES:

[1]: Wikipedia

[2]: Computer Architecture: A Quantitative Approach

[3]: Udemy.com

[4]: NPTEL Videos