DOCUMENTATION

1) MACHINE ARCHITECTURE

16 Registers - 0 to F
5 flags: zero, carry, sign, parity, overflow
Address space 16 bit: 0000H to FFFFH
Data length - 16 bit word addressable
Offset - 12 bit
Immediate value - 16 bit
Base Register (F) contains Base address of that module which will be used while linking
3 addressing modes:

0 - register - register
1 - Immediate
2 - Base + offset

2) INSTRUCTIONS SUPPORTED

Our assembler supports 25 instructions which are as follows:

INSTRUCTION	HEX EQUIVALENT	DESCRIPTION
ADDRR	0000	Add register to register
ADCRR	1000	Add register to register with carry
ADDIV	0100	Add immediate value to register
ADCIV	1100	Add immediate value to register with carry
ADDBO	0200	Add data[address] to register
ADCBO	1200	Add data[address] to register with carry
SUBRR	2000	Subtract register from register
SBBRR	3000	Subtract register from register with borrow

SUBIV	2100	Subtract immediate value from register
SBBIV	3100	Subtract immediate value from register with borrow
SUBBO	2200	Subtract data[address] from register
SBBBO	3200	Subtract data[address] from register with borrow
MOVRR	4000	Move register to register
MOVIV	4100	Move immediate data to register
MOVST	4201	Move data from register to memory (Store)
MOVLD	4200	Move data from memory to register (Load)
JMPBO	5200	Jump unconditional
JZRBO	6200	Jump on zero
JNZBO	7200	Jump on not zero
JCRBO	8200	Jump on carry
JNCBO	9200	Jump on not carry
JPOBO	A200	Jump on positive
JNEBO	B200	Jump on negative
JEPBO	C200	Jump on even parity
JOPBO	D200	Jump on odd parity

3) Data structures used:

- Machine Operation-code Table
- Pseudo Operation-code Table
- Symbol Table
- Literal Table
- Location Counter