Online Assignmet-3 (Compulsory)				
S.N	**Reg. No.**	**Name**	**Roll No.**	
1	11917313	Kulwant Singh Rathore	RE1901A01	
2	11908266	N Mouli Sharma	RE1901A02	
3	11907889	Mane Shubham Kisan	RE1901A03	**Roll Number 1 to 18**
4	11907676	Tanikanti Venkata Sudheer	RE1901A04	
5	11907347	Kuruva Shiva	RE1901A05	1. Write a Verilog program to:
6	11907434	Yalagada Parimala Mercy	RE1901A06	
7	11906397	Tammana Ganesh	RE1901A07	
8	11904218	Sathavelly Abhilash	RE1901A08	a. Implement 2x1 and 4x1 Multiplexer using conditional Operator.
9	11904463	Mohit Rawat	RE1901A09	
10	11904553	Mohammed Nisam	RE1901A10	
11	11904580	Vajid N O	RE1901A11	b. Design a 16x1 Multiplexer in Data flow model by using 4x1 and 2x1 multiplexers.
12	11904206	Ayush Raja	RE1901A12	
13	11903869	B Praveenraj	RE1901A13	
14	11903891	S S Keerthi Vasan	RE1901A14	
15	11904965	Ranga Mani Kumar	RE1901A15	
16	11904845	Ram Krishna Pattanayak	RE1901A16	
17	11904800	Krishna Pathak	RE1901A17	
18	11905144	Challa Venkateswara Rao	RE1901A18	
19	11905562	Padithapu Chaitanya Kumar	RE1901A19	
20	11905407	Vasamsetti Ramana Sai Durga Sekhar	RE1901A20	
21	11908502	Ganesula Mohan Durga Chandra Teja	RE1901A21	
22	11909921	Kasa Venu	RE1901A22	
23	11909707	Neelima Paleti	RE1901A23	
24	11910130	Dhanireddy Chandramohan Reddy	RE1901A24	**Roll Number 19 to 38**
25	11912339	Hrutik M	RE1901A25	
26	11912592	Pothula Srikanth	RE1901A26	1. Write a Verilog program to:
27	11901768	Tummala Yagna Gopal Chowdary	RE1901A27	
28	11902231	Adireddy Vasu	RE1901A28	a. Implement a Full adder using half adder in data flow model.
29	11902153	Vivekananda Reddy Annapa Reddy	RE1901A29	
30	11902204	Ankit Agrawal	RE1901A30	b. Design 5 bit full adder in data flow model using full adder and half adder mudules.
31	11902259	Musi Jagadeesh	RE1901A31	
32	11902945	Singampalli Yagna Prasad	RE1901A32	
33	11902891	Tamma Trinadh Reddy	RE1901A33	
34	11903118	Yalamati Gnana Deepika	RE1901A34	
35	11903149	Hruthik Sai S	RE1901A35	
36	11903113	Yalamati Jnana Sahithi	RE1901A36	
37	11707041	Ayush Ranjan	RE1901A38	