Assignment Submission Sheet

Term: 321221	**Submission Date: 11-09-2021**	
Lecture Date: 1-09-2021	**Assignment Number: 01**	
Course Code: ECE290	**Section: E1901**	**Group: A**
Registration Number: 11904463	**Student Name: Mohit Rawat**	**Roll No: 09**

1. **Concept Learned**

   This assignment make me learn how to put any small digital circuit in verilog code and give input to circuit and make input and output waveform and to analys the wave.

2. **Key Observations &Insights**

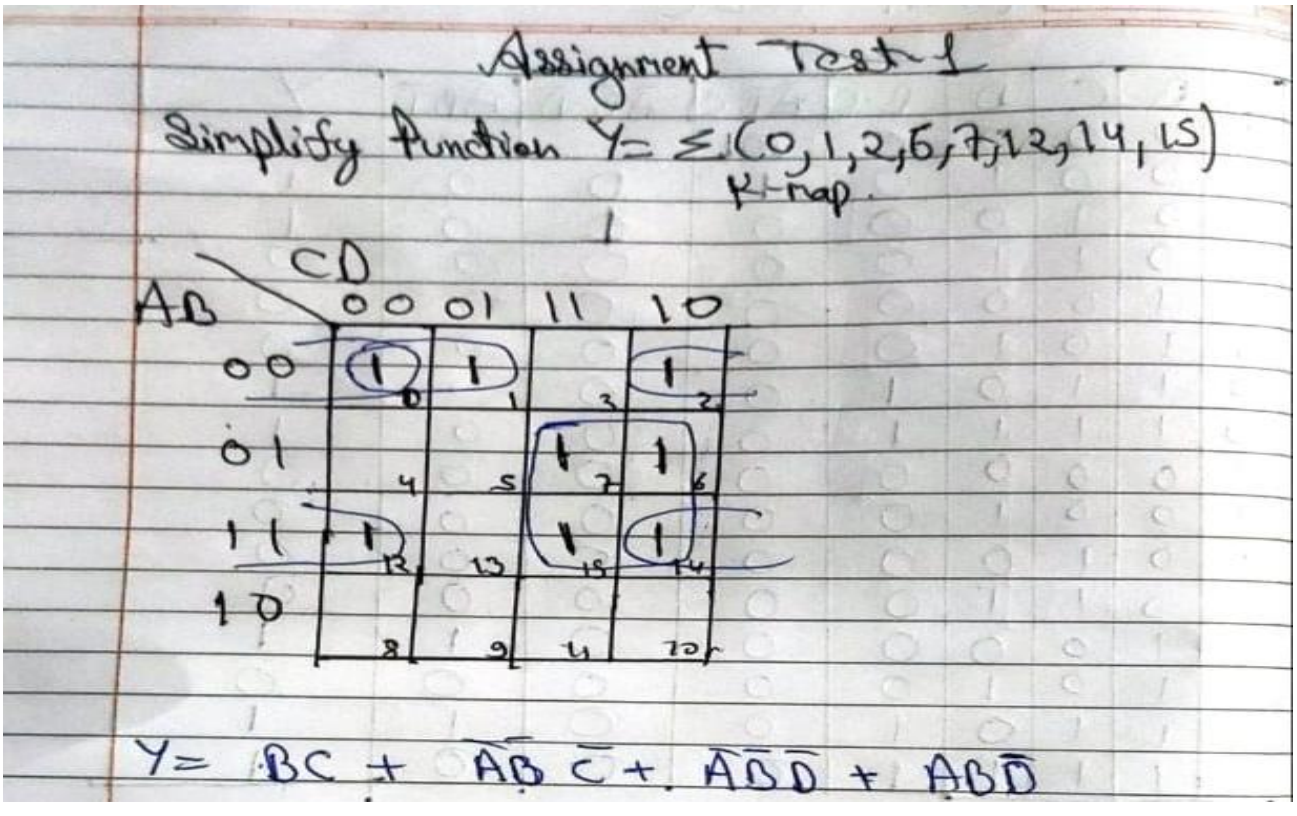
   My main observation from this assignment was the key words of verilog language and there use and other observation was teh wave form which was behaving same as we program in test bench and giving same output as truth table o fcircuit which was previously solved by me.

3. **Application Areas**

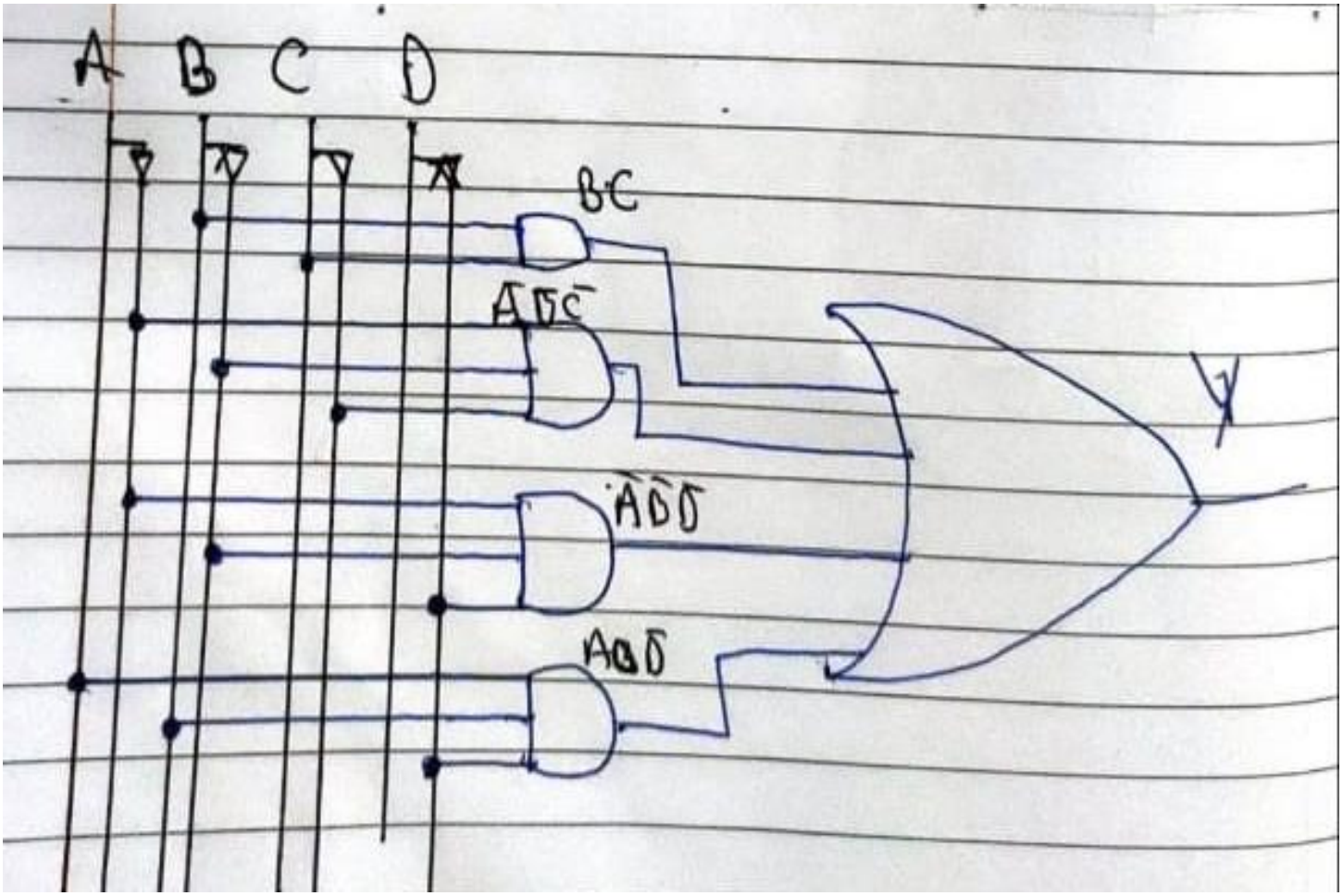
   This was a small part of any higher digital circuit. If we talk about gates than gates are used in all circuits where we need logical output. Verilog HDL is use to design this microprocessor, microcontroller, and other Ics.

4. **Project File / Code / Report / (Work Proof)** (uploaded on UMS as .zipfile)

Simplify Function Y = ∑ (0, 1, 2, 6, 7, 12, 14, 15)



Logic gate Design of function Y



Truth Table for function Y

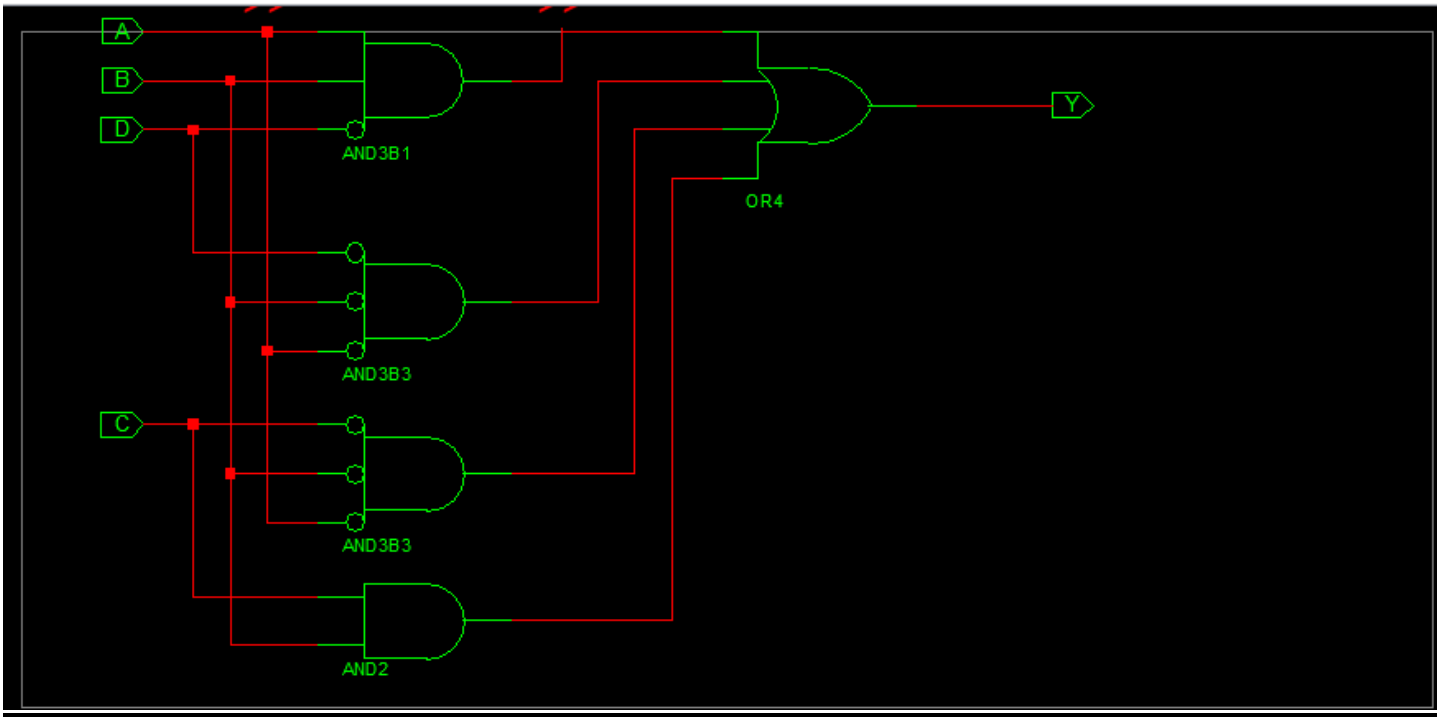
Truth Table

A	B	C	D	B·C	$A\bar{B}\bar{C}$	$A\bar{B}\bar{D}$	$\bar{A}BD$	Y
0	0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	0	1
0	0	1	0	0	0	1	0	1
0	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	0	1
0	1	1	1	1	0	0	0	1
1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0
1	1	0	0	0	0	0	1	1
1	1	0	1	0	0	0	0	0
1	1	1	0	1	0	0	1	1
1	1	1	1	1	0	0	0	1

Verilog code

```
1  `timescale 1ns / 1ps
2  module main(
3     input A,B,C,D,
4     output Y
5  );
6  wire w1, w2, w3, w4;
7
8  not (a, A);
9  not (b, B);
10 not (c, C);
11 not (d, D);
12
13 and (w1,B,C);
14 and (w2,a,b,c);
15 and (w3,a,b,d);
16 and (w4,A,B,d);
17
18 or (Y,w1,w2,w3,w4);
19
20 endmodule
21
```

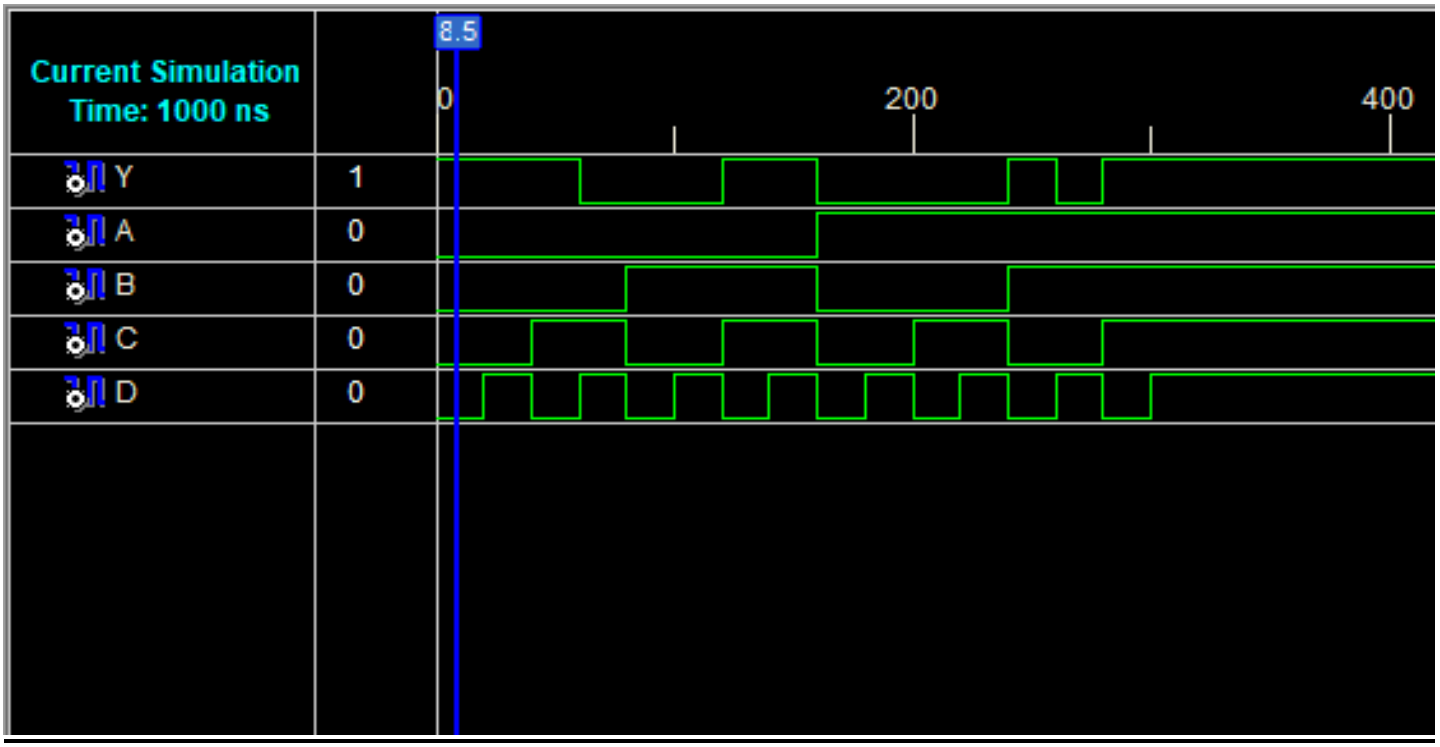
Circuit design



Test bench code

```
1  `timescale 1ns / 1ps
2  module main_tb();
3  reg A, B, C, D;
4  wire Y;
5  localparam period = 20;
6  main (A,B,C,D,Y);
7  initial
8     begin
9     A=0; B=0; C=0; D=0;    #period;
10    A=0; B=0; C=0; D=1;    #period;
11    A=0; B=0; C=1; D=0;    #period;
12    A=0; B=0; C=1; D=1;    #period;
13    A=0; B=1; C=0; D=0;    #period;
14    A=0; B=1; C=0; D=1;    #period;
15    A=0; B=1; C=1; D=0;    #period;
16    A=0; B=1; C=1; D=1;    #period;
17    A=1; B=0; C=0; D=0;    #period;
18    A=1; B=0; C=0; D=1;    #period;
19    A=1; B=0; C=1; D=0;    #period;
20    A=1; B=0; C=1; D=1;    #period;
21    A=1; B=1; C=0; D=0;    #period;
22    A=1; B=1; C=0; D=1;    #period;
23    A=1; B=1; C=1; D=0;    #period;
24    A=1; B=1; C=1; D=1;    #period;
25    end
26 endmodule
27
```

Waveform



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