Assignment Submission Sheet

Term: 321221	**Submission Date: 11-12-2021**	
	Assignment Number: 06	
Course Code: ECE290	**Section: E1901**	**Group: A**
Registration Number: 11904463	**Student Name: Mohit Rawat**	**Roll No: 09**

1. **Concept Learned**

   I have learned how to make Logical gates using cmos technology and how we combine pmos and nmos to make cmos and building the logical gates. After that I have learned how to make switch level program to make cmos gates.

2. **Key Observations &Insights**

   Key observation is the working of pull-up and pull-down networks and how we make all gates using this circuits.

3. **Application Areas**

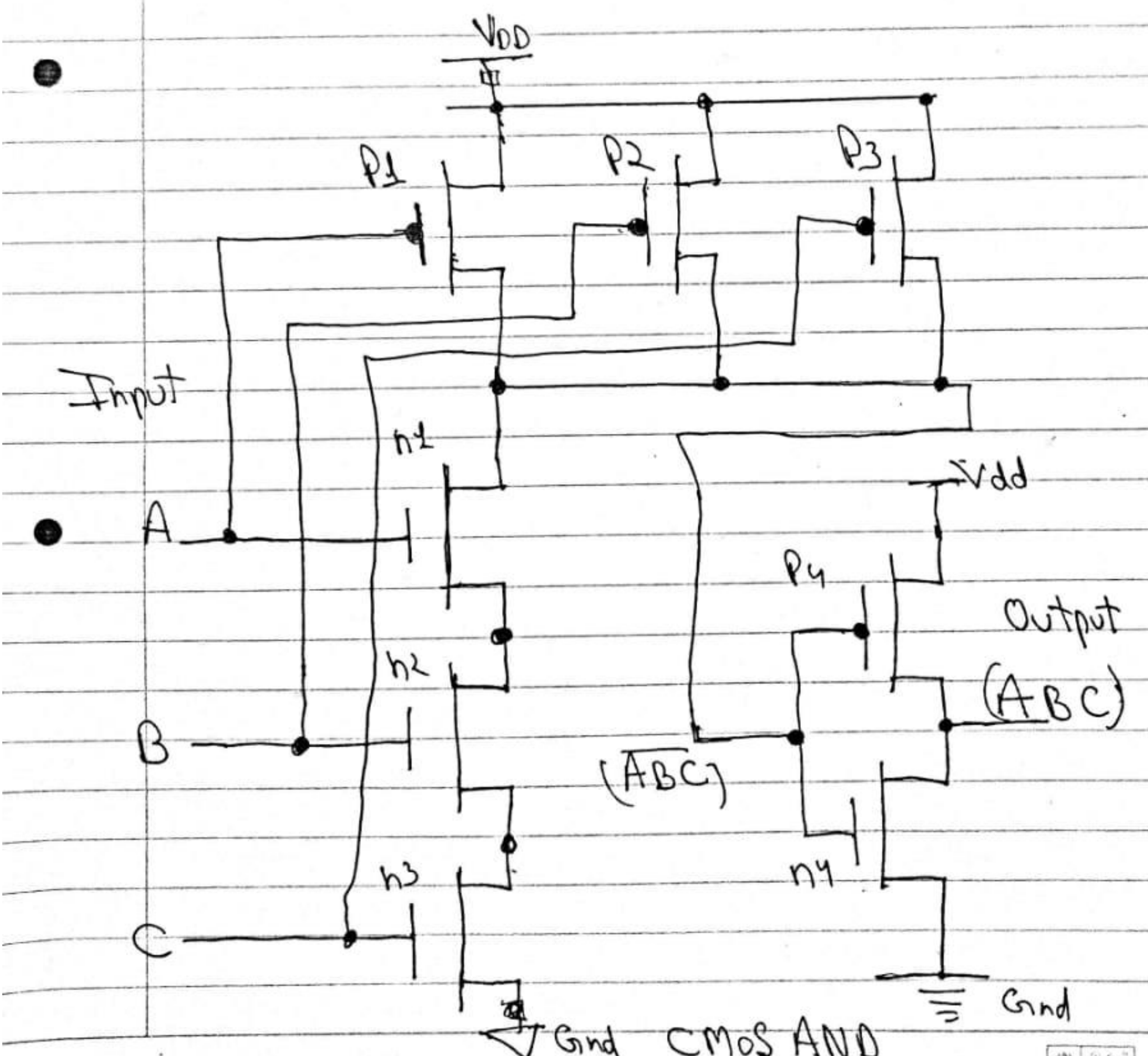
   Application of CMOS technology is in many place like designing gates for ICs and for other embedded systems. We makes processor and other microcontrollers using CMOS technology.

1. Draw and explain CMOS 3-input AND gate and write a Verilog code using Switch level model.
2. 2. Write a Verilog code of OR gate and NOR gate using UDP.

Topic Date

Name: Mohit Rawat Online Assignment- 6.
Section: E1901
Roll no: 09

Q1 Draw & explain CMOS 3-input AND gate and code. write switch level model.



CMOS AND

A CMOS gate is a technology that uses one pmos which is pull-up network and connected to output 1 (V_{DD}) and othe one is nmos which is pull-down network, connected to output 0 (GND). The Combination of nmos & pmos makes cmos and Combination of cmos, we makes logical gates.

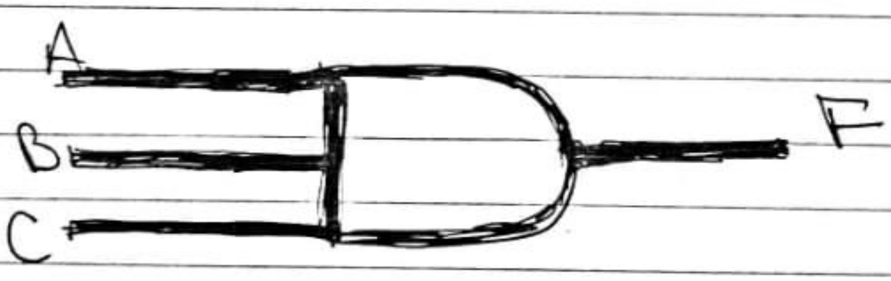
To make CMOS AND, we uses 4-pmos and 4 nmos. In the diagram drawn in previous page, firse 3 pmos are connected in parallel. and upper end is source which is connected to supply in. 3 nmos are connected in series and last portion is connected to ground. Afted combining this nmos & pmos, bath are connected in series. Now it become 3- Input NAND. To make it AND Gate, we use NOT Gate. 1 nmos & 1 pmos 're connected in series to make Not Gate. The output of NAND Gate is connected to NOT Gate so now bath combined make one AND Gate of 3-input.

Topic__________ Date________

Function Table for CMOS 3In - AND Gate

A	B	C	n1	p1	n2	p2	n3	p3	A·B·C	F
L	L	L	off	on	off	on	off	on	H	L
L	L	H	off	on	off	on	on	off	H	L
L	H	L	off	on	on	off	off	on	H	L
L	H	H	off	on	on	off	on	off	H	L
H	L	L	on	off	off	on	off	on	H	L
H	L	H	on	off	off	on	on	off	H	L
H	H	L	on	off	on	of	off	on	H	L
H	H	H	on	off	on	of	on	off	L	H

Logical Symbol.



Verilog Code for 3-input AND Gate.

```
`timescale 1ns/1ps
module CMOS_AND(A,B,C,F);
input A,B,C; // 3 input for AND Gate
output F;    // Output function of AND.

supply1 vdd;   // supply for pmos.
supply0 gnd;   // and nmos

wire F_not, O1, O2;
pmos P1(F_not, vdd, A);   } Pmos in parallel  } NAND
pmos P2(F_not, vdd, B);
pmos P3(F_not, vdd, C);

nmos N1(O2, gnd, C);      } nmos in Series
nmos N2(O1, O2, B);
nmos N3(F_not, O1, A);

pmos P4(F, vdd, F_not);   } not gat to invert
nmos N4(F, gnd, F_not);     NAND gate
                            ad get AND gate.

endmodule
```

Q2.

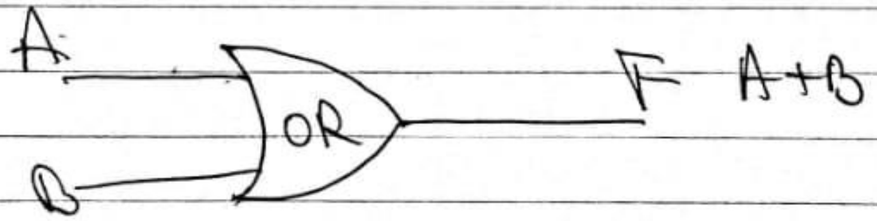
Verilog code of OR gate using UDP.

```
primitive ORgate (F, A, B);
 output F;
 input A, B;

 table
     // A   B  :  F;
        0   0     0
        0   1     1
        1   0     1
        1   1     1
 endtable
endprimitive.
```

Symbol and Truth table of OR Gate.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



Topic __________ Date __________

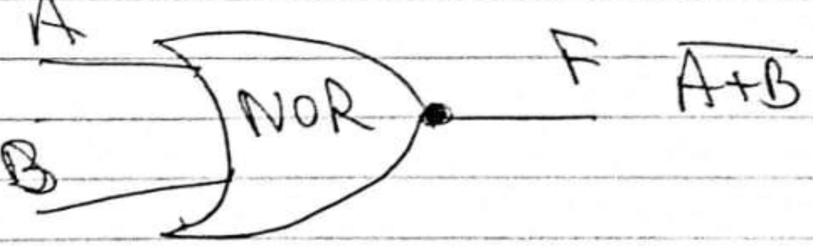
Verilog Cod of NOR gate using UDP

```
primitive NOR_gate (F, A,B);
 output F;
 input A, B;

  table
       // A   B  : F;
          0   0    1
          0   1    0
          1   0    0
          1   1    0
 endtable
endprimitive
```

Symbol and truth table of NOR Gate

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



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