Assignment Submission Sheet

Term: 321221 **Submission Date: 02-11-2021**

Assignment Number: 04

Course Code: ECE290 **Section: E1901** **Group: A**

Registration Number: 11904463 **Student Name: Mohit Rawat** **Roll No: 09**

1. **Concept Learned**

   I have learn about how to make 4 bit up counter using verilog and how to make testbench and give clock in circuit.

2. **Key Observations &Insights**

   Key observation is the output waveform was that it start from 0000 and count up to 1111 and again starting from 0000.

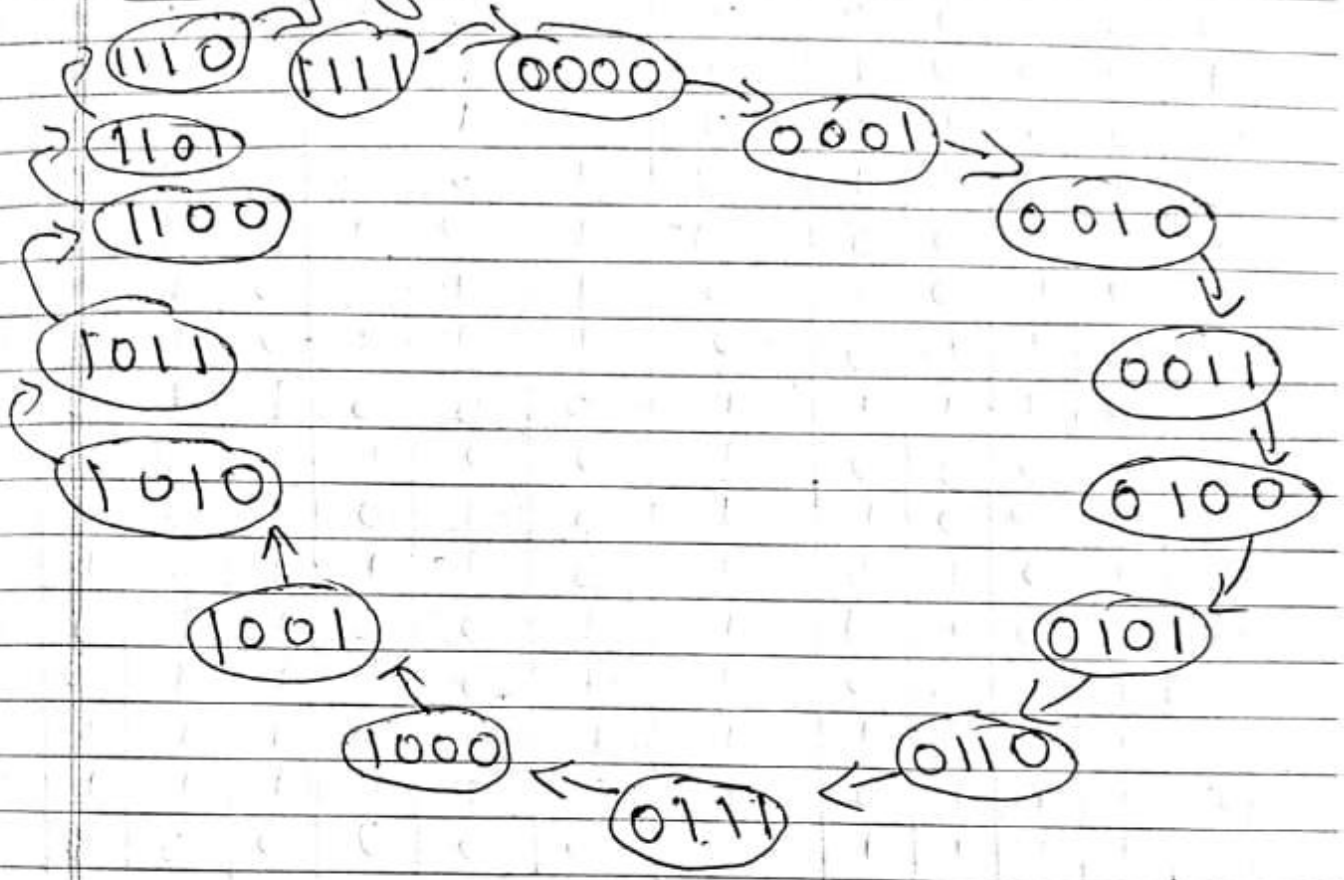
3. **Application Areas**

   Application of counter is in many digital machine like washing machine, micro owner, program counter in computer.

4. A verilog Program to implement 4 bit synchronous Up counter using D- Flip Flop.

Q => A verilog program to implement 4-bit Synchronous up counter using D FF.

Sol => State diagram:-



Excitation table of D Flip Flop:-

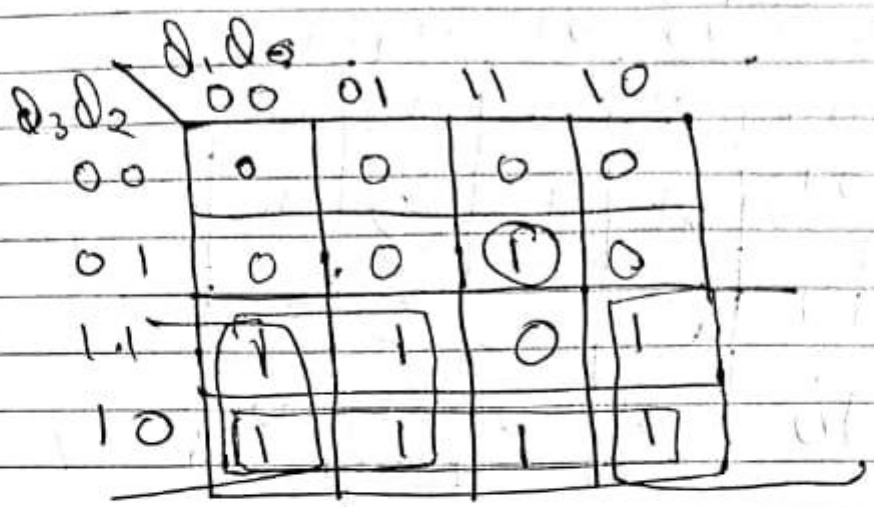
Q	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of 4-bit Up Counter using D FF.

	Present State				Next State				FF input			
	Q_3	Q_2	Q_1	Q_0	$Q_3(t+1)$	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	0
2	0	0	1	0	0	0	1	1	0	0	1	1
3	0	0	1	1	0	1	0	0	0	1	0	0
4	0	1	0	0	0	1	0	1	0	1	0	1
5	0	1	0	1	0	1	1	0	0	1	1	0
6	0	1	1	0	0	1	1	1	0	1	1	1
7	0	1	1	1	1	0	0	0	1	1	0	0
8	1	0	0	0	1	0	0	1	1	0	0	1
9	1	0	0	1	1	0	1	0	1	0	1	0
10	1	0	1	0	1	0	1	1	1	0	1	1
11	1	0	1	1	1	1	0	0	1	1	0	0
12	1	1	0	0	1	1	0	1	1	1	0	1
13	1	1	0	1	1	1	1	0	1	1	1	0
14	1	1	1	0	1	1	1	1	1	1	1	1
15	1	1	1	1	0	0	0	0	0	0	0	0

K-map For FF Inputs.

K-map D_3 :-



$$D_3 = Q_3\bar{Q}_2 + Q_3\bar{Q}_1 + Q_3\bar{Q}_0 + \bar{Q}_3Q_2Q_1Q_0$$
$$= Q_3(\bar{Q}_2 + \bar{Q}_1 + \bar{Q}_0) + \bar{Q}_3(Q_2Q_1Q_0)$$
$$= Q_3(Q_2Q_1Q_0)' + Q_3'(Q_2Q_1Q_0)$$

$$\boxed{D_3 = Q_3 \oplus (Q_2Q_1Q_0)}$$

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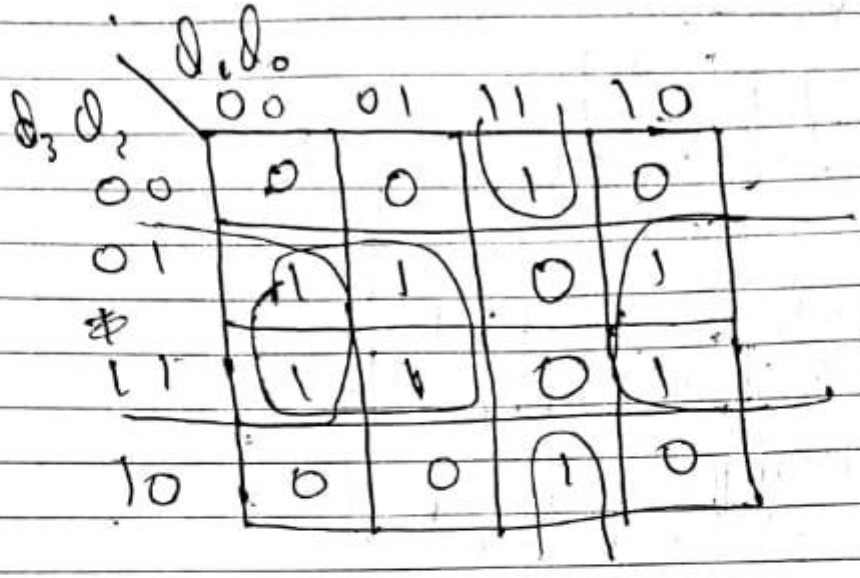
Kmap - D_2



$$D_2 = Q_2\bar{Q}_1 + Q_2\bar{Q}_0 + \bar{Q}_2Q_1Q_0$$
$$= Q_2(\bar{Q}_1 + \bar{Q}_0) + \bar{Q}_2(Q_1Q_0)$$
$$= Q_2\overline{(Q_1Q_0)} + \bar{Q}_2(Q_1Q_0)$$

$$\boxed{D_2 = Q_2 \oplus (Q_1Q_0)}$$

Карта – D_1

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$$D_1 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0$$

$$\boxed{D_1 = Q_1 \oplus Q_0}$$

Карта – D_0

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

$$\boxed{D_0 = \bar{Q}_0}$$

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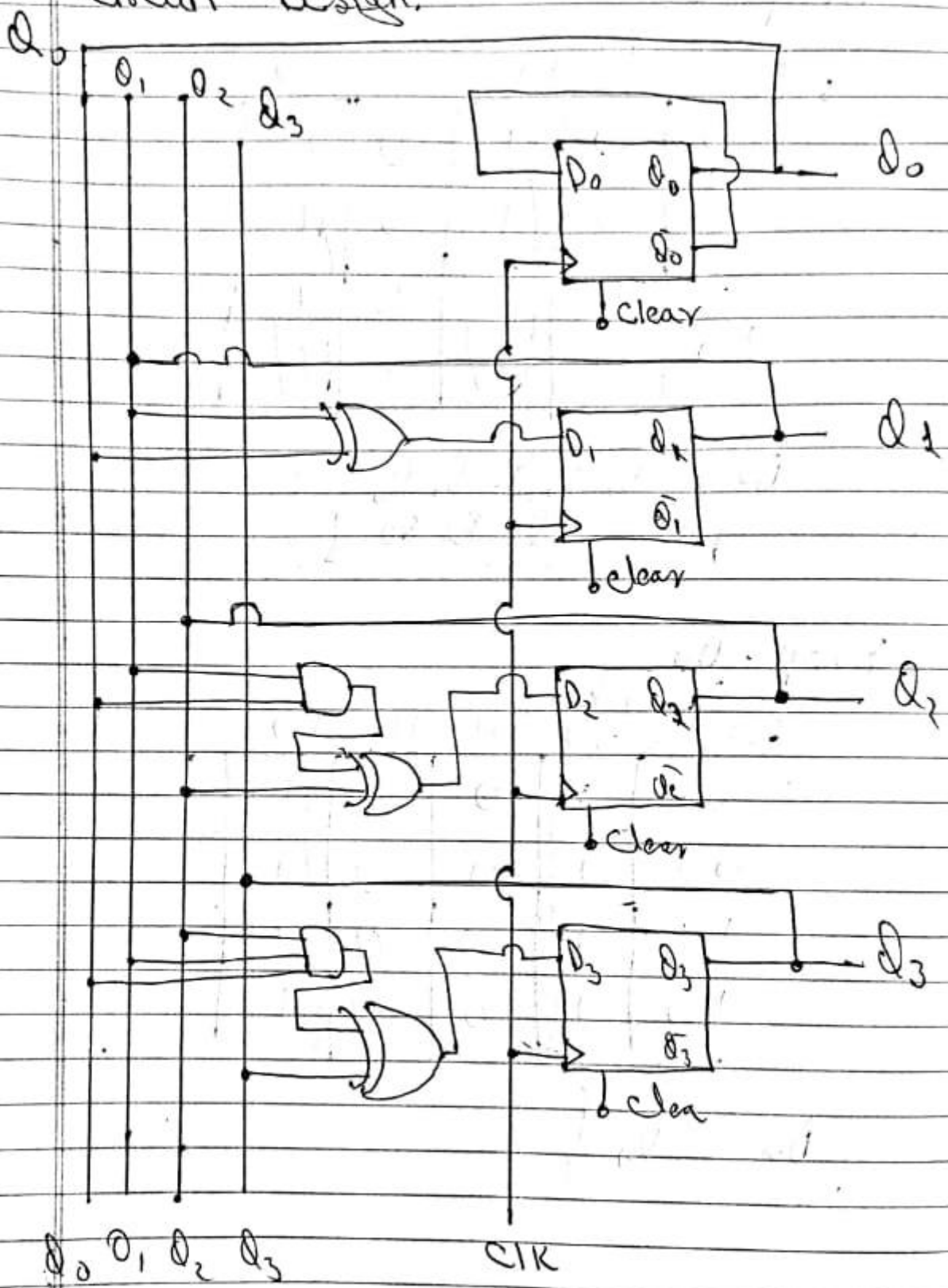
Circuit Design.



Verilog Code

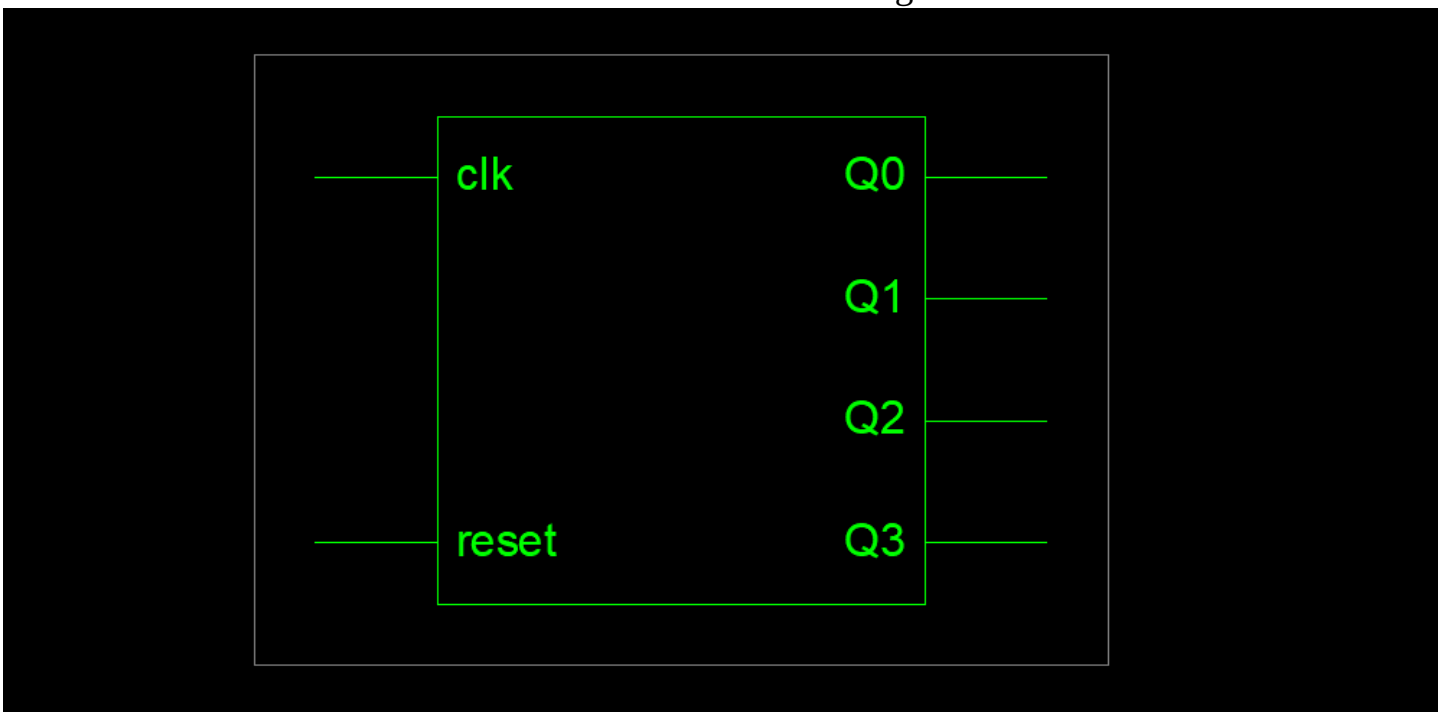
```
1  `timescale 1ns / 1ps
2  module D_Flip_Flop(Q, Q_bar, D, clk, reset);
3  input clk, reset, D;
4  output reg Q;
5  output Q_bar;
6  assign Q_bar = ~Q;
7  always @(posedge clk)
8  begin
9  if(reset)
10    Q<=1'b0;
11 else
12    Q<=D;
13 end
14 endmodule
15 // 4 bit up Counter
16 module UP_Counter_4_bit(clk,reset, Q0, Q1, Q2, Q3);
17 input clk, reset;
18 output Q0, Q1, Q2, Q3;
19 wire Q0_b, Q1_b, Q2_b, Q3_b;
20
21 wire d1, d2, d3, w1, w2;
22
23 xor x1(d1, Q0, Q1);
24 and(w1, Q0, Q1);
25 xor x2(d2,Q2, w1);
26 and(w2, Q0, Q1, Q2);
27 xor x3(d3,Q3, w2);
28
29
30 D_Flip_Flop D1(Q0, Q0_bar, Q0_bar, clk, reset);
31 D_Flip_Flop D2(Q1, Q1_bar, d1, clk, reset);
```

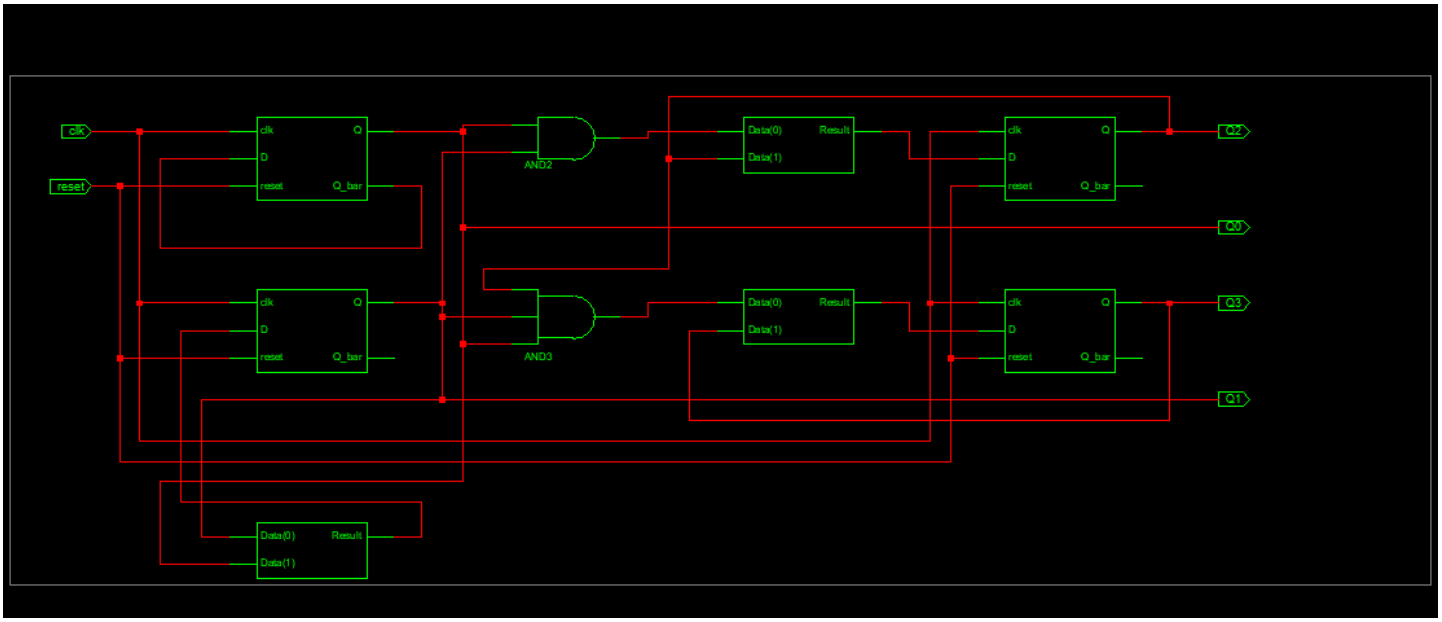
```
12    Q<=D;
13 end
14 endmodule
15 // 4 bit up Counter
16 module UP_Counter_4_bit(clk,reset, Q0, Q1, Q2, Q3);
17 input clk, reset;
18 output Q0, Q1, Q2, Q3;
19 wire Q0_b, Q1_b, Q2_b, Q3_b;
20
21 wire d1, d2, d3, w1, w2;
22
23 xor x1(d1, Q0, Q1);
24 and(w1, Q0, Q1);
25 xor x2(d2,Q2, w1);
26 and(w2, Q0, Q1, Q2);
27 xor x3(d3,Q3, w2);
28
29
30 D_Flip_Flop D1(Q0, Q0_bar, Q0_bar, clk, reset);
31 D_Flip_Flop D2(Q1, Q1_bar, d1, clk, reset);
32 D_Flip_Flop D3(Q2, Q2_bar, d2, clk, reset);
33 D_Flip_Flop D4(Q3, Q3_bar, d3, clk, reset);
34
35 //D_Flip_Flop D1(Q0, Q0_bar, Q0_bar, clk, reset);
36 //D_Flip_Flop D2(Q1, Q1_bar, (Q0^Q1), clk, reset);
37 //D_Flip_Flop D3(Q2, Q2_bar, (Q2^(Q1&Q0)), clk, reset);
38 //D_Flip_Flop D4(Q3, Q3_bar, Q3^(Q0&Q1&Q2), clk, reset);
39
40 endmodule
41
```

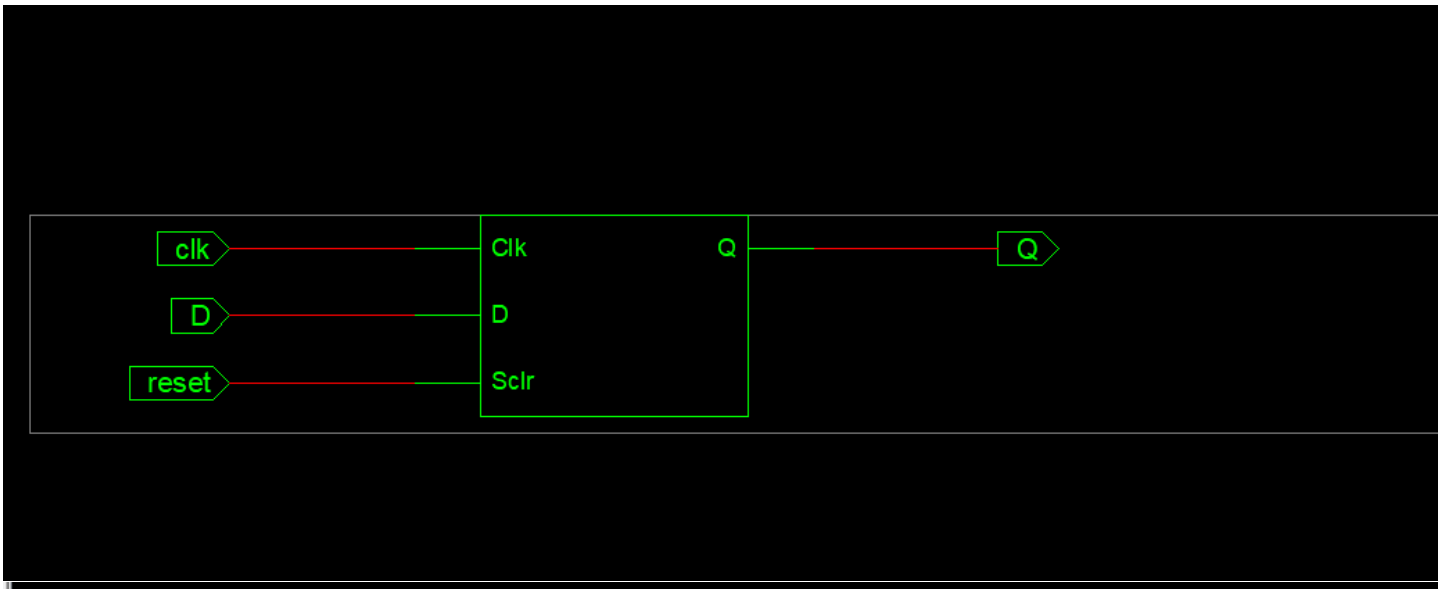
Test Bench For Verilog Code

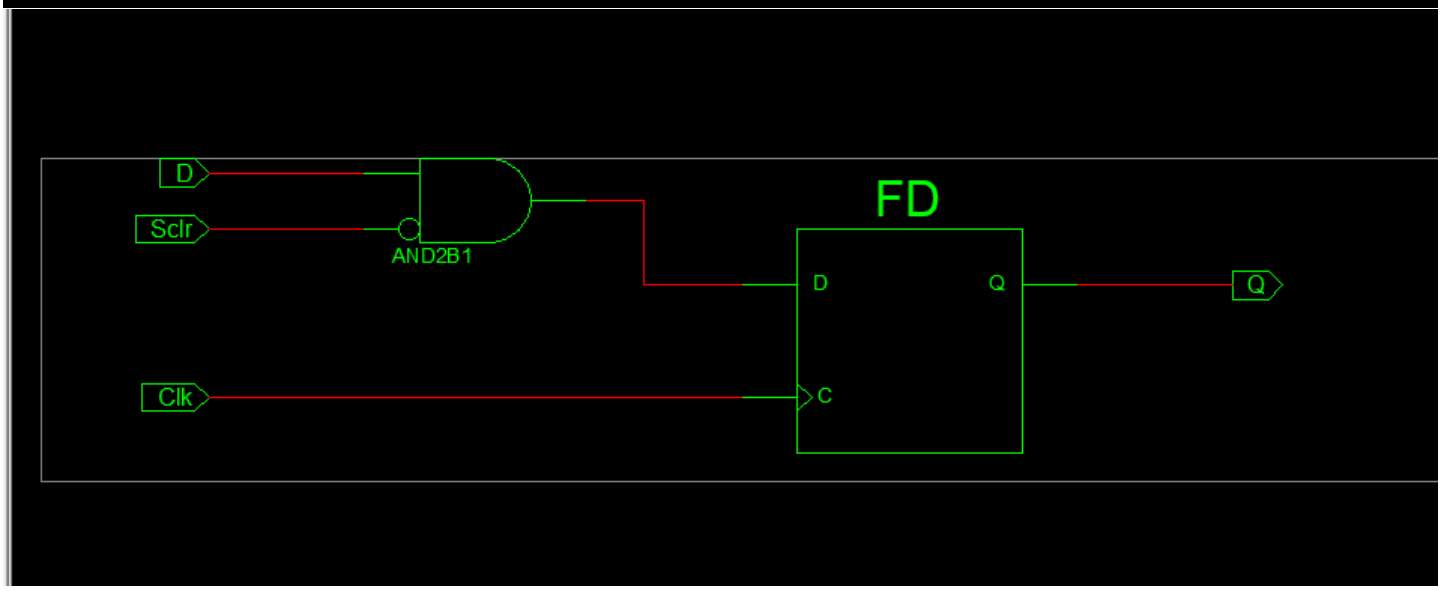
```
1  `timescale 1ns / 1ps
2  module Clock_v;
3     reg clk, reset;
4     wire Q0, Q1, Q2, Q3;
5     // Instantiate the Unit Under Test (UUT)
6     UP_Counter_4_bit uut (
7        .clk(clk),
8        .reset(reset),
9        .Q0(Q0),
10       .Q1(Q1),
11       .Q2(Q2),
12       .Q3(Q3)
13    );
14
15    initial begin
16       clk = 0;
17       forever #1 clk = ~clk;
18       end
19       initial begin
20       reset = 1;
21       #5 reset = 1'b0;
22       end
23
24 endmodule
25
26
```

Schematic Diagram

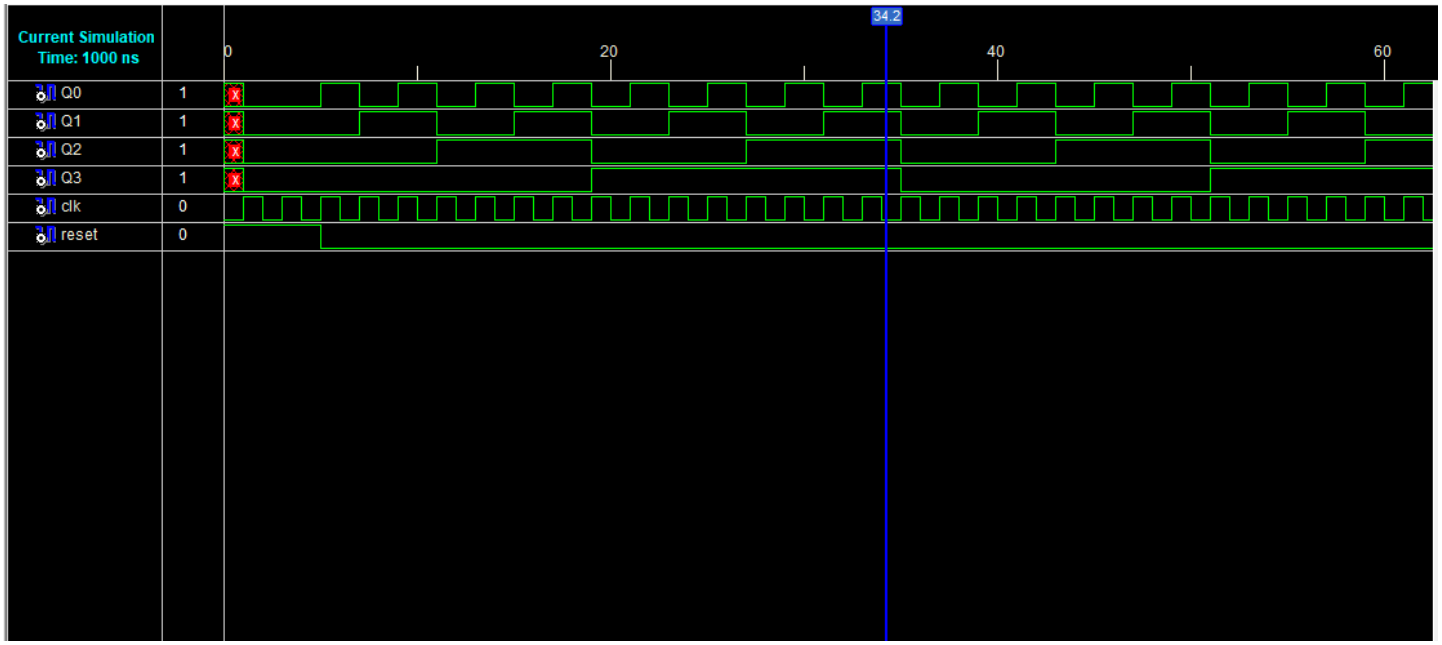








Wave Form (Output Counter)


Current Simulation Time: 1000 ns
34.2
0
20
40
60
Q0
1
Q1
1
Q2
1
Q3
1
clk
0
reset
0

END