**Assignment Submission Sheet**

|  |  |  |
| --- | --- | --- |
| **Term: 321221** | **Submission Date: 28-09-2021** |  |
| **Lecture Date: 15-09-2021** | **Assignment Number: 02** |
| **Course Code: ECE290** | **Section: E1901** | **Group: A** |
| **Registration Number: 11904463** | **Student Name: Mohit Rawat** | **Roll No: 09** |

### Concept Learned

### I have learned how to make half adder and full adder using verilog and how to make 3-bit ripple carry adder that addes 3 bit number and make wave form of input and output signal.

1. **Key Observations &Insights**

My key observation was how ripple carry adder addes two number and gives result and how our test bench make output form of output given by 3-bit ripple carry adder.

1. **Application Areas**

The application of adder is in ALU of processor. This is unit of processor where all mathematical operation done and addition is basic process of ALU. It use addition to for subtraction, division and multiplication like operation.

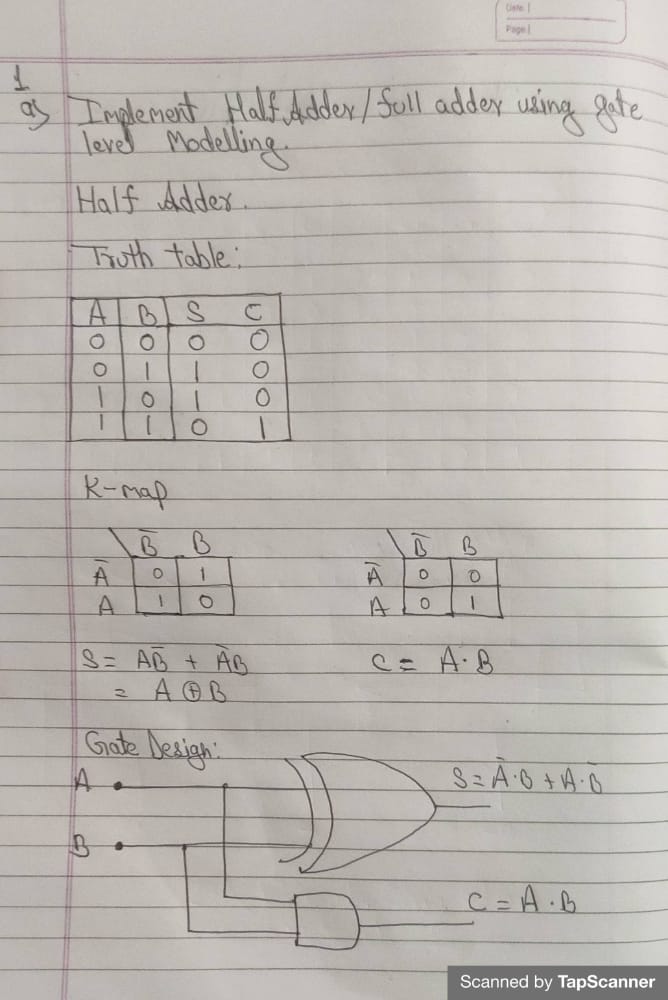
1. **A)**

**Half Adder/ Full Adder**

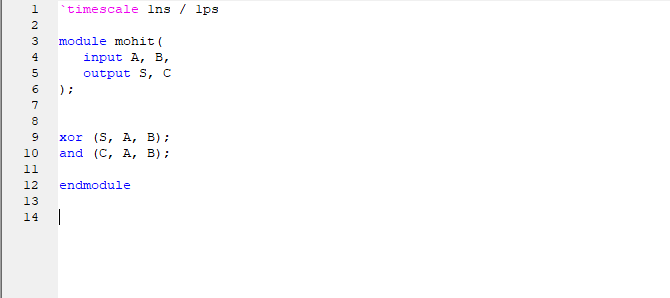
**B)**

**3-bit ripple carry adder using half adder / full adder.**

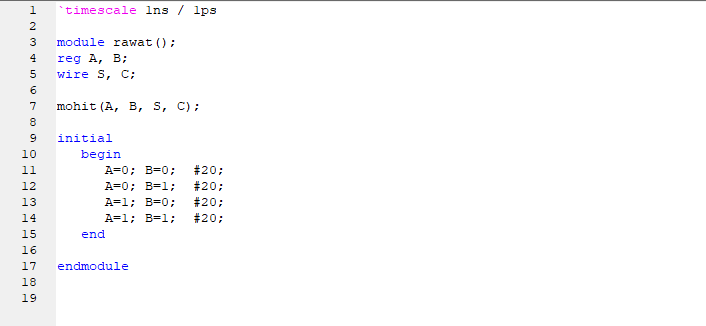
**Half - Adder**



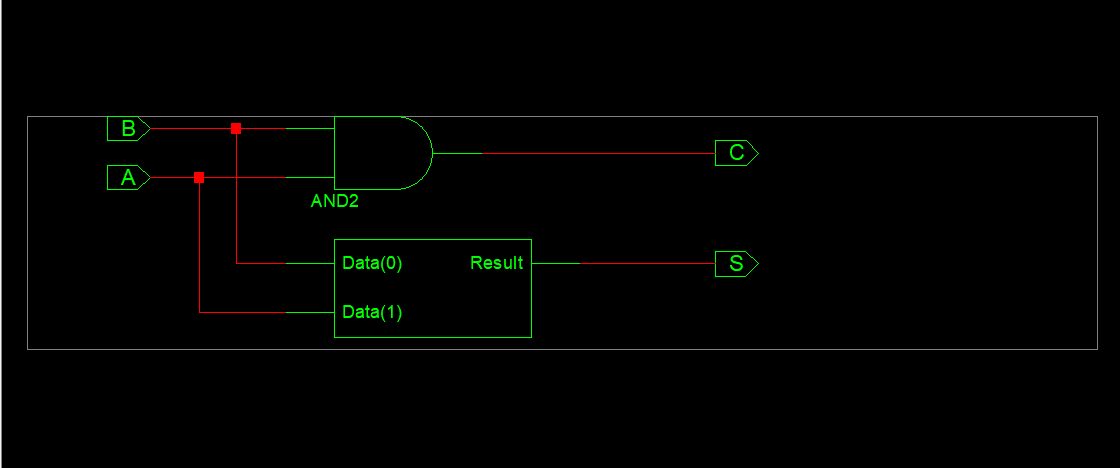
**Verilog Code**

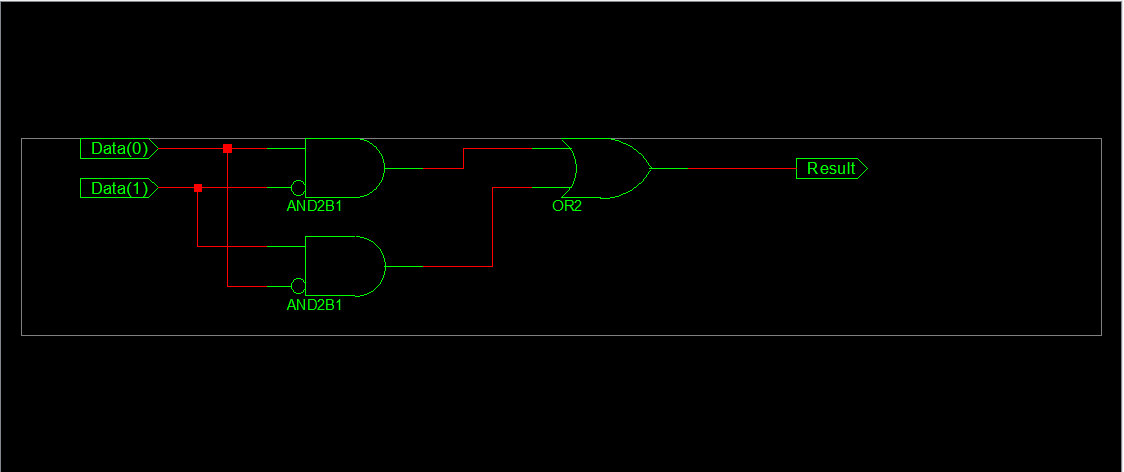
****

**Test bench code**

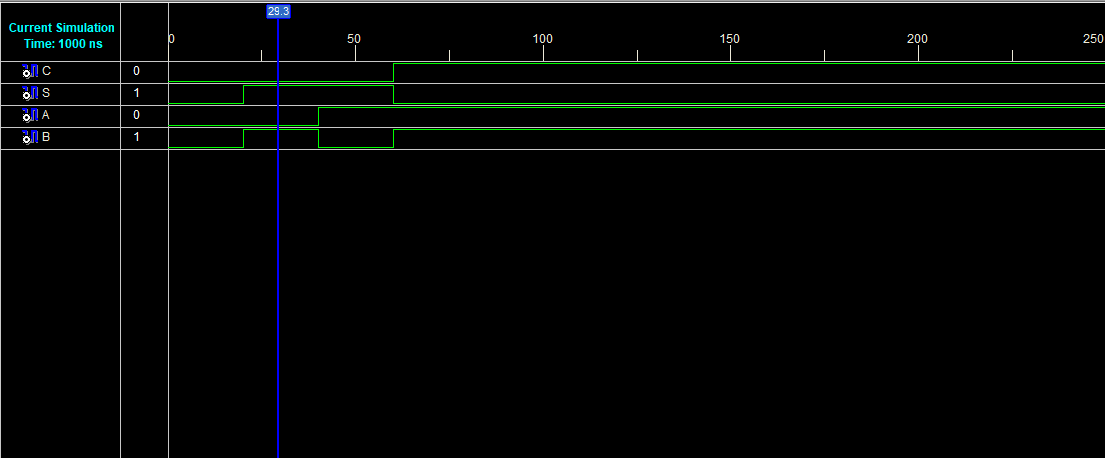
****

**Circuit design**

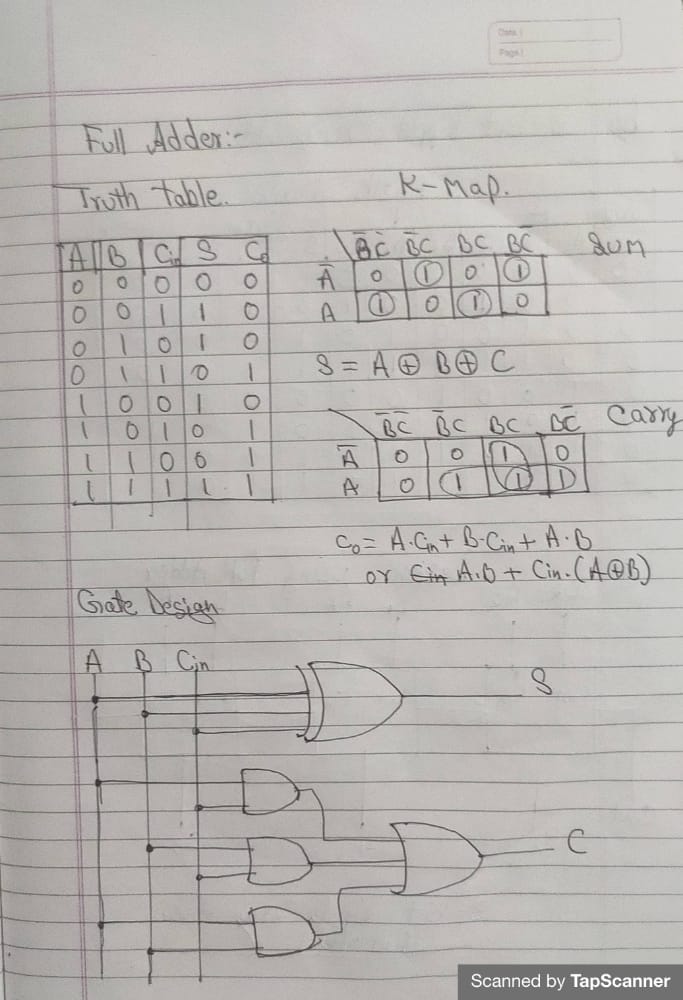
****

****

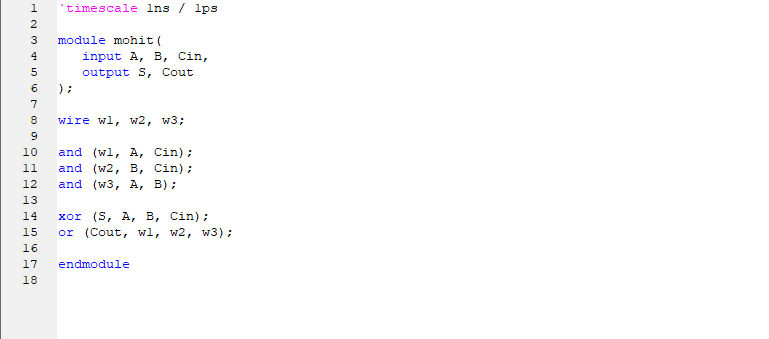
**Wave form**

****

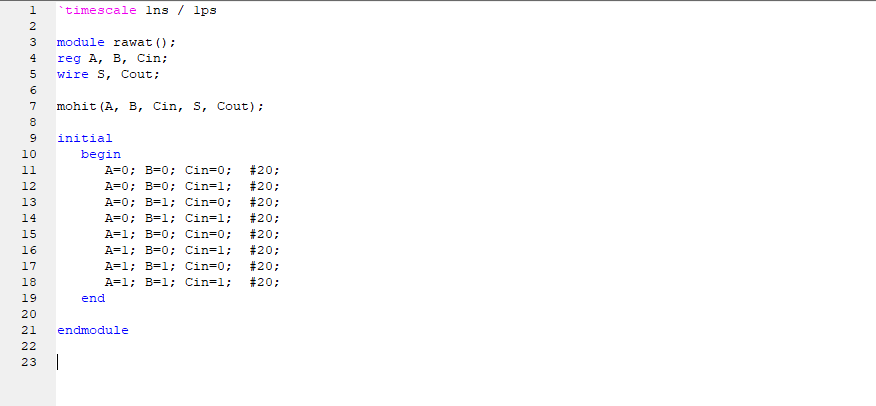
**Full adder**

****

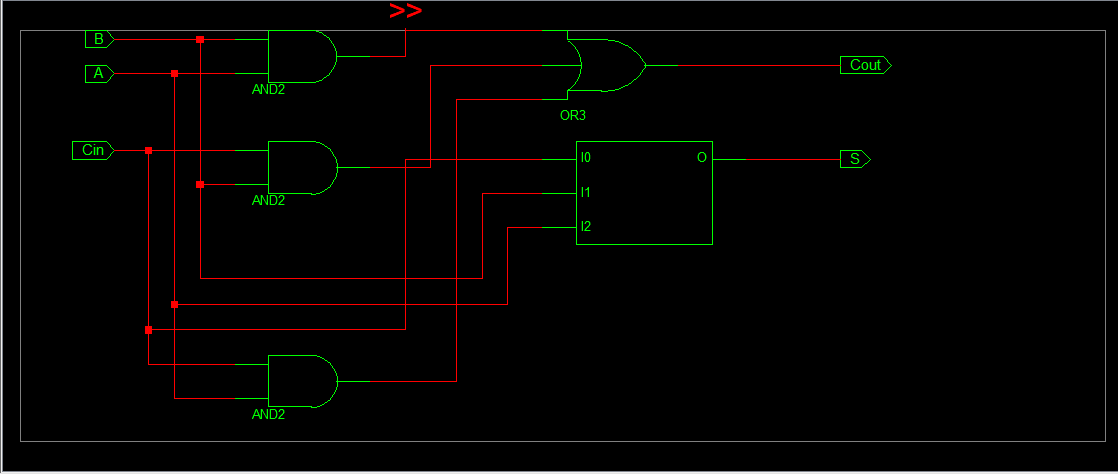
**Verilog Code**

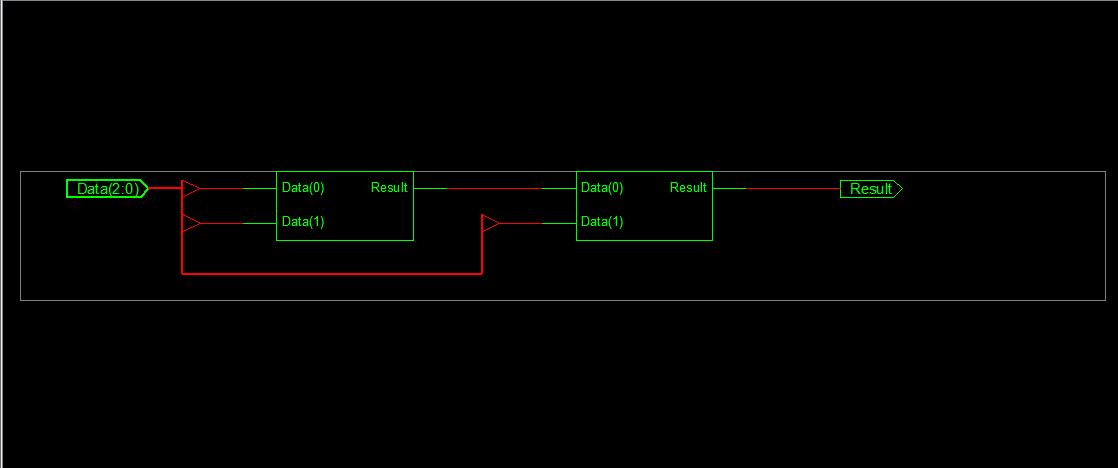
****

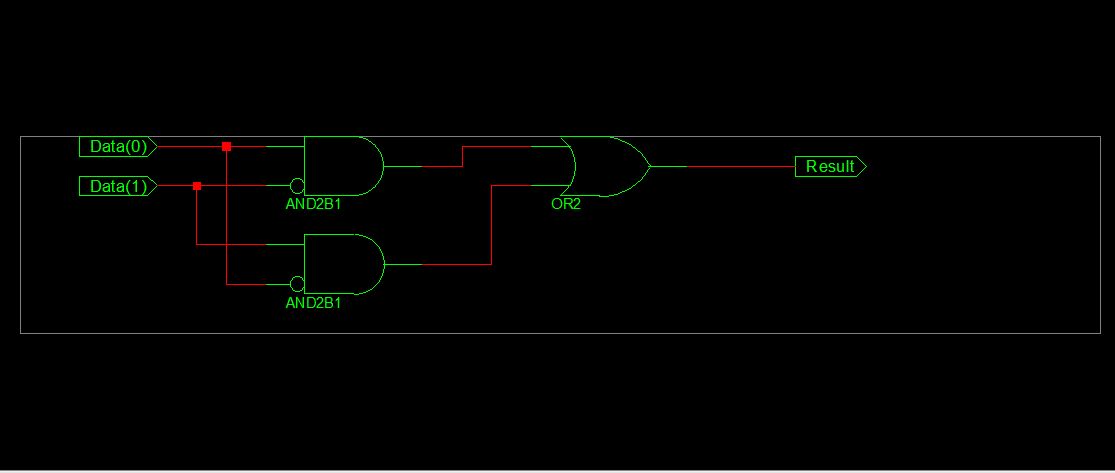
**Test bench code**

****

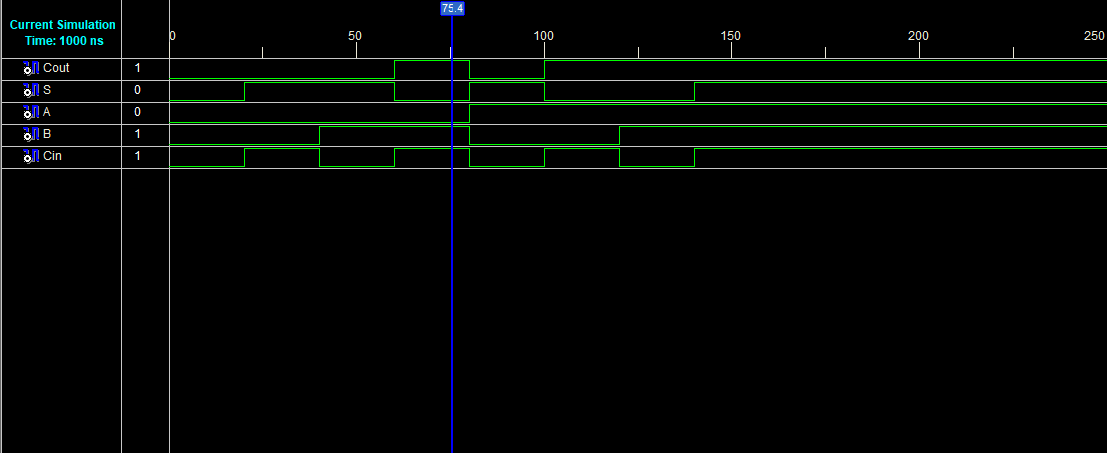
**Circuit**

****

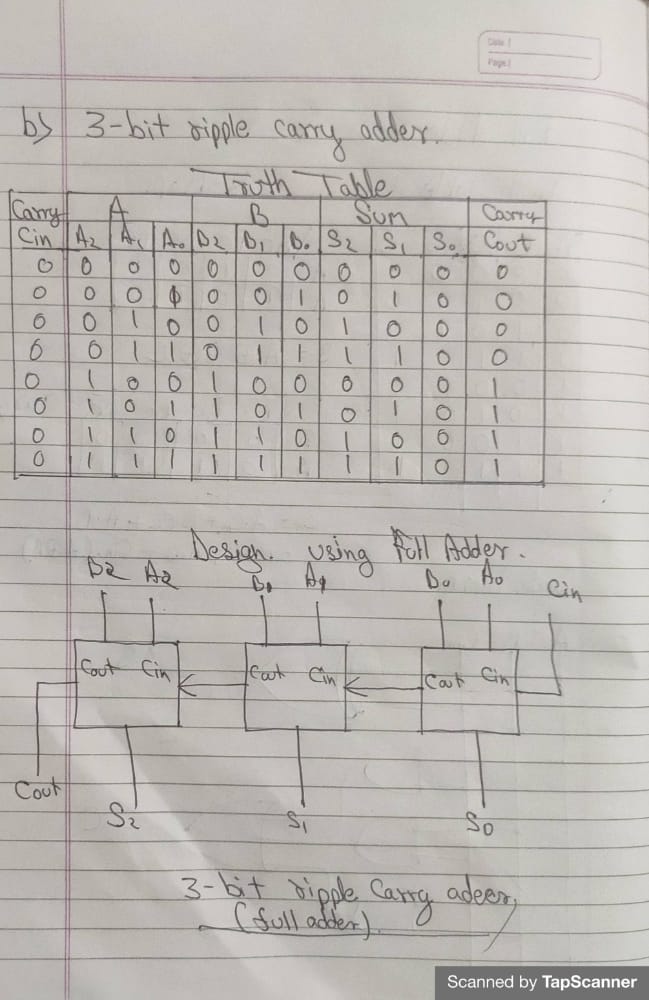
****

****

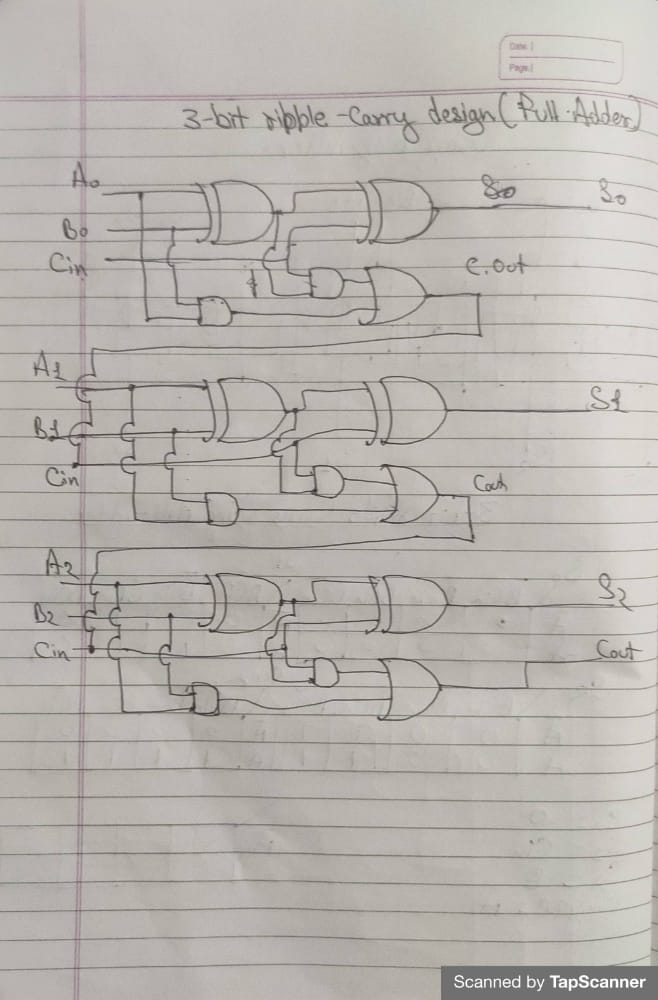
**Waveform**

****

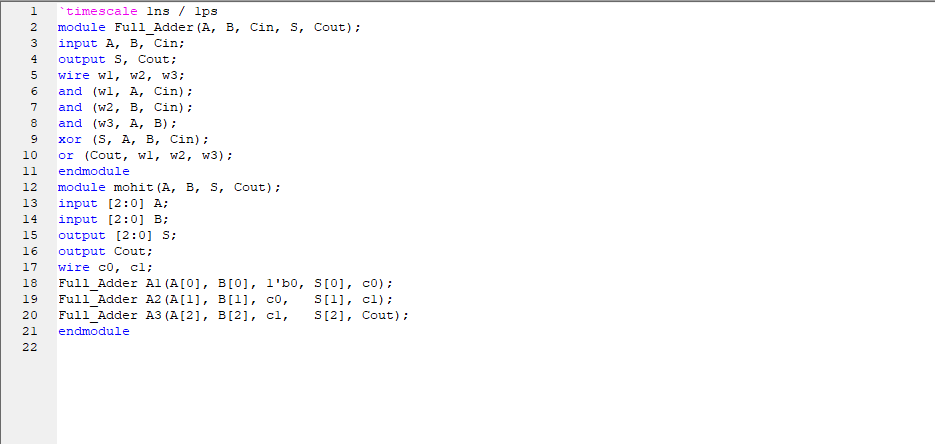
**3-bit Ripple carry Adder (using Full Adder)**

****

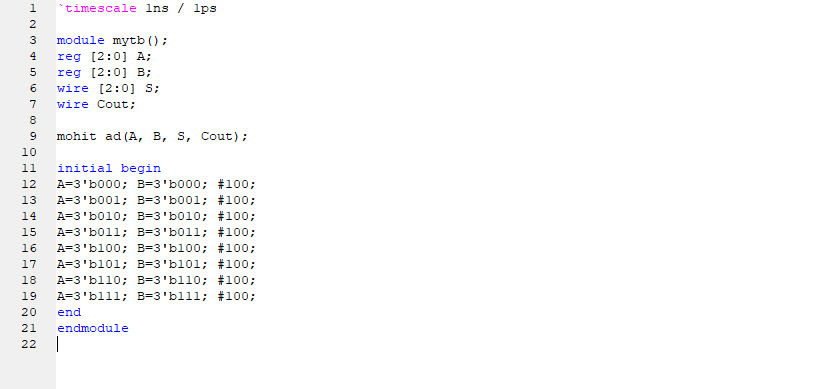
**Circuit**

****

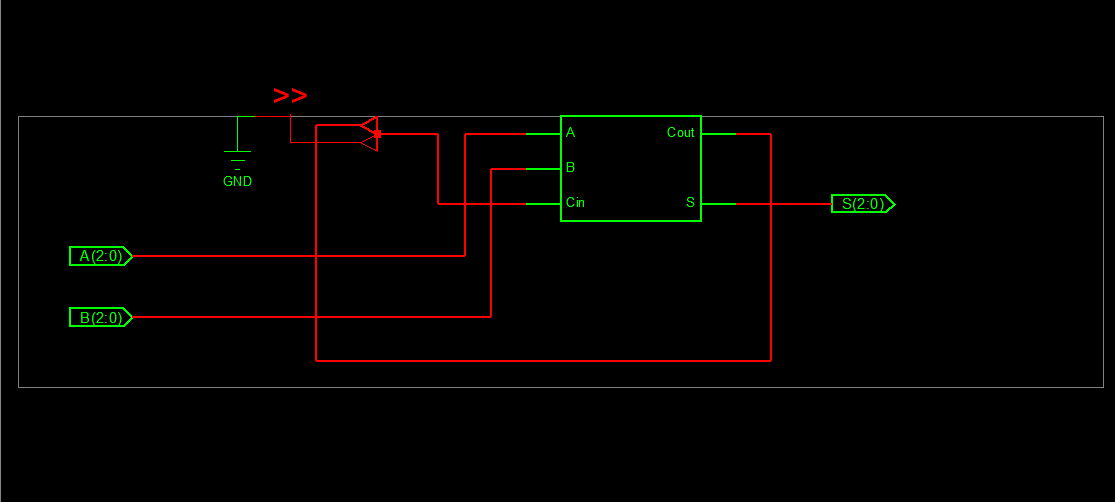
**Verilog Code**

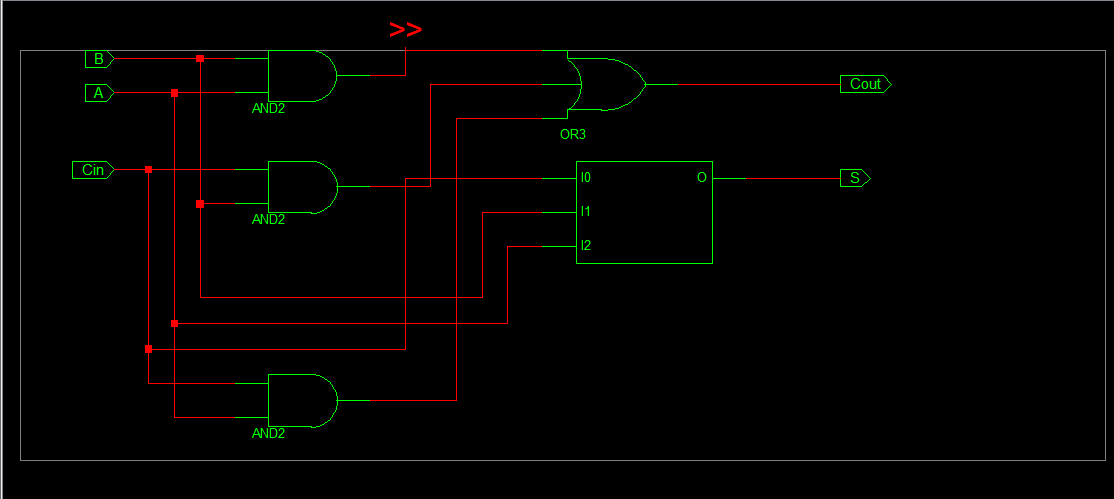
****

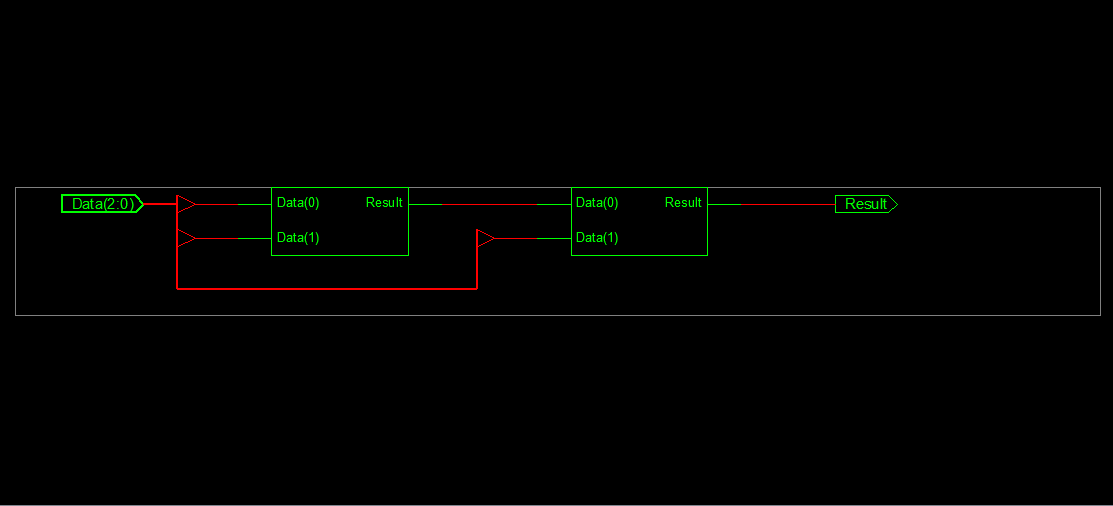
**Test bench Program**

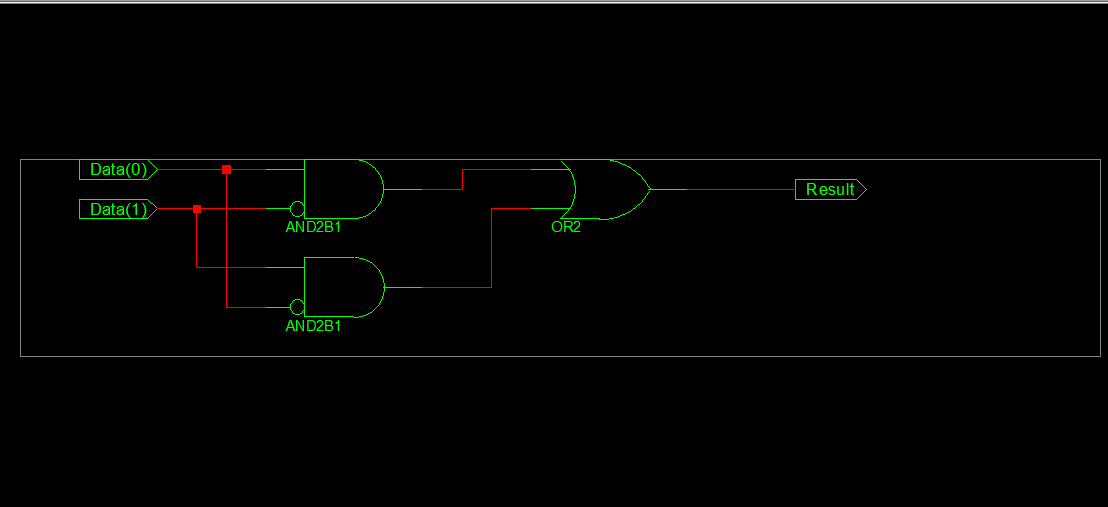


**Circuit Diagram**

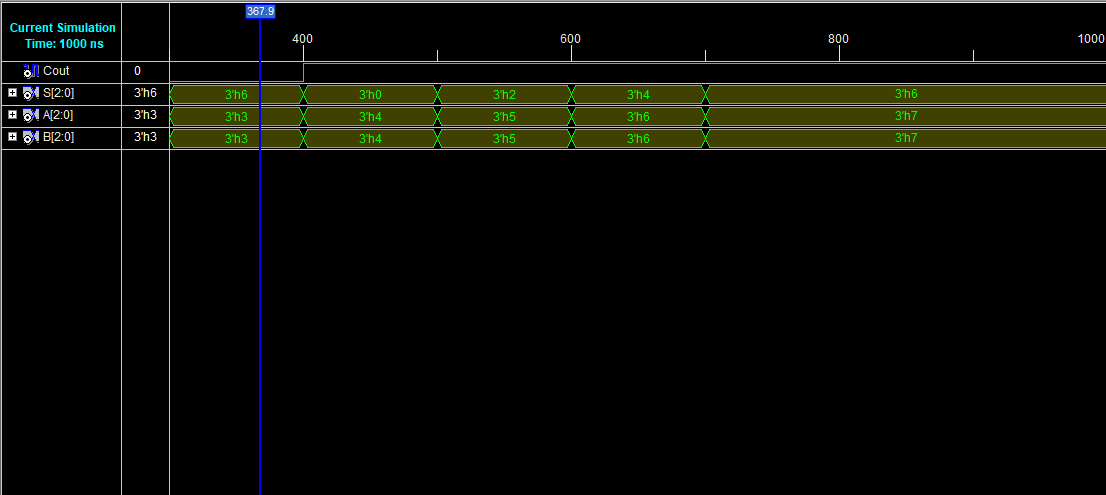




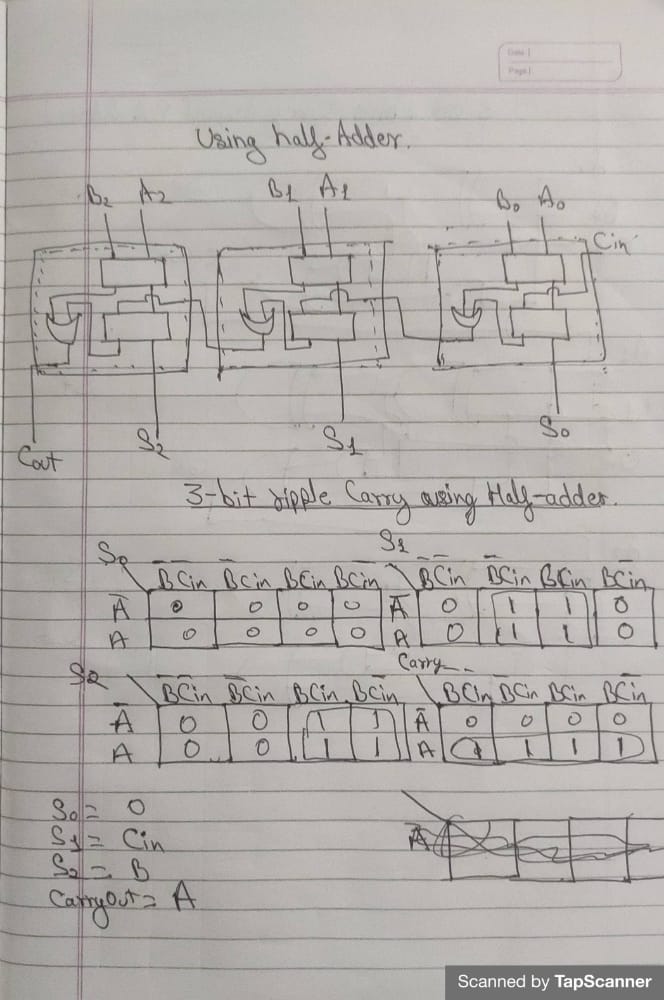




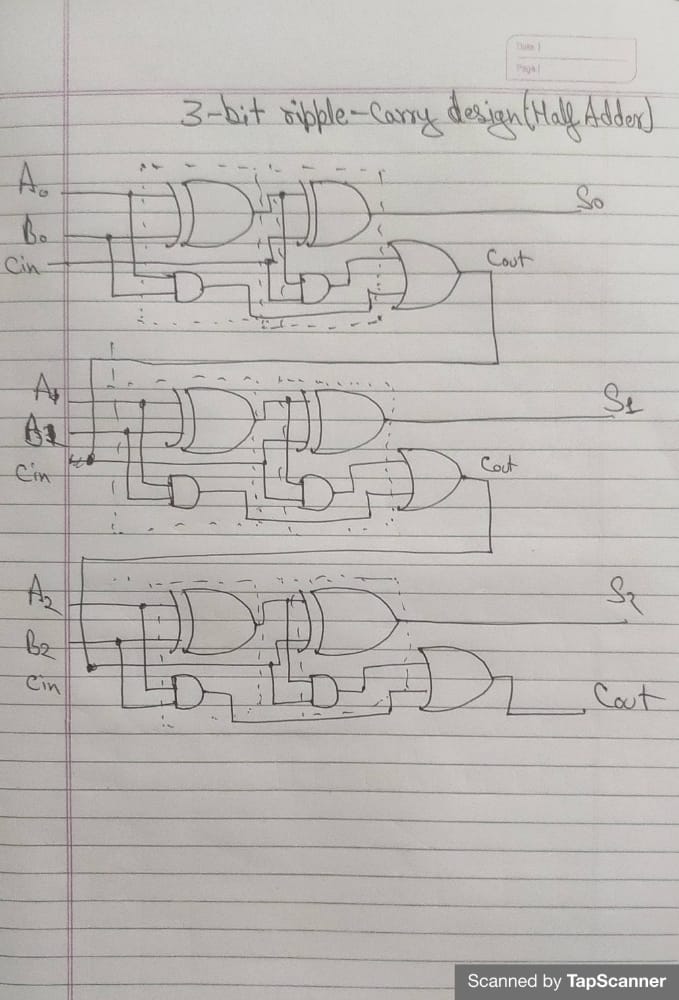
**Waveform**

****

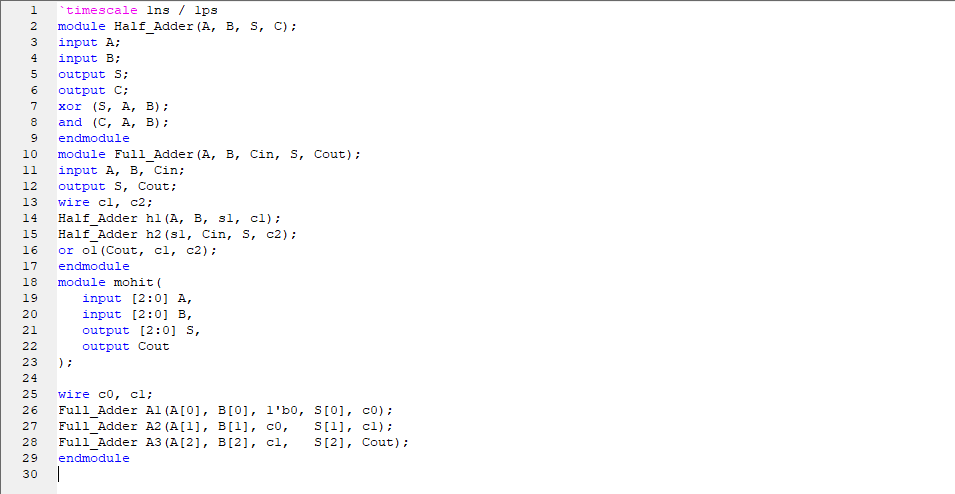
**3-bit Ripple Carry Adder(Using Half Adder)**

****

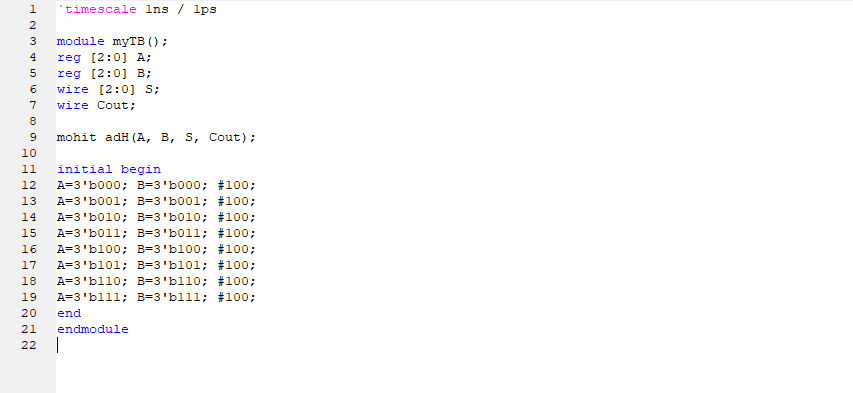
**Circuit Diagram**

****

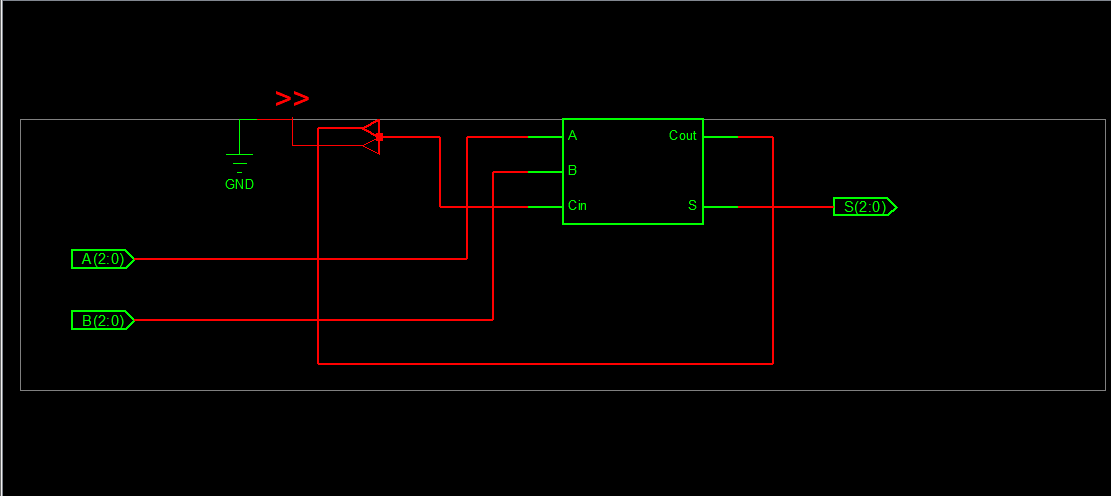
**Verilog code**

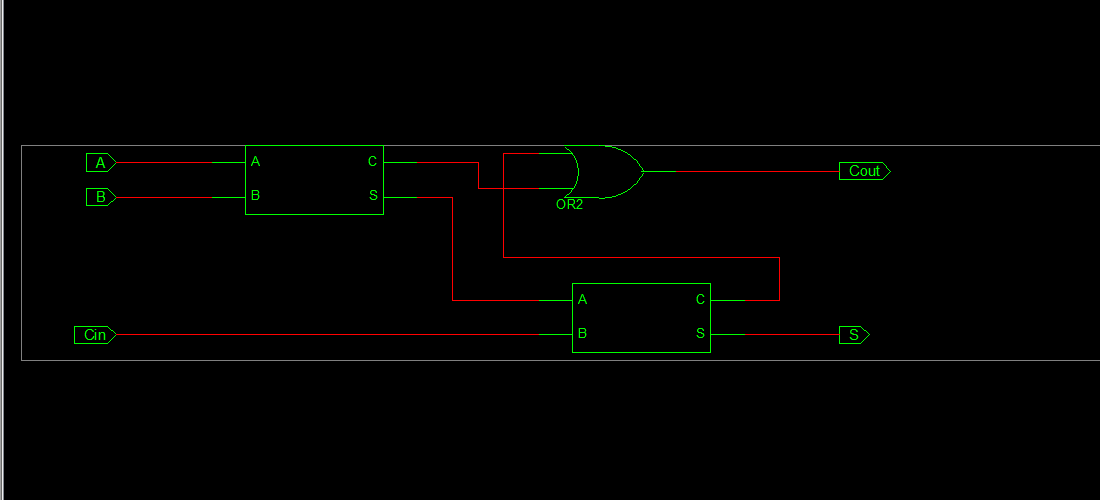


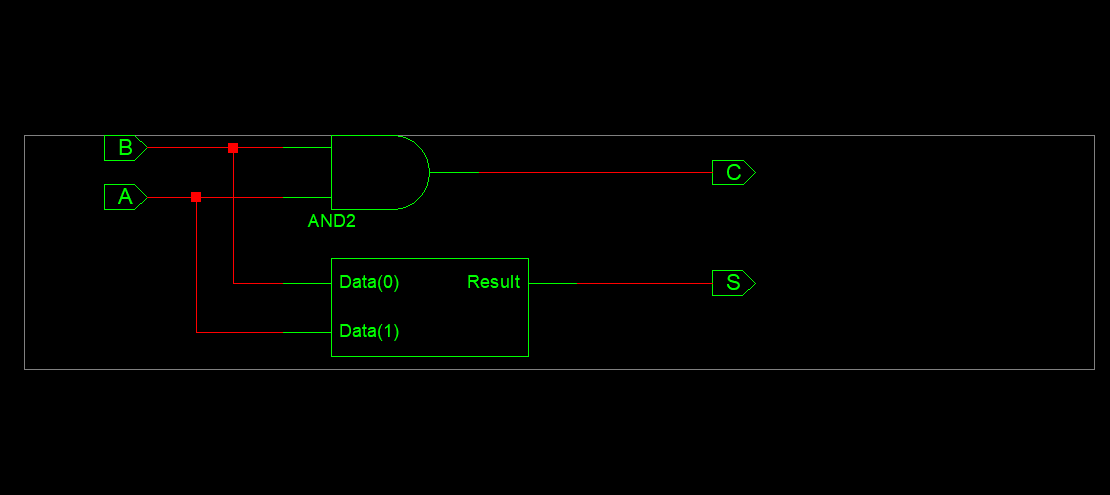
**Test bench code**

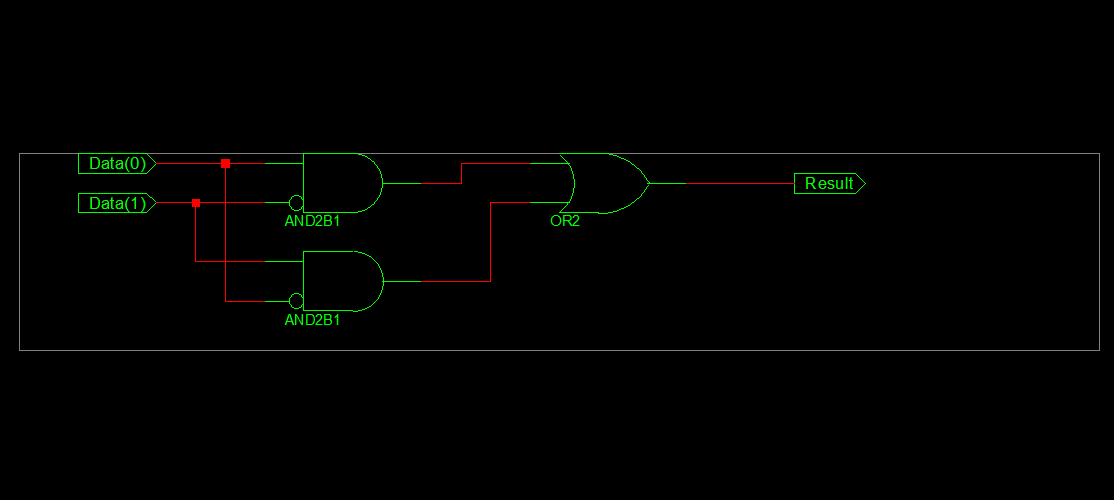


**Circuit Diagram**

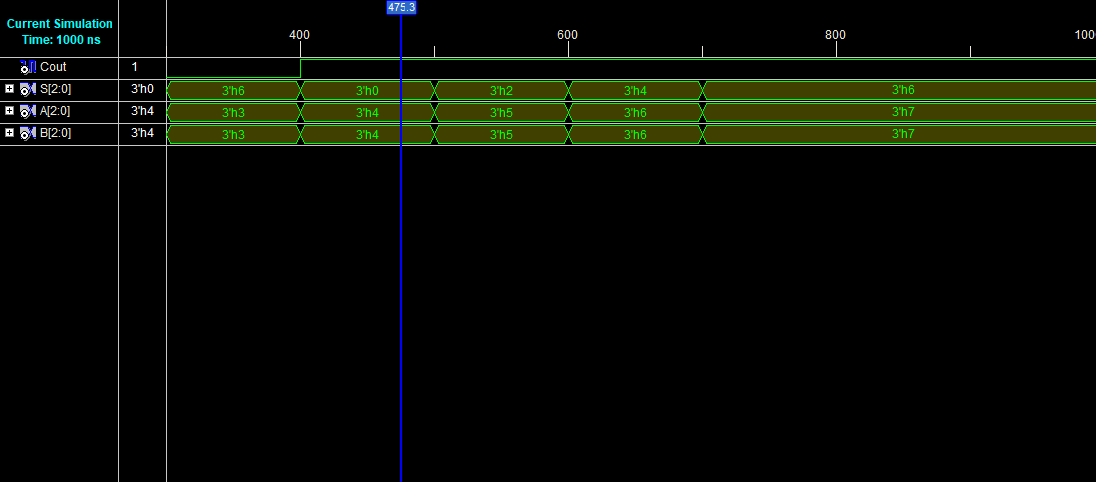








**Waveform**



**END**