CA-2

LOVELY PROFESSIONAL UNIVERSITY
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ECE 390: **WORKSHOP ON ANALOG DESIGN USING CADENCE VIRTUOSO**

Name: _____

Section:_____ Roll No:_____ Registration No: _____

Max Marks: 30

Q1. Design a 4-bit adder using tanner tool using created symbol of full adder circuit. Verify the operation using spice simulation for A=1010 and B=0111. (5)

Q2. Implement 2x1 Mux using transmission gate technology and simulate on tanner tool. Attach the screenshots of S-edit, T-spice and W-Edit of the same. (5)

Q3. Design ALU capable to perform addition, subtraction, multiplication and division operations on two 2-bit numbers in S-edit, simulate for transient analysis in T-spice. Indicate each operation separately in the wave-form using vertical bars. (5)

Q4. Implement 4-bit LFSR circuit with characteristic equation $1+ x + x^4$ in S-edit using D-flip-flops and Ex-OR gate. Simulate the same and identify number of non-identical patterns generated in the waveform. (5)

Q5. Design 1-bit 6T-SRAM cell in S-edit. Choose the timings wisely to show storage of logic 0 and logic 1 in the waveform. Also verify the Read/Write operation using vertical bars (5)

Q6. Design 4X4 ROM using NMOS and perform the read operation using 2x4 address decoder. Verify the functionality after storing data “1000”, “0100”, “0010”, “0001”. (5)