Set3

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ECE 390: **WORKSHOP ON ANALOG DESIGN USING CADENCE VIRTUOSO**

Name: _____

Section:_____ Roll No:_____ Registration No: _____

Max Marks: 30

Q1. Design a CMOS inverter using tanner tool and create a symbol named NOT gate of the same.

(5)

Q2. Implement NAND gate using CMOS technology and simulate on tanner tool using level 1 model file. Attach the screenshots of S-edit, T-spice and W-Edit of the same.

(5)

Q3. Design CMOS inverter in S-edit, simulate for transient analysis in T-spice. Calculate propagation delay using the generated waveform.

(5)

Q4. Implement Full-adder circuit in S-edit, simulate for transient analysis in T-spice. Choose the ON time and time period wisely to verify the truth table in the generated waveform.

(5)

Q5. Design J-K flip-flop in S-edit using instances of earlier designed NAND and Not gates as symbols, simulate for transient analysis in T-spice. Calculate propagation delay using the generated waveform.

(5)

Q6. Design 4 bit Shift register using D flip-flop in S-edit, simulate for transient analysis in T-spice. Verify the functionality by giving input pattern 1101 in serial fashion.

(5)