Set3

ECE 390: WORKSHOP ON ANALOG DESIGN USING CADENCE VIRTUOSO

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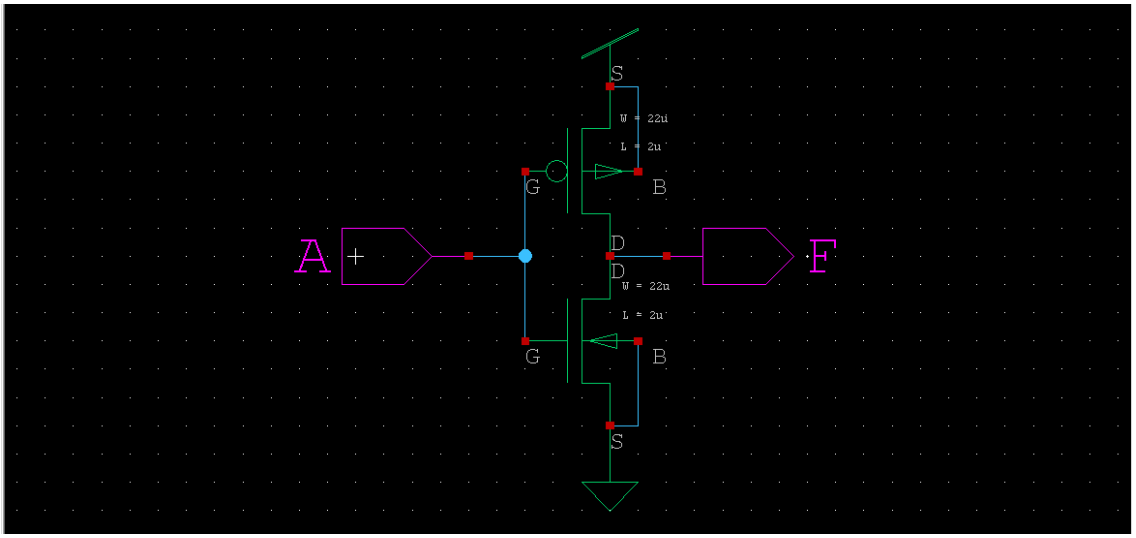
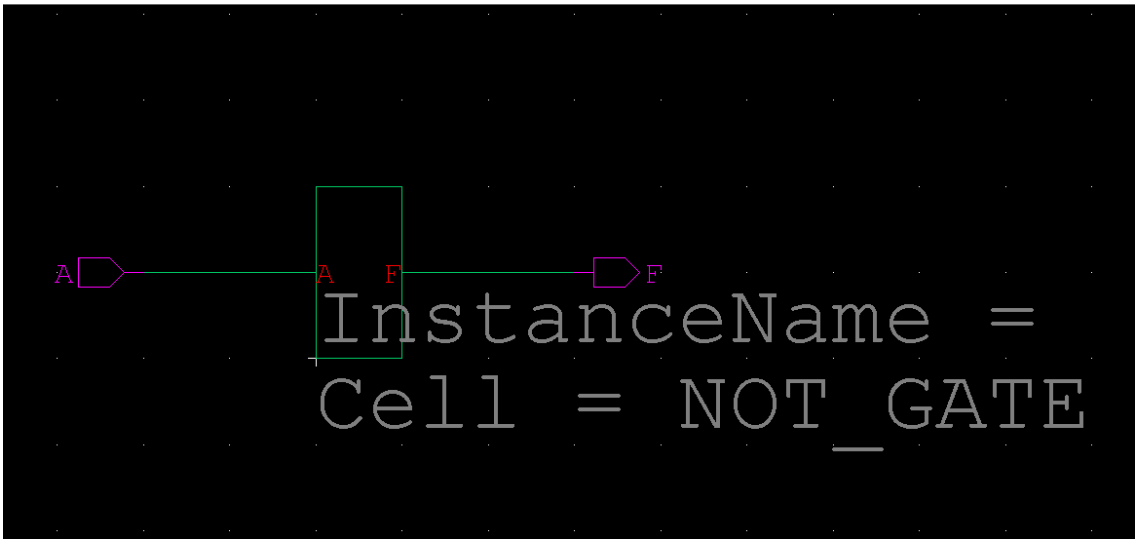
Section: E1901 Roll No: 09 Registration No: 11904463

Max Marks: 30

Q1. Design a CMOS inverter using tanner tool and create a symbol named NOT gate of the same.





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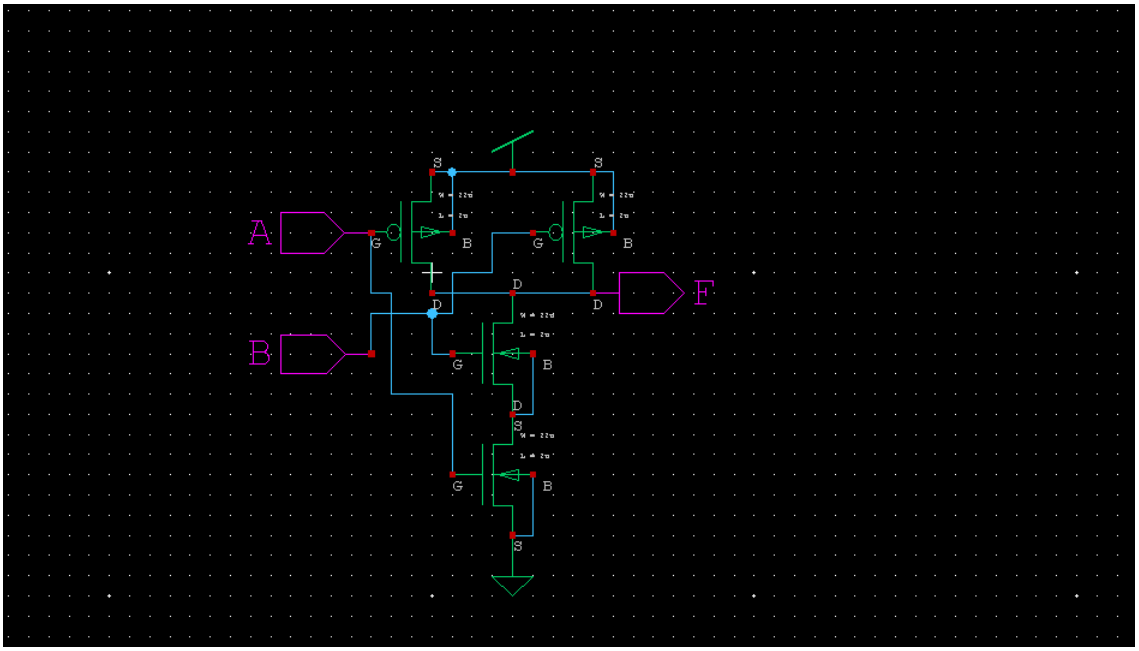
Q2. Implement NAND gate using CMOS technology and simulate on tanner tool using level 1 model file. Attach the screenshots of S-edit, T-spice and W-Edit of the same.



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********** Simulation Settings - Parameters and SPICE options **********

MMOSFET_N_1 F B N_1 N_1 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 N_1 A Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 F A Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_3 F B Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

********* Simulation Settings - Analysis section *********
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)

Vdd Vdd Gnd 3.3V
Vin1 A Gnd pulse(0 3.3v 40n 1n 1n 40n 40n)
Vin2 B Gnd pulse(0 3.3v 20n 1n 1n 20n 40n)
.Tran 1ns 80ns
.print V(A) V(B) V(F)
********* Simulation Settings - Additional SPICE commands *********
.end
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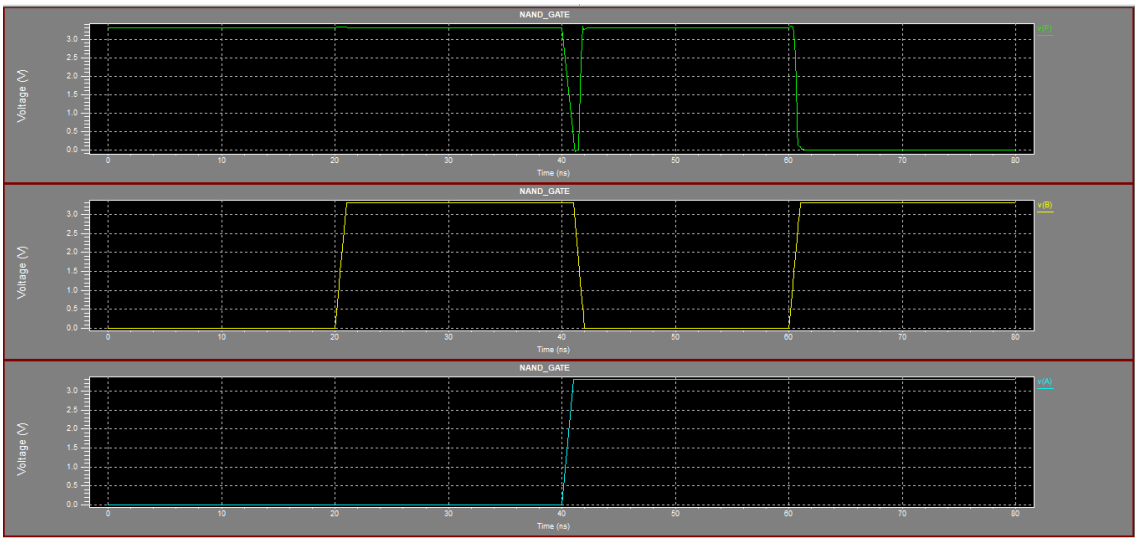

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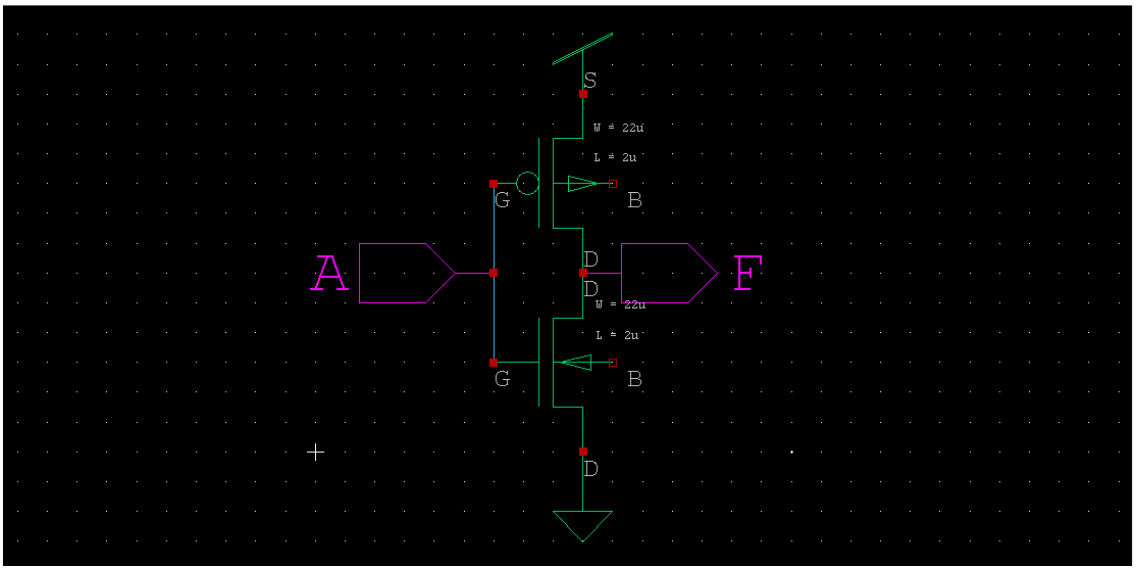
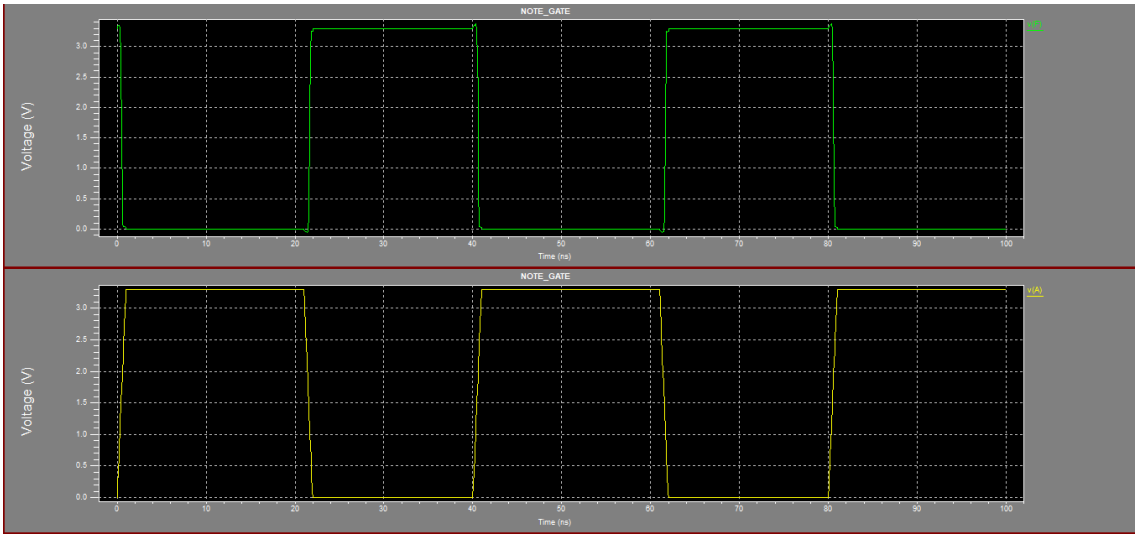
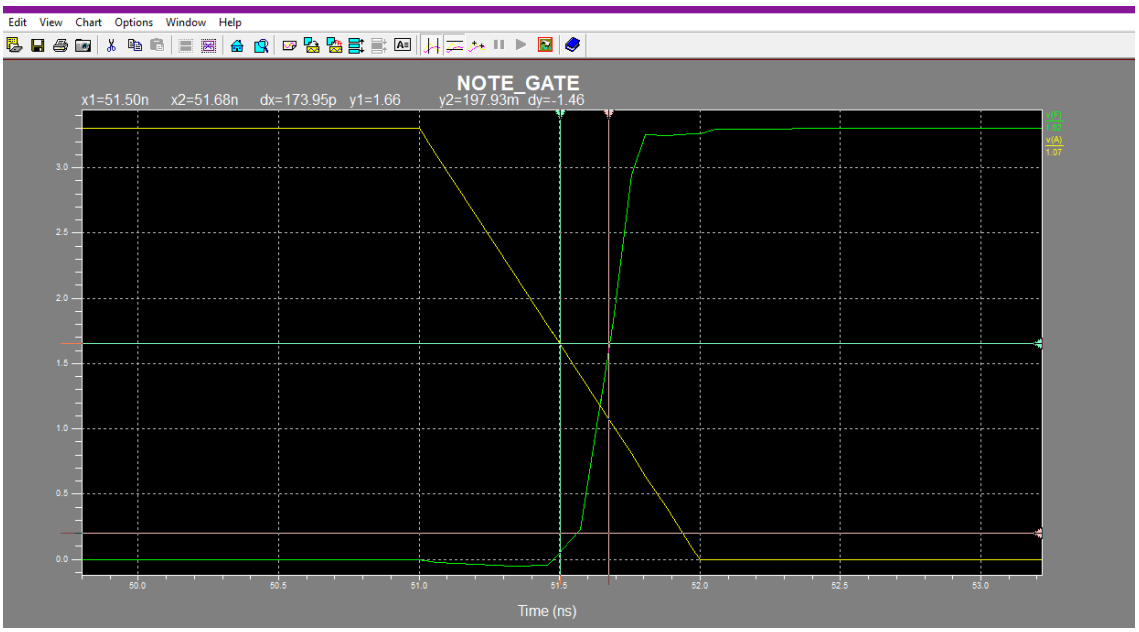
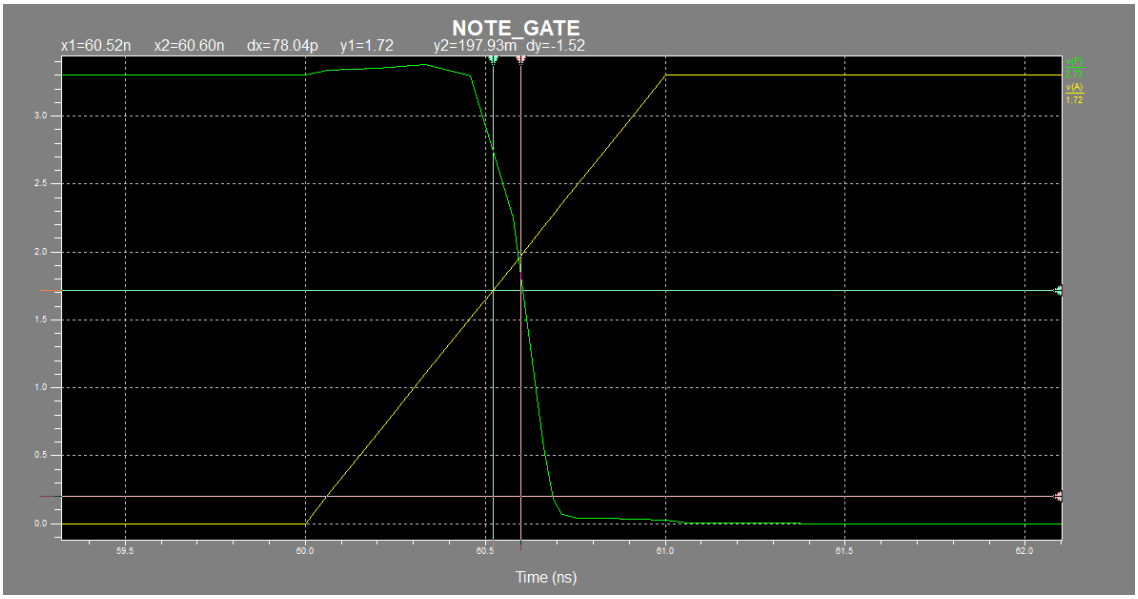
Q3. Design CMOS inverter in S-edit, simulate for transient analysis in T-spice. Calculate propagation delay using the generated waveform.




NOTE_GATE
Voltage (V)
Time (ns)
NOTE_GATE
Voltage (V)
Time (ns)


Edit View Chart Options Window Help
NOTE_GATE
x1=51.50n x2=51.68n dx=173.95p y1=1.66 y2=197.93m dy=-1.46
Time (ns)



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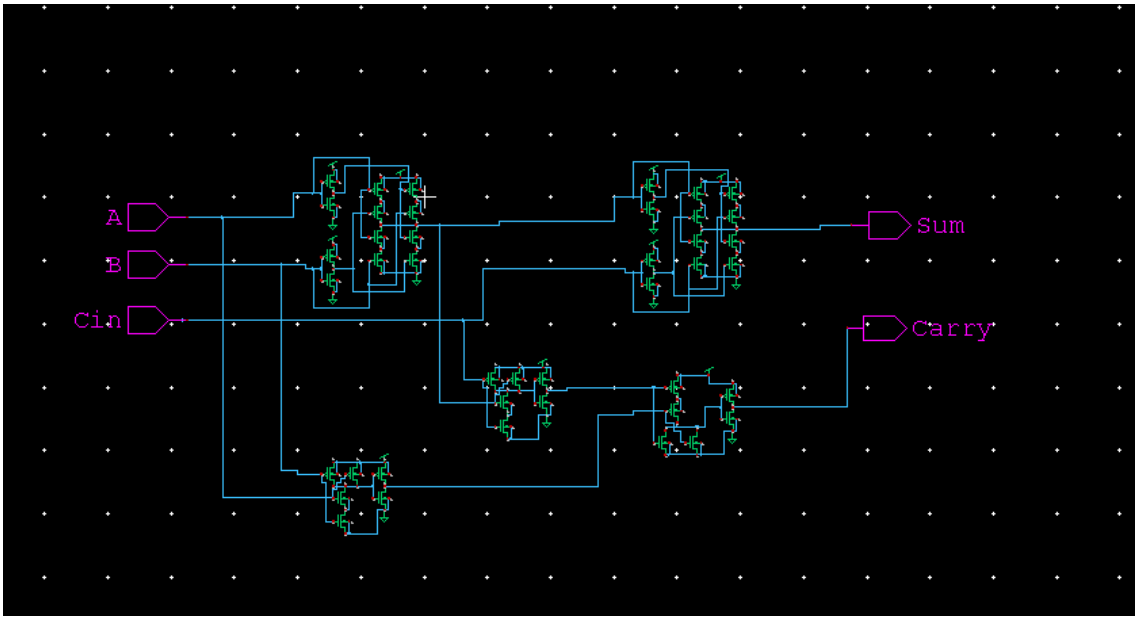
Q4. Implement Full-adder circuit in S-edit, simulate for transient analysis in T-spice. Choose the ON time and time period wisely to verify the truth table in the generated waveform.

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********* Simulation Settings - Analysis section *********
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)

Vdd Vdd Gnd 3.3V
Vin1 A Gnd pulse(0 3.3v 40n 1n 1n 40n 40n)
Vin2 B Gnd pulse(0 3.3v 20n 1n 1n 20n 40n)
Vin3 Cin Gnd pulse(0 3.3v 10n 1n 1n 10n 20n)
.Tran 1ns 80ns
.print V(A) V(B) V(Cin) V(Sum) V(Carry)
********* Simulation Settings - Additional SPICE commands *********

.end
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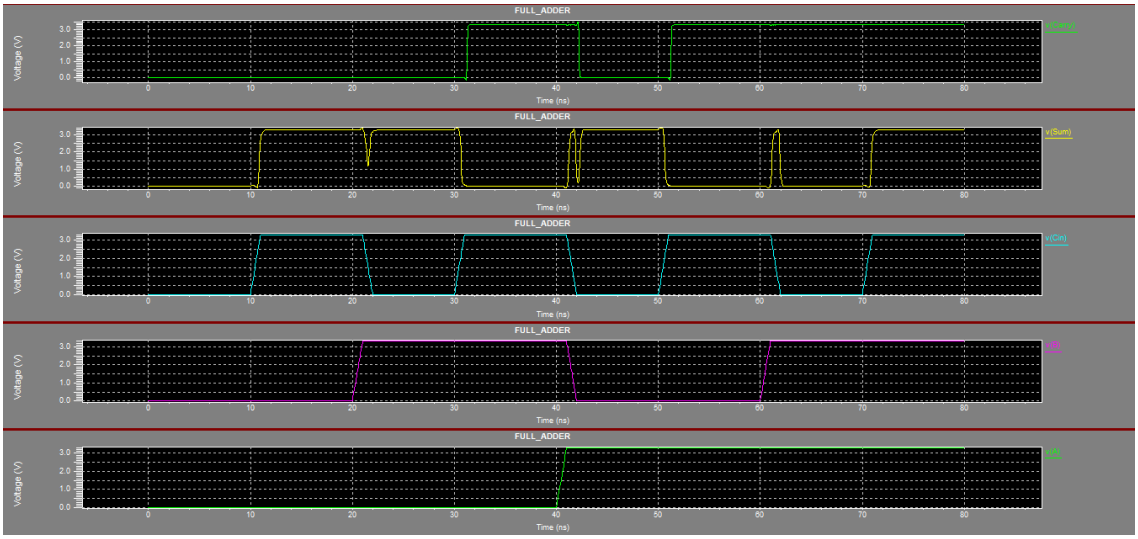
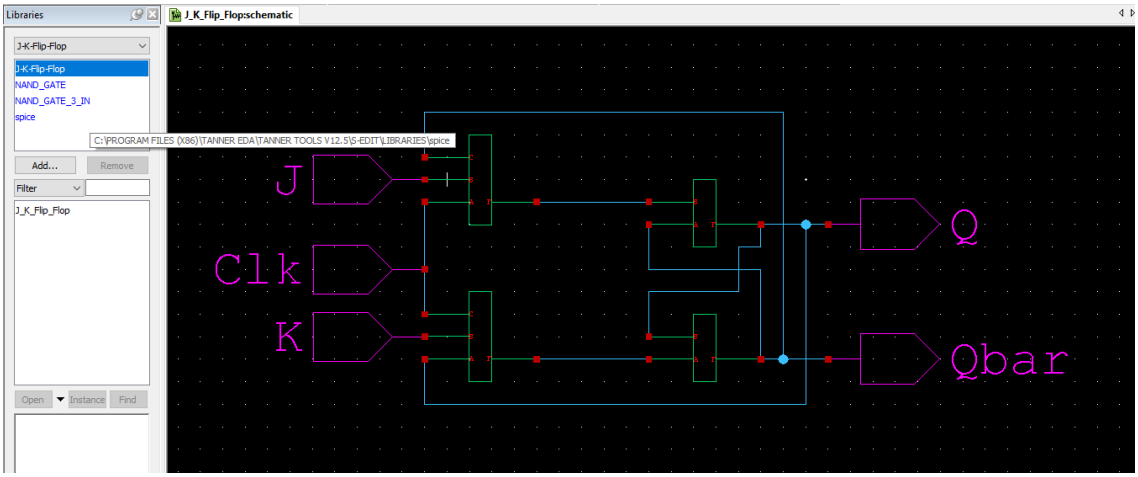


Q5. Design J-K flip-flop in S-edit using instances of earlier designed NAND and Not gates as symbols, simulate for transient analysis in T-spice. Calculate propagation delay using the generated waveform.



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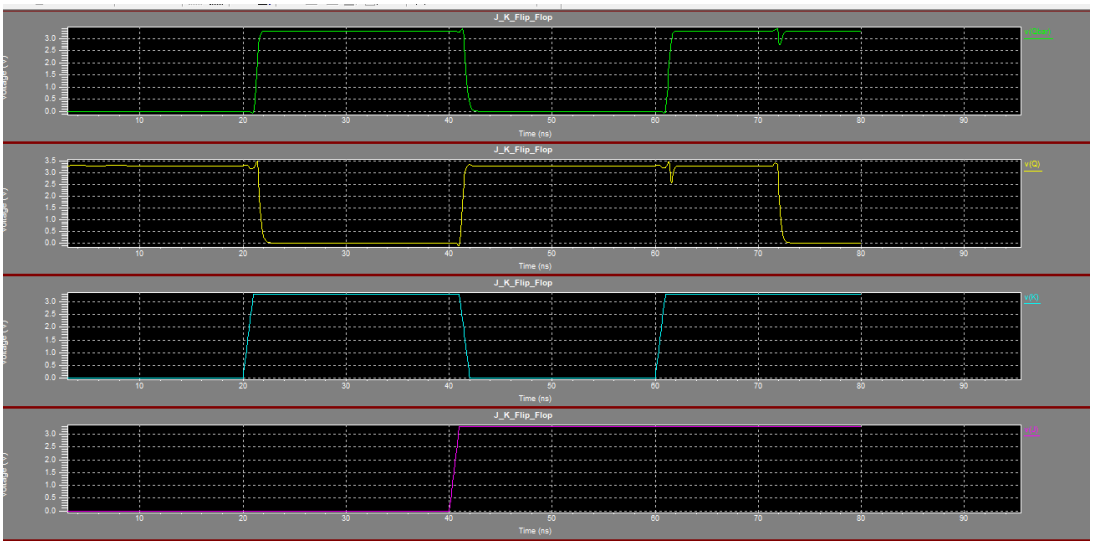
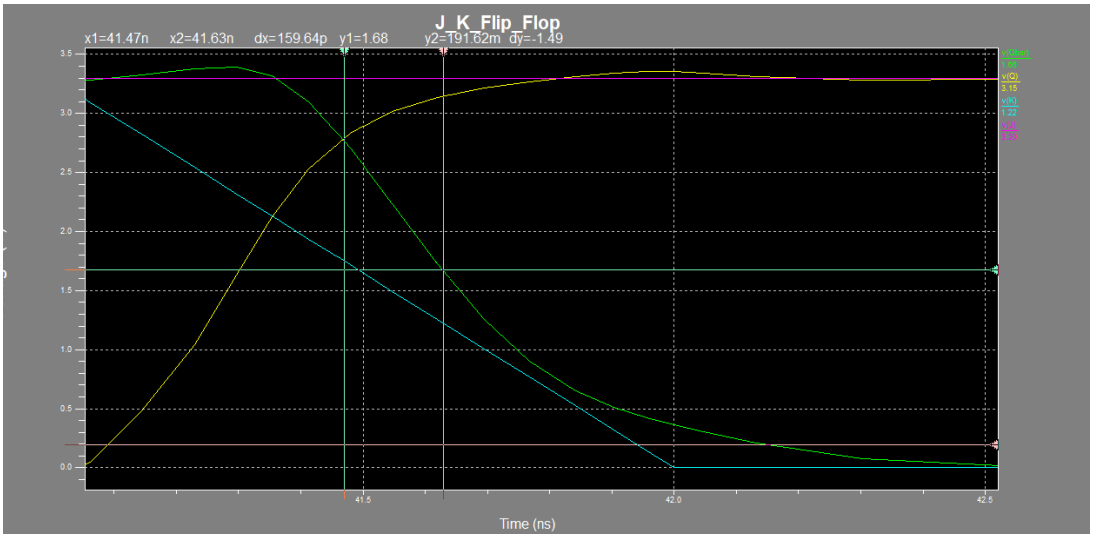
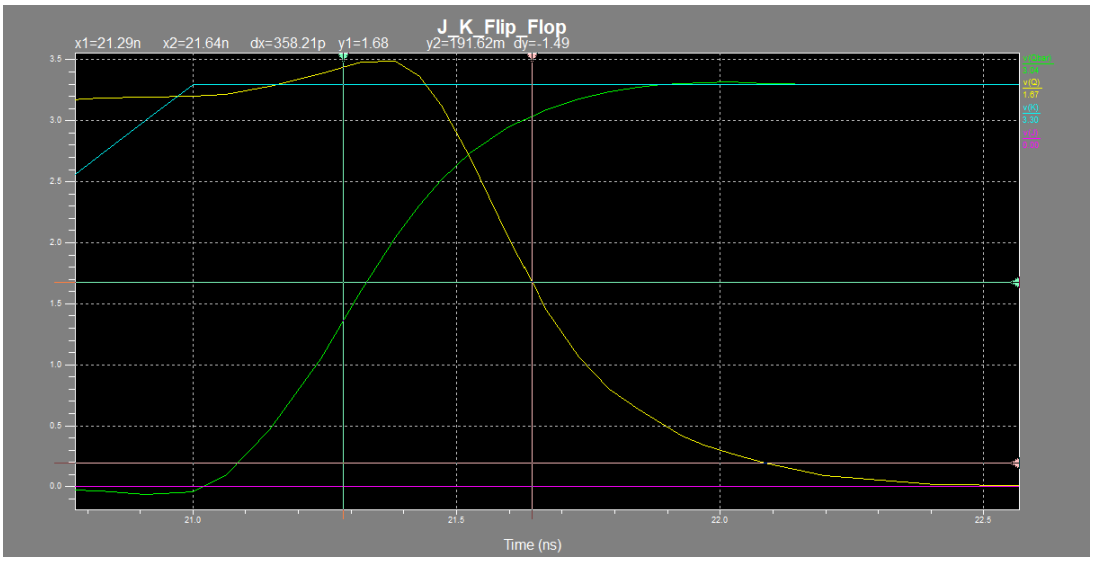
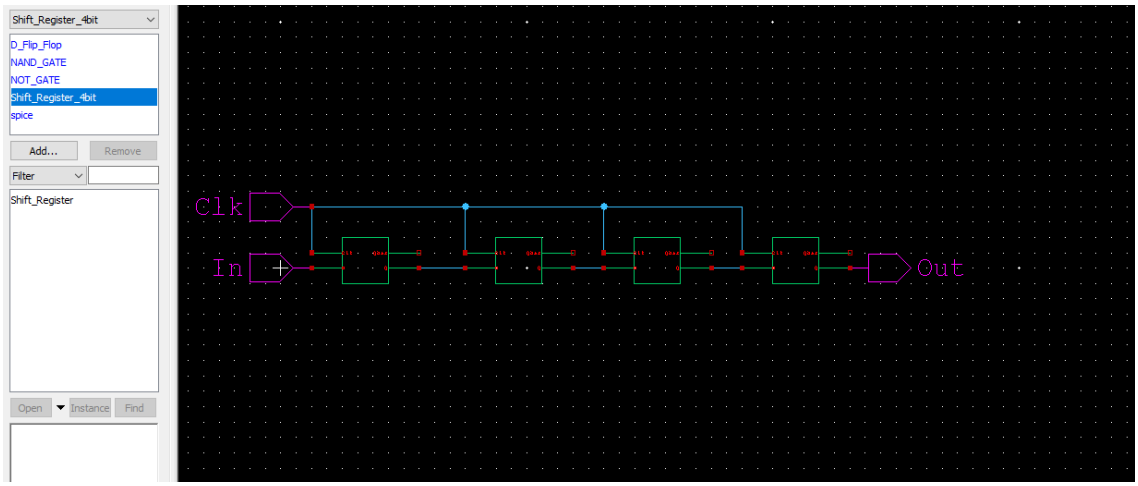



J_K_Flip_Flop
x1=41.47n x2=41.63n dx=159.64p y1=1.68 y2=191.62m dy=-1.49
Time (ns)


J_K_Flip_Flop
x1=21.29n x2=21.64n dx=358.21p y1=1.68 y2=191.62m dy=-1.49
Time (ns)

Q6. Design 4 bit Shift register using D flip-flop in S-edit, simulate for transient analysis in Tspice. Verify the functionality by giving input pattern 1101 in serial fashion.

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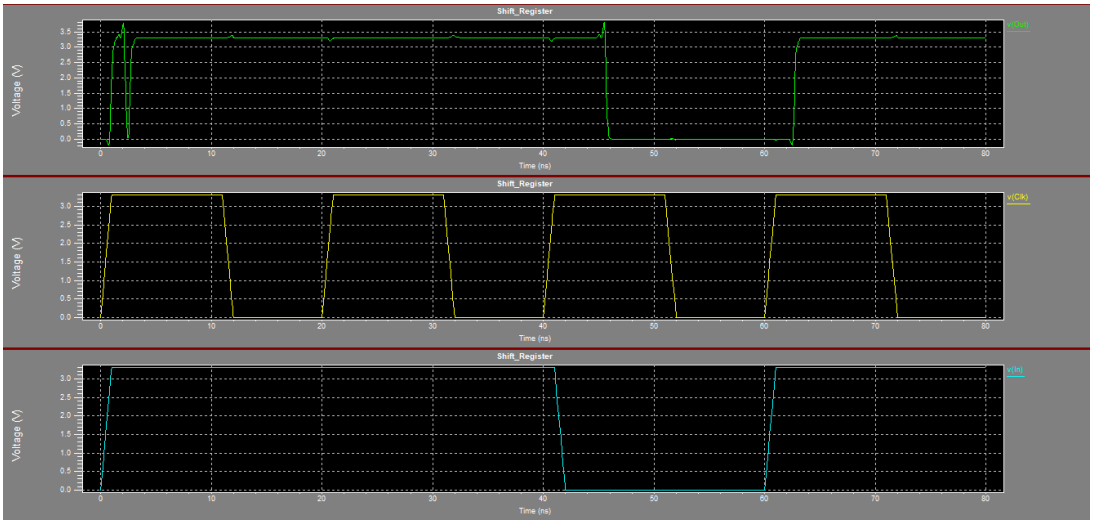
XD_Flip_Flop_1 Clk In N_1 N_2 Gnd Vdd D_Flip_Flop
XD_Flip_Flop_2 Clk N_1 N_3 N_4 Gnd Vdd D_Flip_Flop
XD_Flip_Flop_3 Clk N_3 N_5 N_6 Gnd Vdd D_Flip_Flop
XD_Flip_Flop_4 Clk N_5 Out N_7 Gnd Vdd D_Flip_Flop

********* Simulation Settings - Analysis section *********
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)

Vdd Vdd Gnd 3.3V
Vin1 In Gnd pulse(0 3.3v 0 1n 1n 40n 60n)
Vin2 Clk Gnd pulse(0 3.3v 0 1n 1n 10n 20n)
.Tran 1ns 80ns
.print V(In) V(Clk) V(Out)
********* Simulation Settings - Additional SPICE commands *
********

.end
```



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