CA-2

ECE 390: **WORKSHOP ON ANALOG DESIGN USING CADENCE VIRTUOSO**

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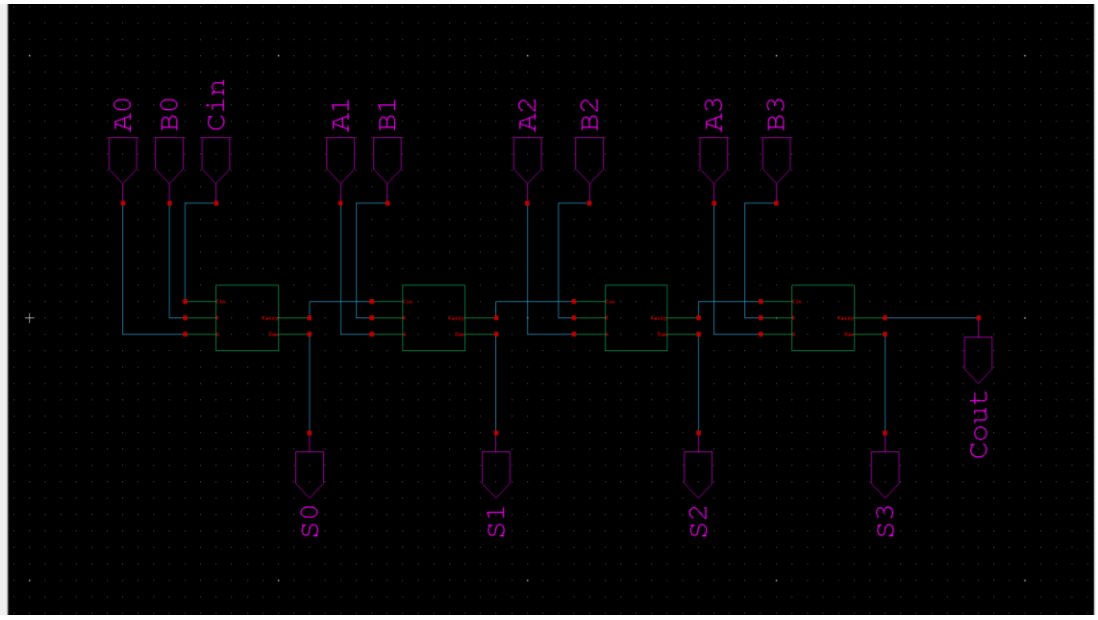
Section:_____E1901____ Roll No:_15____ Registration No: 11904463___

Max Marks: 30

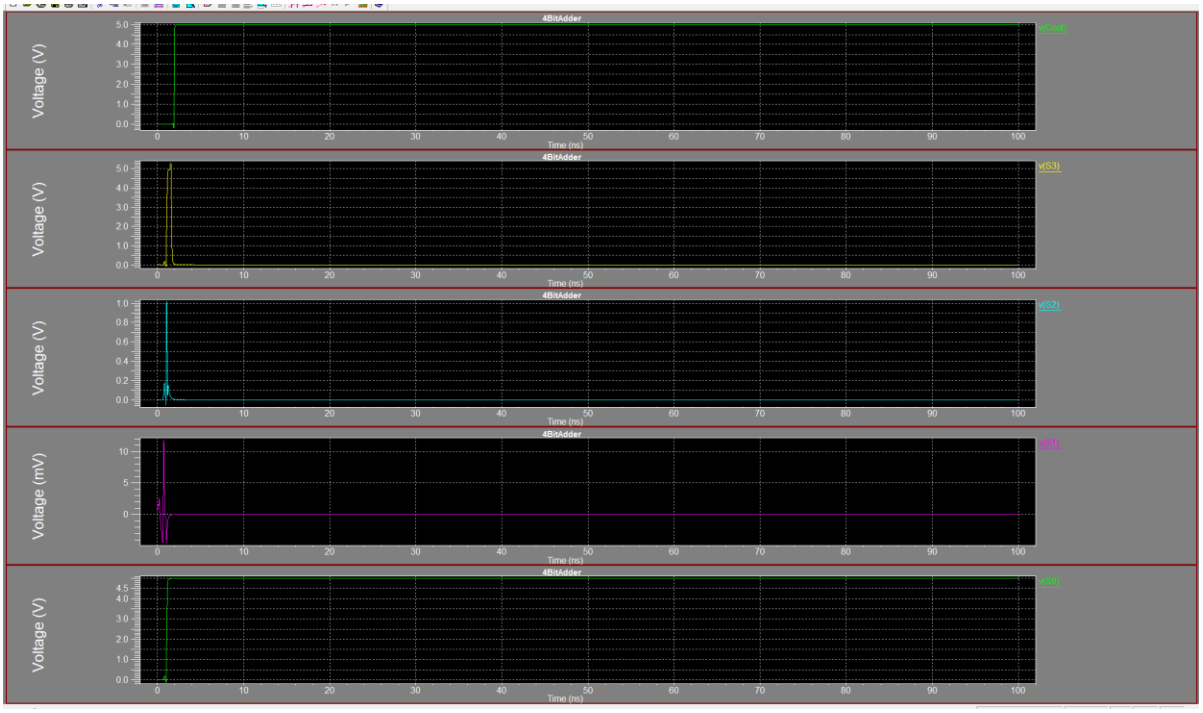
Q1. Design a 4-bit adder using tanner tool using created symbol of full adder circuit. Verify the operation using spice simulation for A=1010 and B=0111.



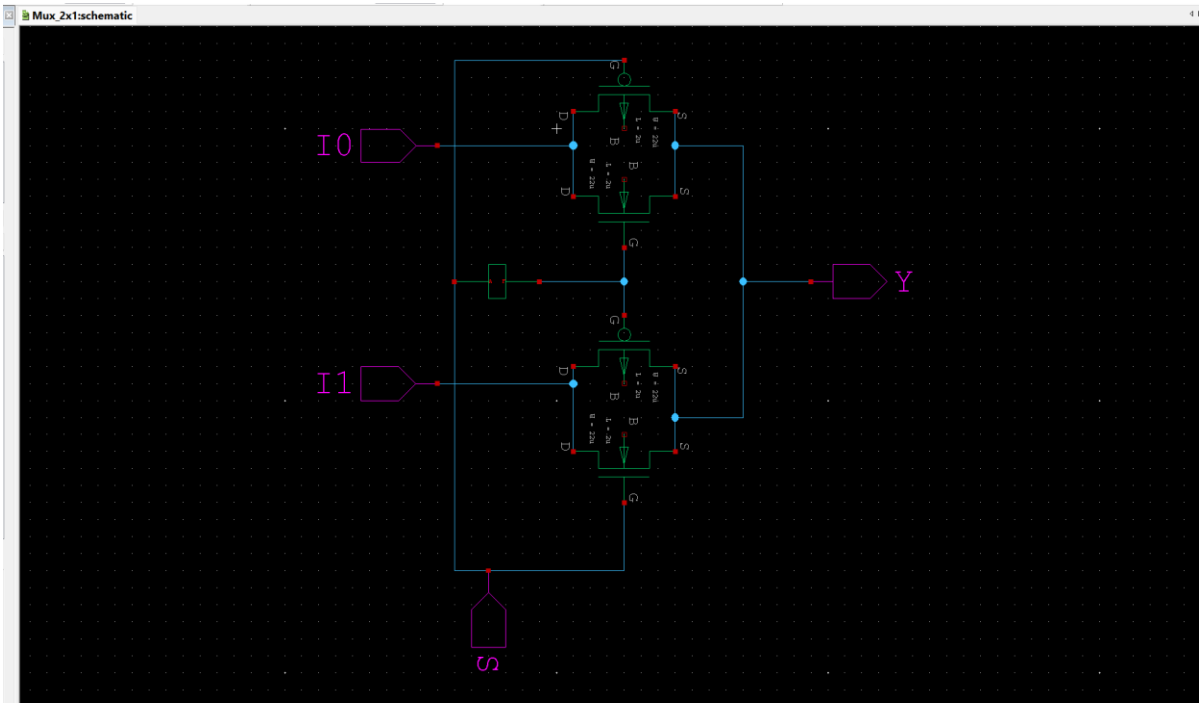
T-Spice - [4BitAdder]

File Edit View Simulation Table Setup Window Help

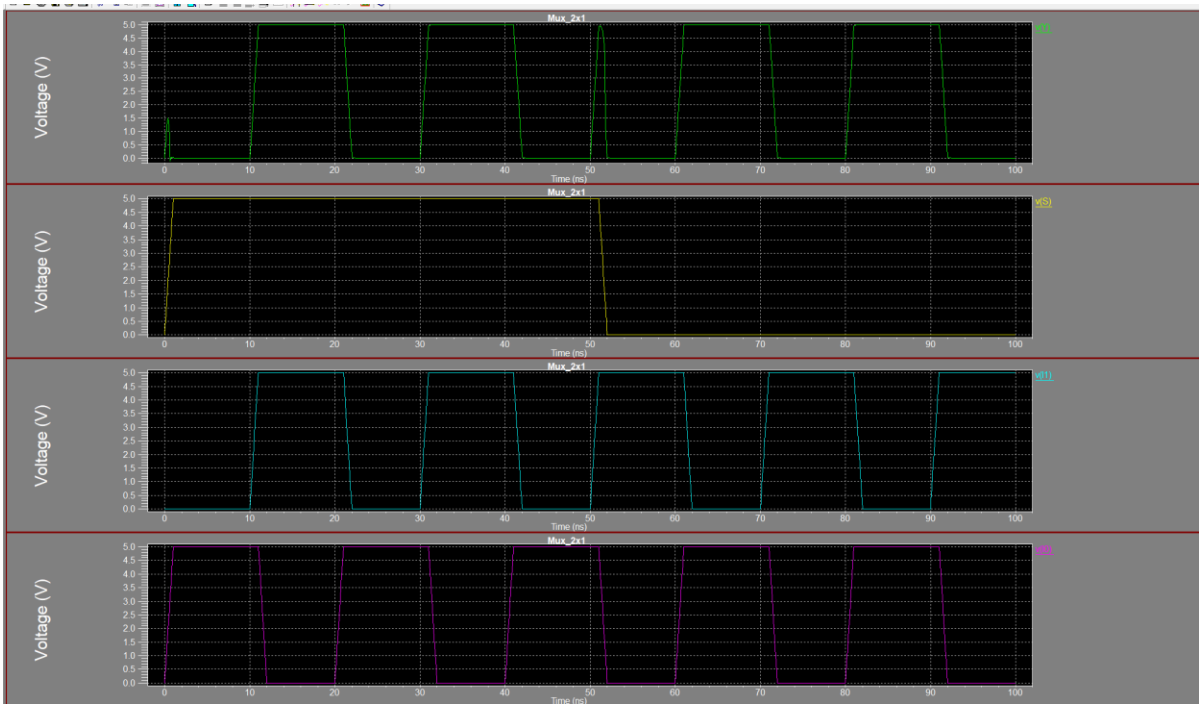
```
MMOSFET_P_15 Sum N_18 N_14 N_14 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_16 Sum Cin N_15 N_15 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_17 N_15 N_16 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_18 N_14 N_4 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_19 N_18 Cin Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
.ends


********* Simulation Settings - Parameters and SPICE Options *********

XFULL_ADDER_1 A0 B0 N_1 Cin S0 Gnd Vdd FULL_ADDER
XFULL_ADDER_2 A1 B1 N_2 N_1 S1 Gnd Vdd FULL_ADDER
XFULL_ADDER_3 A2 B2 N_3 N_2 S2 Gnd Vdd FULL_ADDER
XFULL_ADDER_4 A3 B3 Cout N_3 S3 Gnd Vdd FULL_ADDER

********* Simulation Settings - Analysis section *********

.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V

Vin1 A0 Gnd pulse(0 5v 100n 1n 1n 100n 100n)
Vin2 B0 Gnd pulse(0 5v 0 1n 1n 100n 100n)
Vin3 Cin Gnd pulse(0 5v 100n 1n 1n 100n 100n)

Vin4 A1 Gnd pulse(0 5v 0 1n 1n 100n 100n)
Vin5 B1 Gnd pulse(0 5v 0 1n 1n 100n 100n)

Vin6 A2 Gnd pulse(0 5v 100n 1 1n 100n 100n)
Vin7 B2 Gnd pulse(0 5v 0 1n 1n 100n 100n)

Vin8 A3 Gnd pulse(0 5v 0 1n 1n 100n 100n)
Vin9 B3 Gnd pulse(0 5v 100n 1n 1n 100n 100n)

.Tran 1ns 100ns

**.print V(A0) V(B0) V(Cin) V(A1) V(B1) V(A2) V(B2) V(A3) V(B3)
.print V(S0) V(S1) V(S2) V(S3) V(Cout)


********* Simulation Settings - Additional SPICE commands *********

.end
```



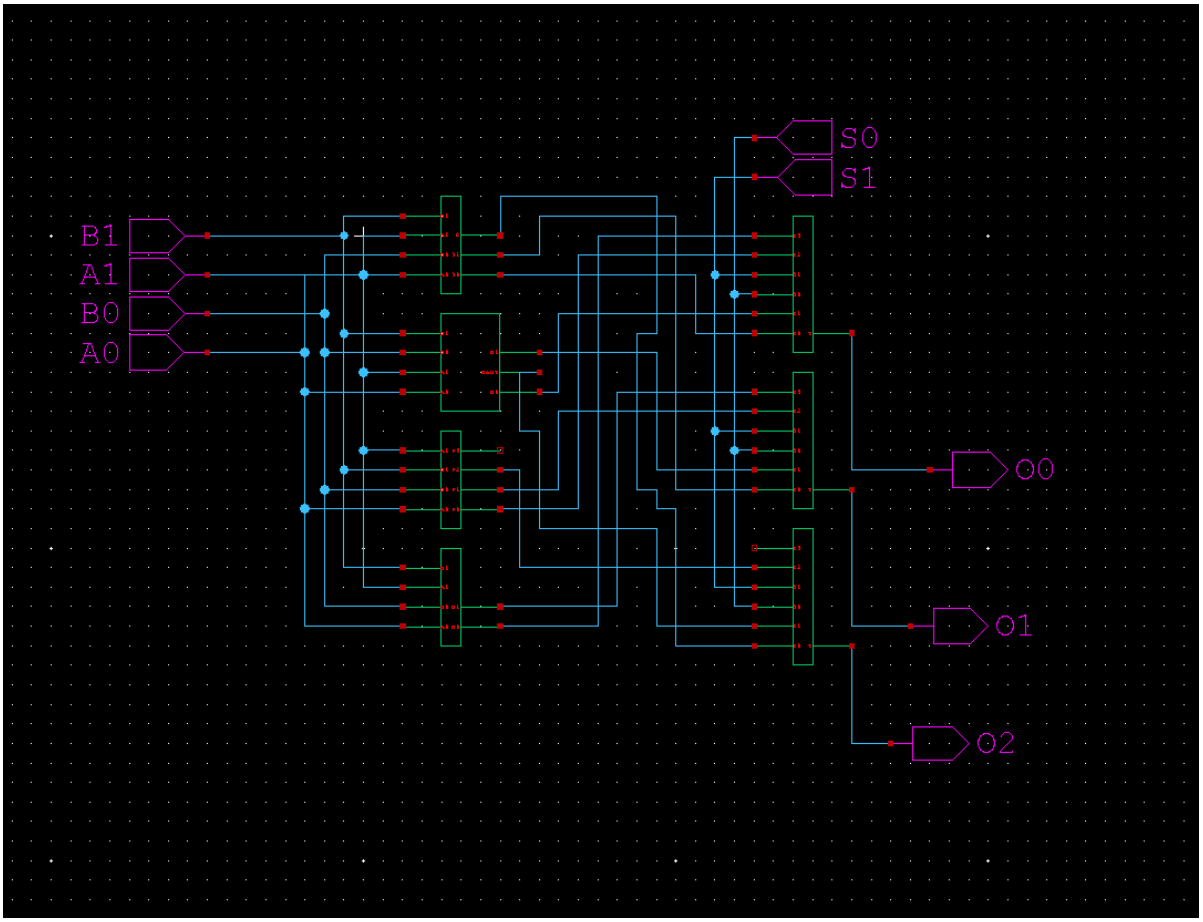
Q2. Implement 2x1 Mux using transmission gate technology and simulate on tanner tool. Attach the screenshots of S-edit, T-spice and W-Edit of the same.



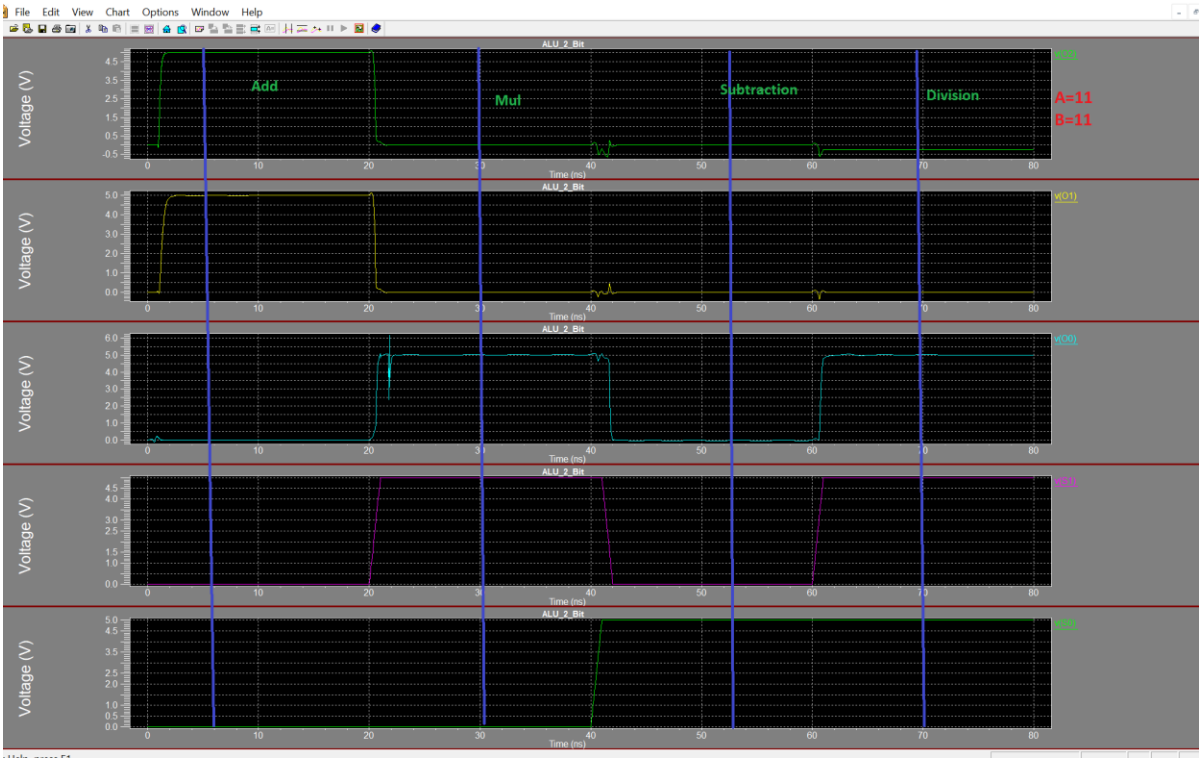

```
* Expand paths: yes
* Root path: D:\ECE\AnalogDesign\Mux\Mux_2x1
* Exclude global pins on subcircuits: no
* Export control property name: SPICE
* Wrap lines: no (to 0 characters)

********* Simulation Settings - General section *********

*************** Subcircuits *****************
.subckt NOT_GATE A F Gnd Vdd
MMOSFET_N_1 F A Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 F A Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
.ends


********* Simulation Settings - Parameters and SPICE Options *********

MMOSFET_N_1 I0 N_2 Y N_1 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 I1 S Y N_3 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 I0 S Y N_4 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 I1 N_2 Y N_5 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
XNOT_GATE_1 S N_2 Gnd Vdd NOT_GATE

********* Simulation Settings - Analysis section *********

.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)

Vdd Vdd Gnd 5V

Vin1 I0 Gnd pulse(0 5v 0 1n 1n 10n 20n)
Vin2 I1 Gnd pulse(0 5v 10n 1n 1n 10n 20n)

Vin3 S Gnd pulse(0 5v 0 1n 1n 50n 100n)

.Tran 1ns 100ns
.print V(I0) V(I1) V(S) V(Y)

********* Simulation Settings - Additional SPICE commands *********

.end
```



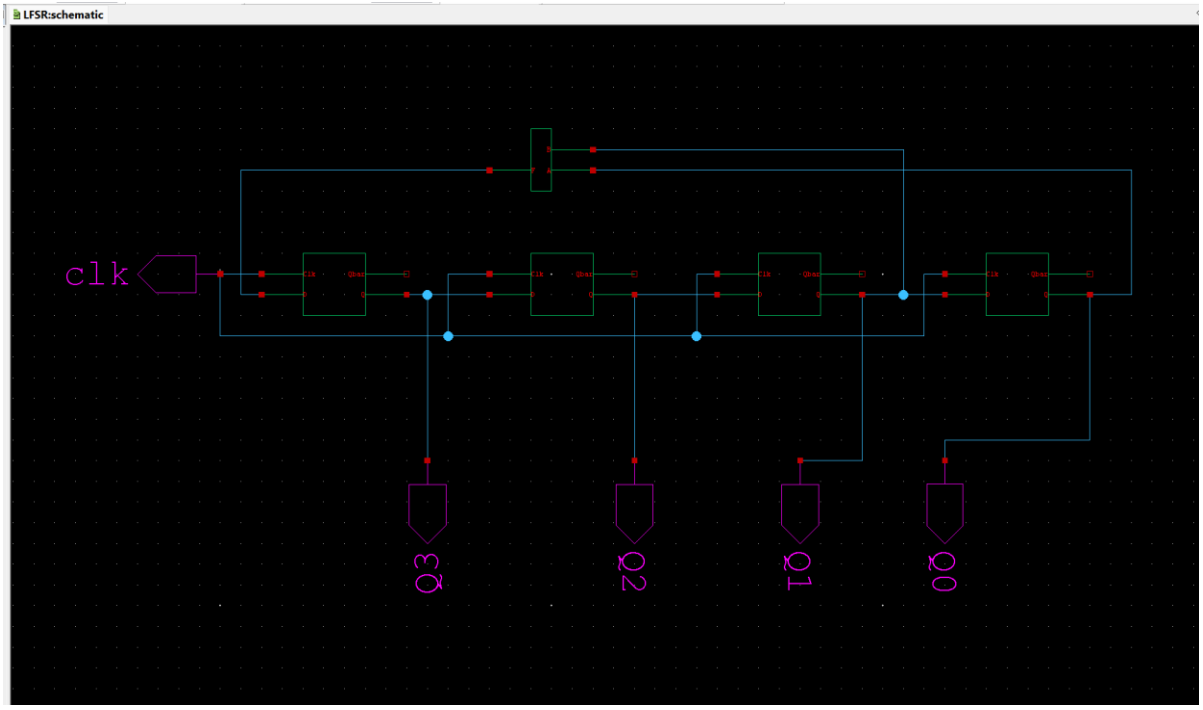
Q3. Design ALU capable to perform addition, subtraction, multiplication and division operations on two 2-bit numbers in S-edit, simulate for transient analysis in T-spice. Indicate each operation separately in the wave-form using vertical bars.



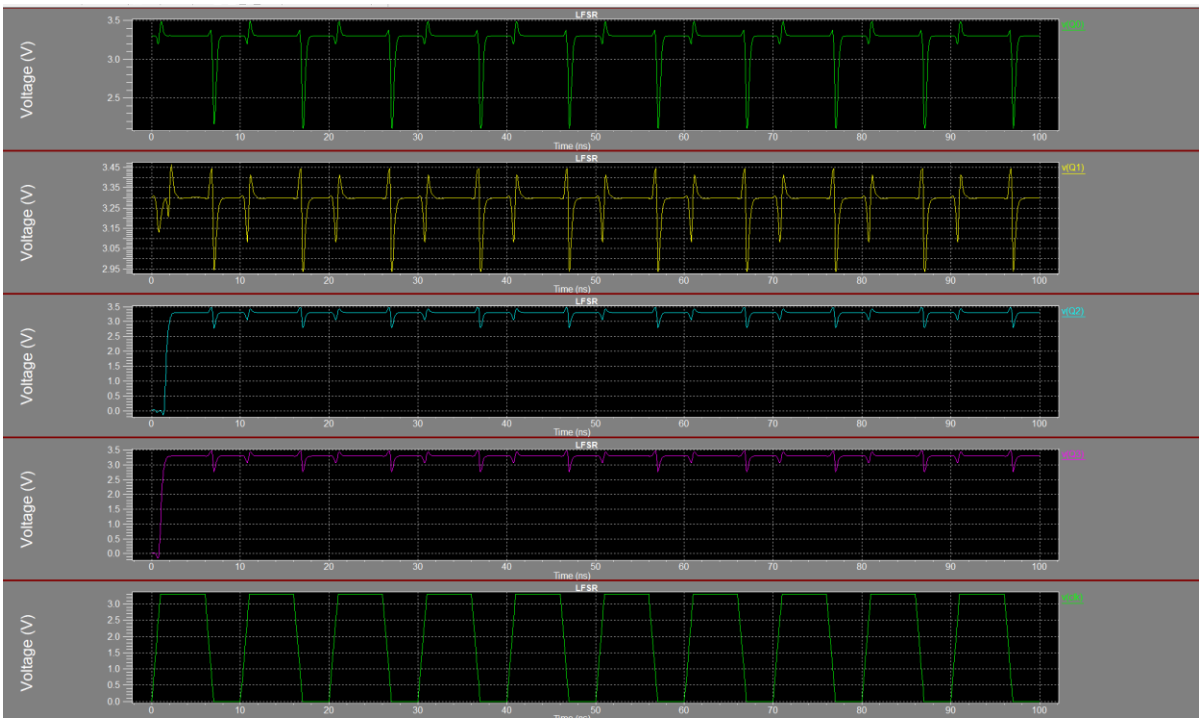

```
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 5V

Vin1 A0 Gnd pulse(0 5v 0 1n 1n 100n 100n)
Vin2 B0 Gnd pulse(0 5v 0 1n 1n 100n 100n)

Vin3 A1 Gnd pulse(0 5v 0 1n 1n 100n 100n)
Vin4 B1 Gnd pulse(0 5v 0n 1n 1n 100n 100n)

Vin5 S0 Gnd pulse(0 5v 40n 1n 1n 40n 80n)
Vin6 S1 Gnd pulse(0 5v 20n 1n 1n 20n 40n)

.Tran 1ns 80ns

.print V(S0) V(S1) V(O0) V(O1) V(O2)
********* Simulation Settings - Additional SPICE commands *********

.end
```



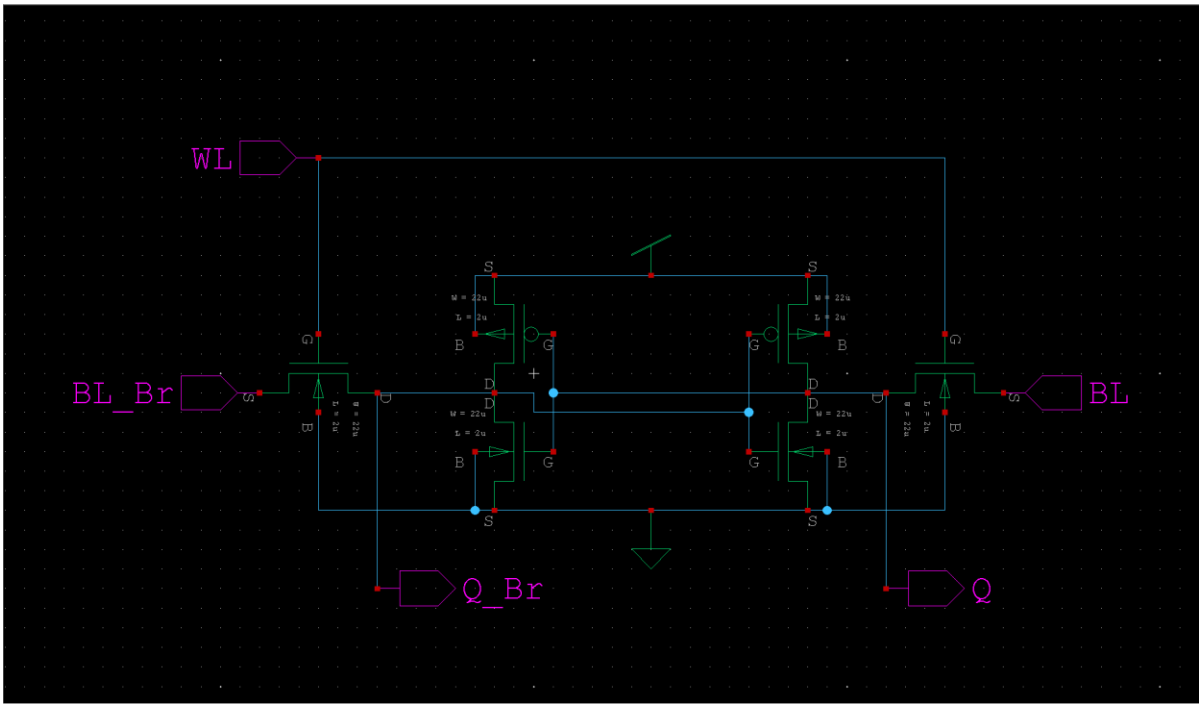
Q4. Implement 4-bit LFSR circuit with characteristic equation $1+ x + x^4$ in S-edit using D-flip-flops and Ex-OR gate. Simulate the same and identify number of non-identical patterns generated in the waveform.



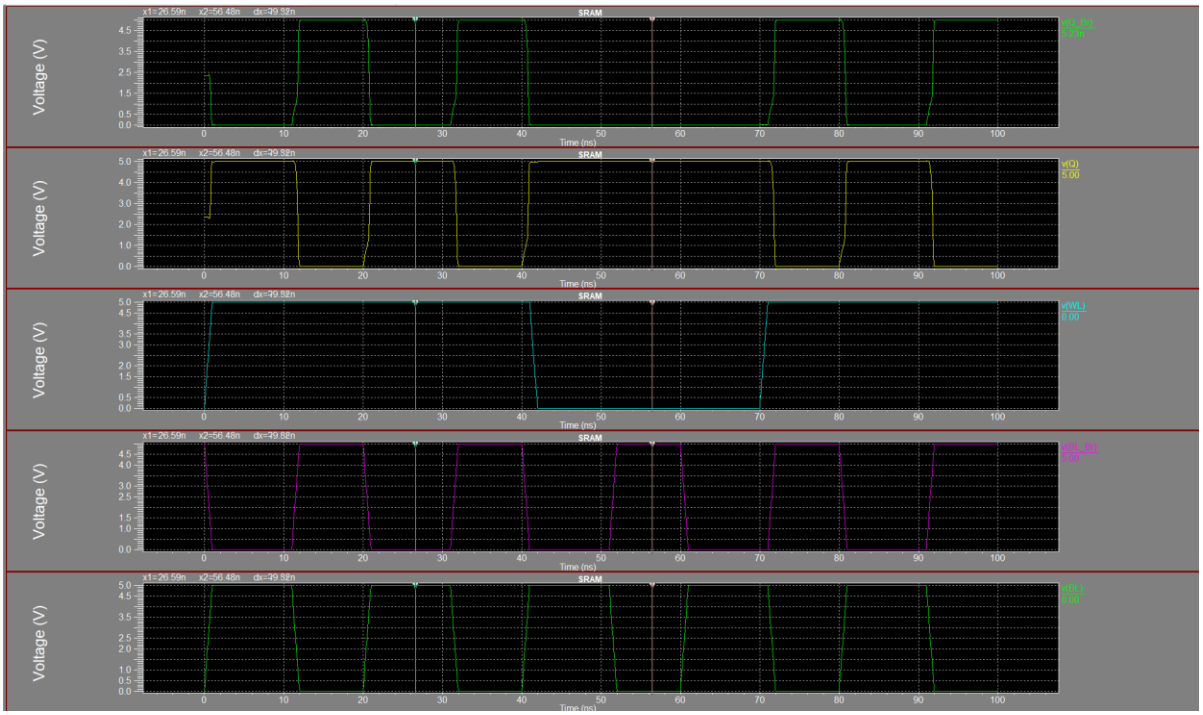
```
********* Simulation Settings - Parameters and SPICE Options *********

XD_Flip_Flop_1 clk N_1 Q3 N_2 Gnd Vdd D_Flip_Flop
XD_Flip_Flop_2 clk Q3 Q2 N_3 Gnd Vdd D_Flip_Flop
XXNOR_1 Q0 Q1 N_1 Gnd Vdd XNOR
XD_Flip_Flop_3 clk Q2 Q1 N_4 Gnd Vdd D_Flip_Flop
XD_Flip_Flop_4 clk Q1 Q0 N_5 Gnd Vdd D_Flip_Flop

********* Simulation Settings - Analysis section *********
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)

Vdd Vdd Gnd 3.3V
Vin clk Gnd pulse(0 3.3v 0 1n 1n 5n 10n)
.Tran 1ns 100ns
.print V(clk) V(Q3) V(Q2) V(Q1) V(Q0)
********* Simulation Settings - Additional SPICE commands *********

.end
```



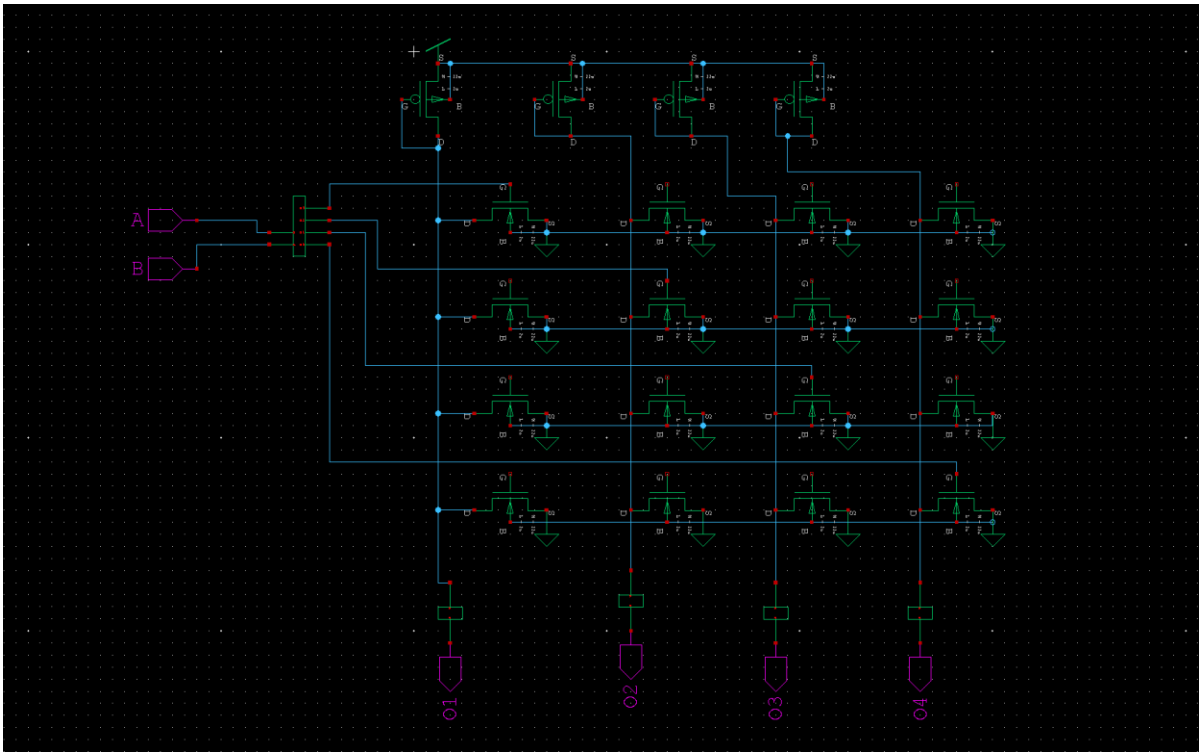
Q5. Design 1-bit 6T-SRAM cell in S-edit. Choose the timings wisely to show storage of logic 0 and logic 1 in the waveform. Also verify the Read/Write operation using vertical bars




```
MMOSFET_N_1 Q Q_Br Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 Q_Br Q Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_1 Q_Br Q Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_3 Q_Br WL BL_Br Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 Q Q_Br Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_4 Q WL BL Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

********* Simulation Settings - Analysis section *********
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)

Vdd Vdd Gnd 5V

Vin1 BL Gnd pulse(0 5v 0 1n 1n 10n 20n)
Vin2 BL_Br Gnd pulse(5v 0 0 1n 1n 10n 20n)
Vin3 WL Gnd pulse(0 5v 0 1n 1n 40n 70n)

.Tran 1ns 100ns
.print V(BL) V(BL_Br) V(WL) V(Q) V(Q_Br)
********* Simulation Settings - Additional SPICE commands *********

.end
```



Q6. Design 4X4 ROM using NMOS and perform the read operation using 2x4 address decoder. Verify the functionality after storing data “1000”, “0100”, “0010”, “0001”.



```
********* Simulation Settings - Parameters and SPICE Options *********

MMOSFET_P_1 N_1 N_1 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_2 N_4 N_4 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_3 N_5 N_5 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_P_4 N_2 N_2 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
XNOT_GATE_1 N_1 O1 Gnd Vdd NOT_GATE
XNOT_GATE_2 N_4 O2 Gnd Vdd NOT_GATE
XNOT_GATE_3 N_5 O3 Gnd Vdd NOT_GATE
XNOT_GATE_4 N_2 O4 Gnd Vdd NOT_GATE
MMOSFET_N_1 Gnd N_3 N_1 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_2 Gnd N_11 N_1 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_3 Gnd N_12 N_1 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_4 Gnd N_14 N_1 N_13 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_5 Gnd N_15 N_4 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_6 Gnd N_22 N_4 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_7 Gnd N_16 N_4 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_10 Gnd N_6 N_5 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_8 Gnd N_17 N_4 N_13 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_11 Gnd N_28 N_5 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_9 Gnd N_18 N_5 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_12 Gnd N_7 N_5 N_13 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_13 Gnd N_8 N_2 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_14 Gnd N_9 N_2 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_15 Gnd N_10 N_2 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
MMOSFET_N_16 Gnd N_37 N_2 N_13 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
XDEC2x4_1 B A N_37 N_28 N_22 N_3 Gnd Vdd DEC2x4

********* Simulation Settings - Analysis section *********
.Model NMOS NMOS(Vto=0.8V Kp=45u Lambda=0.01 Gamma=0.4 phi=0.6)
.Model PMOS PMOS (Vto=-0.9V Kp=33u Lambda=0.02 Gamma=0.4 phi=0.6)
Vdd Vdd Gnd 3.3V
Vin1 A Gnd pulse(0 3.3v 0 1n 1n 25n 50n)
Vin2 B Gnd pulse(0 3.3v 0 1n 1n 40n 80n)
.Tran 1ns 100ns
.print V(A) V(B) V(O1) V(O2) V(O3) V(O4)
********* Simulation Settings - Additional SPICE commands *********

.end
```