SWC_INT

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Data Structure Index

Data Structures

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File Index

File List

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Data Structure Documentation

GICR_type Union Reference

: Type define of Union bit field of "General INT Control Register" #include <INT priv.h>

Collaboration diagram for GICR_type:



Data Fields

- <u>u8 u_Reg</u>
- struct {
- <u>IO u8</u>: 5
- <u>IO u8 m_INT2E</u>: 1
- <u>IO u8 m INT0E</u>: 1
- <u>IO u8 m_INT1E</u>: 1
- } <u>sBits</u>

Detailed Description

: Type define of Union bit field of "General INT Control Register"

Type: Union Unit: None

Field Documentation

__IO u8 m_INT0E

External Interrupt Request Enable 0

__<u>IO</u> <u>u8</u> m_INT1E

External Interrupt Request Enable 1

__<u>IO u8</u> m_INT2E

External Interrupt Request Enable 2

struct { ... } sBits

Reversed

u8 u_Reg

The documentation for this union was generated from the following file:

INT_priv.h

GIFR_type Union Reference

: Type define of Union bit field of "General INT Flag Register"

#include <INT priv.h>

Collaboration diagram for GIFR_type:



Data Fields

- <u>u8</u> <u>u Reg</u>
- struct {
- <u>IO u8</u>: 5
- <u>IO u8 m INT2F</u>: 1
- <u>IO u8 m INT0F</u>: 1
- <u>IO u8 m INT1F</u>: 1
- } <u>sBits</u>

Detailed Description

: Type define of Union bit field of "General INT Flag Register"

Type: Union Unit: None

Field Documentation

__IO u8 m_INT0F

External Interrupt Request Flag 0

IO u8 m_INT1F

External Interrupt Request Flag 1

External Interrupt Request Flag 2

```
struct { ... } sBits
```

Reversed

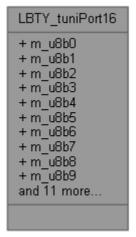
u8 u_Reg

The documentation for this union was generated from the following file:

INT_priv.h

LBTY_tuniPort16 Union Reference

#include <LBTY_int.h>
Collaboration diagram for LBTY_tuniPort16:



Data Fields

- struct {
- <u>u8 m_u8b0</u>:1
- <u>u8 m u8b1</u>:1
- <u>u8 m_u8b2</u>:1
- <u>u8 m u8b3</u>:1
- <u>u8 m u8b4</u>:1
- u8 m_u8b5:1
- <u>u8 m u8b6</u>:1
- <u>u8 m_u8b7</u>:1
- <u>u8 m u8b8</u>:1
- <u>u8</u> <u>m_u8b9</u>:1
- <u>u8 m_u8b10</u>:1
- <u>u8 m u8b11</u>:1
- <u>u8 m_u8b12</u>:1
- <u>u8 m u8b13</u>:1
- <u>u8 m_u8b14</u>:1
- <u>u8 m_u8b15</u>:1
- } <u>sBits</u>
- struct {
- <u>u8 m_u8low</u>
- <u>u8 m_u8high</u>
- } <u>sBytes</u>
- <u>u16 u u16Word</u>

Field Documentation

```
u8 m_u8b0
u8 m_u8b1
u8 m_u8b10
u8 m_u8b11
u8 m_u8b12
u8 m_u8b13
u8 m_u8b14
u8 m_u8b15
u8 m_u8b2
u8 m_u8b3
u8 m_u8b4
<u>u8</u> m_u8b5
u8 m_u8b6
u8 m_u8b7
u8 m_u8b8
u8 m_u8b9
u8 m_u8high
u8 m_u8low
struct { ... } sBits
struct { ... } sBytes
<u>u16</u> u_u16Word
```

The documentation for this union was generated from the following file:

• H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_BSW/<u>LBTY int.h</u>

LBTY_tuniPort8 Union Reference

#include <LBTY_int.h>
Collaboration diagram for LBTY_tuniPort8:



Data Fields

- struct {
- <u>u8 m_u8b0</u>:1
- <u>u8 m_u8b1</u>:1
- <u>u8 m_u8b2</u>:1
- <u>u8 m u8b3</u>:1
- <u>u8 m_u8b4</u>:1
- <u>u8 m_u8b5</u>:1
- <u>u8 m u8b6</u>:1
- <u>u8 m_u8b7</u>:1
- } <u>sBits</u>
- <u>u8 u_u8Byte</u>

Detailed Description

Union Byte bit by bit

Field Documentation

```
      u8 m_u8b0

      u8 m_u8b1

      u8 m_u8b2

      u8 m_u8b3

      u8 m_u8b4

      u8 m_u8b5

      u8 m_u8b6

      u8 m_u8b7

      struct {...} sBits

      u8 u_u8Byte
```

The documentation for this union was generated from the following file:

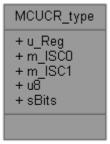
• H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_BSW/<u>LBTY_int.h</u>

MCUCR_type Union Reference

: Type define of Union bit field of "MCU Control Register"

#include <INT_priv.h>

Collaboration diagram for MCUCR_type:



Data Fields

- <u>u8 u_Reg</u>
- struct {
- <u>IO u8 m_ISC0</u>: 2
- <u>IO u8 m ISC1</u>: 2
- <u>IO u8</u>: 4
- } <u>sBits</u>

Detailed Description

: Type define of Union bit field of "MCU Control Register"

Type: Union Unit: None

Field Documentation

```
10 u8 m_ISC0
```

Interrupt 0 Sense Control

__IO u8 m_ISC1

Interrupt 1 Sense Control

struct { ... } sBits

<u>IO u8</u>

Reversed

u8 u_Reg

The documentation for this union was generated from the following file:

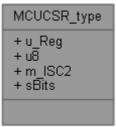
INT_priv.h

MCUCSR_type Union Reference

: Type define of Union bit field of "Control and Status Register"

#include <INT priv.h>

Collaboration diagram for MCUCSR_type:



Data Fields

- <u>u8 u_Reg</u>
- struct {
- <u>IO u8</u>: 6
- <u>IO u8 m ISC2</u>: 1
- } <u>sBits</u>

Detailed Description

: Type define of Union bit field of "Control and Status Register"

Type: Union Unit: None

Field Documentation

__<u>IO u8</u> m_ISC2

Interrupt 2 Sense Control

struct { ... } sBits

Reversed

u8 u_Reg

The documentation for this union was generated from the following file:

INT_priv.h

SREG_type Union Reference

: Type define of Union bit field of "General INT Control Register" $\verb§\#include= < INTP.h>$

Collaboration diagram for SREG_type:



Data Fields

- <u>u8 u_Reg</u>
- struct {
- <u>IO u8 m C</u>: 1
- <u>IO u8 m Z</u>: 1
- <u>IO u8 m N</u>: 1
- <u>IO</u> <u>u8</u> <u>m_V</u>: 1
- <u>IO u8 m S</u>: 1
- <u>IO u8 m_H</u>: 1
- <u>IO u8 m T</u>: 1
- <u>IO u8 m_I</u>: 1
- } <u>sBits</u>

Detailed Description

: Type define of Union bit field of "General INT Control Register"

Type: Union Unit: None

Field Documentation

__<u>IO</u> <u>u8</u> m_C

Carry Flag

__<u>IO</u> <u>u8</u> m_H

Half Carry Flag

__<u>IO</u> <u>u8</u> m_I

Global Interrupt Enable

```
___IO_u8 m_N
Negative Flag
___IO_u8 m_S
Sign Bit
___IO_u8 m_T
Bit Copy Storage
___IO_u8 m_V
Two's Complement Overflow Flag
___IO_u8 m_Z
Zero Flag
struct {...} sBits
____8 u_Reg
```

The documentation for this union was generated from the following file:

• H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_MCU/<u>INTP.h</u>

File Documentation

H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_BSW/LBIT_int.h File Reference

Macros

- #define <u>BV</u>(bit) (1u<<(bit))
- #define \underline{SET} \underline{BIT} (REG, bit) ((REG) |= (1u<<(bit)))
- #define $\underline{\text{CLR BIT}}(\text{REG}, \text{ bit}) ((\text{REG}) \&= \sim (1u << (\text{bit})))$
- #define TOG_BIT(REG, bit) ((REG) ^= (1u<<(bit)))
- #define SET BYTE(REG, bit) ((REG) |= (0xFFu<<(bit)))
- #define $\overline{\text{CLR BYTE}}(\text{REG}, \text{ bit}) ((\text{REG}) \&= \sim (0xFFu << (\text{bit})))$
- #define TOG BYTE(REG, bit) ((REG) ^= (0xFFu<<(bit)))
- #define <u>SET_MASK(REG, MASK)</u> ((REG) |= (MASK))
- #define <u>CLR_MASK(REG, MASK)</u> ((REG) &= ~(MASK))
- #define TOG_MASK(REG, MASK) ((REG) ^= (MASK))
- #define GET MASK(REG, MASK) ((REG) & (MASK))
- #define $\underline{SET}_REG(REG)$ ((REG) = \sim (0u))
- #define $\underline{CLR} \ \underline{REG}(REG) \ ((REG) = (0u))$
- #define $\underline{TOG_REG}(REG)$ ((REG) $^= \sim (0u)$)
- #define GET_BIT(REG, bit) (((REG)>>(bit)) & 0x01u)
- #define GET NIB(REG, bit) (((REG)>>(bit)) & 0x0Fu)
- #define GET_BYTE(REG, bit) (((REG)>>(bit)) & 0xFFu)
- #define <u>ASSIGN_BIT</u>(REG, bit, value) $((REG) = ((REG) \& \sim (0x01u << (bit))) | (((value) \& 0x01u) << (bit)))$
- #define <u>ASSIGN_NIB</u>(REG, bit, value) $((REG) = ((REG) \& \sim (0x0Fu << (bit))) | (((value) \& 0x0Fu) << (bit)))$
- #define $\underline{ASSIGN_BYTE}(REG, bit, value)$ ((REG) = ((REG) & ~(0xFFu<<(bit))) (((value) & 0xFFu)<<(bit)))
- #define CON u8Bits(b7, b6, b5, b4, b3, b2, b1, b0)

(0b##b7##b6##b5##b4##b3##b2##b1##b0)

• #define <u>CON u16Bits</u>(b15, b14, b13, b12, b11, b10, b9, b8, b7, b6, b5, b4, b3, b2, b1, b0)

(0b##b15##b14##b13##b12##b11##b10##b9##b8##b7##b6##b5##b4##b3##b2##b1##b0)

Macro Definition Documentation

```
#define BV(bit) (1u<<(bit))
#define ASSIGN_BIT( REG, bit, value) ((REG) = ((REG) & \sim(0x01u<<(bit)))
                                                                            I
(((value) & 0x01u)<<(bit)))
#define ASSIGN BYTE( REG, bit, value) ((REG) = ((REG) & ~(0xFfu<<(bit)))
                                                                            Τ
(((value) & 0xFFu)<<(bit)))
#define ASSIGN_NIB( REG, bit, value) ((REG) = ((REG) & \sim(0x0Fu<<(bit)))
                                                                            I
(((value) & 0x0Fu)<<(bit)))
#define CLR_BIT( REG, bit) ((REG) &= ~(1u<<(bit)))
#define CLR_BYTE( REG, bit) ((REG) &= ~(0xFFu<<(bit)))
#define CLR_MASK( REG, MASK) ((REG) &= ~(MASK))
#define CLR_REG( REG) ((REG) = (0u))
#define CON_u16Bits( b15, b14, b13, b12, b11, b10, b9, b8, b7, b6, b5,
b4, b3, b2, b1, b0)
       (0b##b15##b14##b13##b12##b11##b10##b9##b8##b7##b6##b5##b4##b3##b2##
b1##b0)
#define CON_u8Bits( b7, b6, b5, b4, b3, b2, b1, b0)
      (0b##b7##b6##b5##b4##b3##b2##b1##b0)
#define GET_BIT( REG, bit) (((REG)>>(bit)) & 0x01u)
#define GET_BYTE( REG, bit) (((REG)>>(bit)) & 0xFFu)
#define GET_MASK( REG, MASK) ((REG) & (MASK))
#define GET_NIB( REG, bit) (((REG)>>(bit)) & 0x0Fu)
#define SET_BIT( REG, bit) ((REG) |= (1u<<(bit)))
   Bitwise Operation
```

```
#define SET_BYTE( REG, bit) ((REG) |= (0xFFu<<(bit)))

#define SET_MASK( REG, MASK) ((REG) |= (MASK))

#define SET_REG( REG) ((REG) = ~(0u))

#define TOG_BIT( REG, bit) ((REG) ^= (1u<<(bit)))

#define TOG_BYTE( REG, bit) ((REG) ^= (0xFFu<<(bit)))

#define TOG_MASK( REG, MASK) ((REG) ^= (MASK))

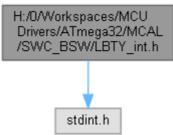
#define TOG_REG( REG) ((REG) ^= ~(0u))
```

LBIT_int.h

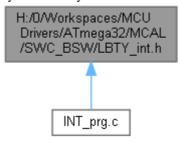
```
Go to the documentation of this file.1 /*
3 /* **********
4 /* File Name : LBIT_int.h
5 /* Author : MAAM
6 /* Version : v01
7 /* date : Mar 24, 2023
8 \ /* \ description : Bitwise Library
9 /* *********
11 /* ***********
12
13 #ifndef LBIT INT H
14 #define LBIT INT H
15
17 /* ***************** TYPE DEF/STRUCT/ENUM SECTION ***************** */
19
23
24 #define _BV(bit)
                                              (1u<<(bit))
25
27 #define SET BIT(REG, bit)
                                           ((REG) \mid = (1u << (bit)))
28 #define CLR BIT(REG, bit)
                                           ((REG) &= ~(1u<<(bit)))
29 #define TOG_BIT(REG, bit)
                                           ((REG) ^= (1u<<(bit)))
30
                                          ((REG) |= (0xFFu<<(bit)))
((REG) &= ~(0xFFu<<(bit)))
31 #define SET_BYTE(REG, bit)
32 #define CLR BYTE (REG, bit)
33 #define TOG BYTE (REG, bit)
                                           ((REG) ^= (0xFFu<<(bit)))
34
                                           ((REG) |= (MASK))
35 #define SET MASK (REG, MASK)
36 #define CLR MASK (REG, MASK)
                                           ((REG) &= ~(MASK))
                                           ((REG) ^= (MASK))
((REG) & (MASK))
37 #define TOG_MASK(REG, MASK)
38 #define GET MASK(REG, MASK)
39
                                           ((REG) = \sim (0u))
((REG) = (0u))
40 #define SET_REG(REG)
41 #define CLR REG(REG)
42 #define TOG REG(REG)
                                           ((REG) ^= \sim (Ou))
43
44 #define GET BIT(REG, bit)
                                           (((REG) >> (bit)) \& 0x01u)
45 #define GET NIB(REG, bit)
                                           (((REG)>>(bit)) & 0x0Fu)
46 #define GET BYTE (REG, bit)
                                           (((REG)>>(bit)) & 0xFFu)
47
48 #define ASSIGN BIT (REG, bit, value)
                                          ((REG) = ((REG) \& \sim (0x01u << (bit)))
| (((value) \& 0x01u) << (bit)))
49 #define ASSIGN NIB(REG, bit, value)
                                          ((REG) = ((REG) \& \sim (0x0Fu << (bit)))
| (((value) & 0x0Fu)<<(bit)))
50 #define ASSIGN_BYTE(REG, bit, value)
                                          ((REG) = ((REG) & \sim (0xFFu << (bit)))
| (((value) & 0xFFu) << (bit)))
51
52 /*
53 #define ASSIGN BIT(REG, bit, value)
                                           do{
54
                                            REG &= \sim (0 \times 01 u << bit);
55
                                            REG \mid= ((value & 0x01u)<<bit);
56
                                           }while(0)
57 */
58
       bits together in an u8 register
59 /*
60 #define CON_u8Bits(b7, b6, b5, b4, b3, b2, b1, b0)
61
(0b##b7##b6##b5##b4##b3##b2##b1##b0)
            bits together in an u16 register
64 #define CON u16Bits(b15, b14, b13, b12, b11, b10, b9, b8, b7, b6, b5, b4, b3, b2, b1,
b0) \
```

H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_BSW/LBTY_int.h File Reference

#include <stdint.h>
Include dependency graph for LBTY_int.h:



This graph shows which files directly or indirectly include this file:



Data Structures

• union <u>LBTY tuniPort8</u>union <u>LBTY tuniPort16</u>

Macros

- #define __IO volatile
- #define __O volatile
- #define __I volatile const
- #define <u>LBTY_u8vidNOP()</u>
- #define <u>LBTY NULL</u> ((void *) 0U)
- #define $\underline{LBTY_u8ZERO}$ (($\underline{u8}$)0x00U)
- #define <u>LBTY u8MAX</u> ((<u>u8</u>)0xFFU)
- #define LBTY $\underline{\text{S8MAX}}$ (($\underline{\text{s8}}$)0x7F)
- #define <u>LBTY_s8MIN</u> ((<u>s8</u>)0x80)
- #define LBTY u16ZERO ((u16)0x0000U)
- #define <u>LBTY_u16MAX</u> ((<u>u16</u>)0xFFFFU)
- #define LBTY s16MAX ((u16)0x7FFF)
- #define LBTY s16MIN ((u16)0x8000)
- #define <u>LBTY u32ZERO</u> ((<u>u32</u>)0x0000000UL)
- #define <u>LBTY u32MAX</u> ((<u>u32</u>)0xFFFFFFFUL)
- #define <u>LBTY_s32MAX</u> ((<u>u32</u>)0x7FFFFFFL)
- #define <u>LBTY s32MIN</u> ((<u>u32</u>)0x80000000L)
- #define <u>LBTY_u64ZERO</u> ((<u>u64</u>)0x0000000000000000ULL)
- #define <u>LBTY u64MAX</u> ((<u>u64</u>)0xFFFFFFFFFFFFFFULL)
- #define <u>LBTY_s64MAX</u> ((<u>u64</u>)0x7FFFFFFFFFFFFFLL)
- #define <u>LBTY_s64MIN</u> ((<u>u64</u>)0x8000000000000000LL)

Typedefs

- typedef uint8_t <u>u8</u>
- typedef uint16_t <u>u16</u>
- typedef uint32_t <u>u32</u>
- typedef uint64_t <u>u64</u>
- typedef int8_t s8
- typedef int16_t <u>s16</u>
- typedef int32_t <u>s32</u>
- typedef int64_t <u>s64</u>
- typedef float <u>f32</u>
- typedef double <u>f64</u>
- typedef <u>u8</u> * <u>pu8</u>
- typedef <u>u16</u> * <u>pu16</u>
- typedef <u>u32</u> * <u>pu32</u>
- typedef <u>u64</u> * <u>pu64</u>
- typedef $\underline{s8} * \underline{ps8}$
- typedef <u>s16</u> * <u>ps16</u>
- typedef $\underline{s32} * \underline{ps32}$
- typedef <u>s64</u> * <u>ps64</u>

Enumerations

- enum <u>LBTY_tenuFlagStatus</u> { <u>LBTY_RESET</u> = 0, <u>LBTY_SET</u> = !LBTY_RESET }
- enum <u>LBTY tenuBoolean</u> { <u>LBTY TRUE</u> = 0x55, <u>LBTY FALSE</u> = 0xAA }
- enum <u>LBTY_tenuErrorStatus</u> { <u>LBTY_OK</u> = (u16)0, <u>LBTY_NOK</u>, <u>LBTY_NULL_POINTER</u>, <u>LBTY_INDEX_OUT_OF_RANGE</u>, <u>LBTY_NO_MASTER_CHANNEL</u>, <u>LBTY_READ_ERROR</u>, <u>LBTY_WRITE_ERROR</u>, <u>LBTY_UNDEFINED_ERROR</u>, <u>LBTY_IN_PROGRESS</u> }

Macro Definition Documentation

```
#define I volatile const
#define __IO volatile
#define O volatile
#define LBTY_NULL ((void *) 0U)
#define LBTY_s16MAX ((u16)0x7FFF)
#define LBTY_s16MIN ((u16)0x8000)
#define LBTY_s32MAX ((u32)0x7FFFFFFL)
#define LBTY_s32MIN ((<u>u32</u>)0x80000000L)
#define LBTY_s64MAX ((u64)0x7FFFFFFFFFFFLL)
#define LBTY s64MIN ((u64)0x800000000000000LL)
#define LBTY_s8MAX ((s8)0x7F)
#define LBTY_s8MIN ((s8)0x80)
#define LBTY_u16MAX ((u16)0xFFFFU)
#define LBTY_u16ZERO ((<u>u16</u>)0x0000U)
#define LBTY_u32MAX ((u32)0xFFFFFFFUL)
#define LBTY_u32ZERO ((<u>u32</u>)0x0000000UL)
#define LBTY_u64MAX ((u64)0xFFFFFFFFFFFFFULL)
#define LBTY_u64ZERO ((<u>u64</u>)0x00000000000000ULL)
#define LBTY_u8MAX ((u8)0xFFU)
#define LBTY_u8vidNOP()
#define LBTY_u8ZERO ((u8)0x00U)
   Data Types Limitation
```

Typedef Documentation

typedef float f32

Standard Real Decimal number

```
typedef double f64
typedef s16* ps16
typedef s32* ps32
typedef <u>s64</u>* <u>ps64</u>
typedef s8* ps8
   Standard Pointer to Signed Byte/Word/Long_Word
typedef u16* pu16
typedef u32* pu32
typedef u64* pu64
typedef u8* pu8
   Standard Pointer to Unsigned Byte/Word/Long_Word
typedef int16_t s16
typedef int32_t s32
typedef int64_t s64
typedef int8_t s8
   Standard Signed Byte/Word/Long_Word
typedef uint16_t u16
typedef uint32_t u32
typedef uint64_t u64
typedef uint8_t u8
   Data Types New Definitions Standard Unsigned Byte/Word/Long_Word
```

Enumeration Type Documentation

enum <u>LBTY_tenuBoolean</u>

Boolean type

Enumerator:

```
LBTY_TRUE

LBTY_FALSE

96 {
97  LBTY TRUE = 0x55,
98  LBTY FALSE = 0xAA
99 } LBTY tenuBoolean;
```

enum <u>LBTY_tenuErrorStatus</u>

Error Return type

Enumerator:

```
LBTY_OK
       LBTY_NOK
  LBTY_NULL_PO
            INTER
  LBTY_INDEX_O
   UT_OF_RANGE
   LBTY_NO_MAS
   TER_CHANNEL
  LBTY_READ_ER
              ROR
  LBTY_WRITE_E
             RROR
  LBTY_UNDEFIN
       ED_ERROR
  LBTY_IN_PROG
             RESS
102
103 LBTY OK = (u16)0,
104 LBTY NOK,
105 LBTY NULL POINTER,
106 LBTY INDEX OUT OF RANGE,
107 LBTY NO MASTER CHANNEL,
107 LBTY NO MASTER CHANNEL,
108 LBTY READ ERROR,
      LBTY WRITE ERROR,
LBTY UNDEFINED ERROR,
109
110
111 LBTY IN PROGRESS
                                /* Error is not available, wait for availability */
112 } LBTY tenuErrorStatus;
```

enum <u>LBTY_tenuFlagStatus</u>

Flag Status type

Enumerator:

```
LBTY_RESET

LBTY_SET

90
91
LBTY_RESET = 0,
92
LBTY_SET = !LBTY_RESET
93 } LBTY_tenuflagStatus;
```

LBTY_int.h

```
Go to the documentation of this file.1 /*
3 /* ***********
4 /* File Name : LBTY_int.h
5 /* Author : MAAM
6 /* Version : v01
7 /* date : Mar 23, 2023
8 /* description : Basic Library
9 /* **********
11 /* ***********
12
13 #ifndef _LBTY_INT_H_
14 #define _LBTY_INT_H_
15
16 #include <stdint.h>
17
21
               <u>u8</u>;
<u>u16</u>;
<u>u32</u>;
<u>u64</u>;
24 typedef uint8 t
25 typedef uint1\overline{6} t
26 typedef uint32 t
27 typedef uint64_t
28
               <u>sb</u>
<u>s16;</u>
<u>s32;</u>
<u>s64</u>
30 typedef int8 t
31 typedef int16_t
32 typedef int32 t
33 typedef int64_t
34
36 typedef float
37 typedef double
                 <u>f64</u>;
38
40 typedef u8*
              pu16;
pu32;
pu64;
41 typedef u16*
42 typedef \overline{u32}*
43 typedef <u>u64</u>*
44
46 typedef s8*
                ps8 ;
47 typedef <u>s16</u>*
              <u>ps16;</u>
<u>ps32;</u>
<u>ps64</u>;
48 typedef \frac{1}{832}*
49 typedef <u>s64</u>*
50
54
60
61 #define LBTY u8vidNOP()
62 #define LBTY NULL
                    ((void *) OU)
63
65 #define LBTY_u8ZERO ((u8)0x00U)
66 #define LBTY_u8MAX ((u8)0xFFU)
67 #define LBTY_s8MAX ((s8)0x7F)
68 #define LBTY_s8MIN ((s8)0x80)
69
70 #define LBTY_u16ZERO ((u16)0x0000U)
71 #define LBTY_u16MAX ((u16)0xFFFFU)
72 #define LBTY_s16MAX ((u16)0x7FFF)
73 #define LBTY_s16MIN ((u16)0x8000)
74
75 #define LBTY_u32ZERO ((u32)0x00000000UL)
76 #define LBTY_u32MAX ((u32)0xFFFFFFFFUL)
77 #define LBTY_s32MAX ((u32)0x7FFFFFFFFL)
77 #define LBTY_s32MAX
78 #define LBTY_s32MIN
                     ((u32)0x7FFFFFFFL)
                  ((u32)0x7FFFFFFFL)
((u32)0x80000000L)
79
```

```
80 #define LBTY u64ZERO ((u64)0x000000000000000ULL)
81 #define LBTY_u64MAX ((u64)0xFFFFFFFFFFFFFFFLLL)

82 #define LBTY_s64MAX ((u64)0x7FFFFFFFFFFFFLL)

83 #define LBTY_s64MIN ((u64)0x8000000000000000LL)
84
87 /* **************
88
90 typedef enum {
    LBTY RESET = 0,
LBTY SET = !LBTY RESET
91
92
93 } LBTY tenuFlagStatus;
94
96 typedef enum {
97 LBTY TRUE = 0x55,
98 \overline{LBTY FALSE} = 0xAA
99 } LBTY_tenuBoolean;
100
102 typedef enum {
     \underline{LBTY OK} = (\underline{u16}) 0,
103
104 <u>LBTY NOK</u>,
105 LBTY NULL POINTER,
106 LBTY INDEX OUT OF RANGE,
107 LBTY NO MASTER CHANNEL,
108 LBTY READ ERROR,
     LBTY READ ERROR,
109 LBTY WRITE ERROR,
110 LBTY UNDEFINED ERROR,
111 LBTY IN PROGRESS
                             /* Error is not available, wait for availability */
112 } LBTY tenuErrorStatus;
113
116 /* ****************
117
119 typedef union {
120 struct {
                      // LSB
      <u>u8</u> <u>m u8b0</u> :1;
121
      <u>u8</u> <u>m u8b1</u> :1;
<u>u8</u> <u>m u8b2</u> :1;
122
123
124
       <u>u8</u> <u>m u8b3</u> :1;
<u>u8</u> <u>m u8b4</u> :1;
125
126
       u8 m u8b5 :1;

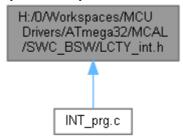
    u8
    m
    u8b6
    :1;

    u8
    m
    u8b7
    :1;

127
128
                         // MSB
129 } sBits;
130 <u>u8 u u8Byte</u>;
131 } LBTY tuniPort8;
132
133 typedef union {
134 struct {
    <u>u8</u> <u>m</u> u8b0
       <u>u8</u> <u>m u8b0</u> :1;
u8 <u>m u8b1</u> :1;
135
                           // LSB
136
                 :1;
      u8 m u8b2
u8 m u8b3
137
138
                   :1;
139
    u8 m u8b4 :1;
       <u>u8</u> <u>m u8b5</u>
<u>u8</u> <u>m u8b6</u>
140
                   :1;
                 :1;
141
142
       <u>u8</u> <u>m u8b7</u>
                 :1;
143
       u8 m u8b8
                  :1;
144
       u8 m u8b9 :1;
      <u>u8</u> m<u>u8b10</u> :1;
145
       u8 m u8b11 :1;
146
<u>u8</u> <u>m u8b15</u> :1;
                          // MSB
150
151 } sBits;
152 struct {
    u8 m u8low;
u8 m u8high;
153
154
155 } sBytes;
156
      u16 u u16Word;
157 } LBTY tuniPort16;
158
159 /* **************************
```

H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_BSW/LCTY_int.h File Reference

This graph shows which files directly or indirectly include this file:



Macros

- #define LCTY_PROGMEM __attribute__((__progmem__))
- #define <u>LCTY PURE</u> __attribute__((__pure__))
- #define <u>LCTY_INLINE</u> __attribute__((always_inline)) static inline
- #define <u>LCTY INTERRUPT</u> __attribute__((interrupt))
- #define <u>CTY_PACKED</u> __attribute__((__packed__))
- #define LCTY_CONST __attribute__((__const__))
- #define <u>LCTY_DPAGE</u> __attribute__((dp))
- #define <u>LCTY_NODPAGE</u> __attribute__((nodp))
- #define <u>LCTY_SECTION</u>(section) __attribute__((section(# section)))
- #define LCTY_ASM(cmd) __asm__ _volatile__ (# cmd ::)

Macro Definition Documentation

```
#define CTY_PACKED __attribute__((__packed__))

#define LCTY_ASM( cmd) __asm____volatile__ ( # cmd ::)

#define LCTY_CONST __attribute__((__const__))

#define LCTY_DPAGE __attribute__((dp))

#define LCTY_INLINE __attribute__((always_inline)) static inline

#define LCTY_INTERRUPT __attribute__((interrupt))

#define LCTY_NODPAGE __attribute__((nodp))

#define LCTY_PROGMEM __attribute__((__progmem__))

#define LCTY_PURE __attribute__((_pure__))

#define LCTY_SECTION( section) __attribute__((section( # section)))
```

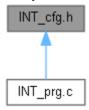
LCTY_int.h

```
Go to the documentation of this file.1 /*
3 /* ***********
4 /* File Name : LCTY_int.h
5 /* Author : MAAM
6 /* Version : v00
7 /* date : Apr 26, 2023
8 /* description : Compiler Library
9 /* ***********
11 /* ***********
12
13 #ifndef LCTY INT H
14 #define LCTY INT H
15
17 /* ***************** TYPE DEF/STRUCT/ENUM SECTION **************** */
19
21 /* ****************** MACRO/DEFINE SECTION **********************************
23
24 /* prog memory attribute */
25 #define LCTY PROGMEM
                    attribute (( progmem ))
26
27 /* pure attribute */
28 #define LCTY PURE
                    __attribute__((__pure__))
29
30 /* Abstraction for inlining */
31 //#define LCTY_INLINE
                    static inline
32 #define LCTY INLINE
                    __attribute__((always_inline)) static inline
33
34 /* define function as interrupt handler */
                    __attribute__((interrupt))
35 #define LCTY INTERRUPT
36
37 /* Memory packed to pass Memory padding */
38 #define CTY_PACKED
                   __attribute__((__packed ))
39
40 /* Const attribute */
41 #define LCTY CONST
                    __attribute__((__const__))
42
43 /* place variable in direct page */
44 #define LCTY_DPAGE
                     attribute ((dp))
45
46 /* do not place variable in direct page */
47 #define LCTY_NODPAGE __attribute__((nodp))
48
49 /* Sections */
50 #define LCTY SECTION(section) attribute ((section( # section)))
51
52 /* Abstraction for assembly command */
53 # define LCTY_ASM(cmd) __asm____volatile__ ( # cmd ::)
54
55 /* ******************
58
62
66
67
68 #endif /* LCTY INT H */
```

INT_cfg.c File Reference

INT_cfg.h File Reference

This graph shows which files directly or indirectly include this file:

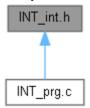


INT_cfg.h

```
Go to the documentation of this file.1 /*
3 /* ************
4 /* File Name : INT_cfg.h
11
12 #ifndef INT_CFG_H_
13 #define INT CFG H
14
18
21 /* *************************
22
23 #if defined(AMIT KIT)
24
25 #define INT_PUSH
      TNTO
26
27 #elif defined(ETA32 KIT)
28
29 #define INT_IR_RECEIVER INTO
30
31 #elif defined(ETA32 MINI KIT)
32
33 #define INT PUSH
      TNTO
34
35 #else
36
37 #endif
38
42
46
47 /*
49
50
51
```

INT_int.h File Reference

This graph shows which files directly or indirectly include this file:



Enumerations

- enum INT_tenuPin { INT0 = (u8)0u, INT1, INT2 }
- enum <u>INT tenuSenseControl</u> { <u>INT Low Level</u> = (u8)0u, <u>INT Logic Change</u>, <u>INT Falling Edge</u>, <u>INT Rising Edge</u>, <u>INT2 Falling Edge</u> = (u8)0u, <u>INT2 Rising Edge</u> }

Functions

- void INT vidInit (u8 u8INT Num)
- void INT_vidSetSenseControl (u8 u8INT_Num, INT_tenuSenseControl u8INT_SC)
- void <u>INT_vidEnable</u> (<u>u8</u> u8INT_Num)
- void INT vidDisable (u8 u8INT Num)
- void INT_vidSetFlag (u8 u8INT_Num)
- void <u>INT vidResetFlag</u> (<u>u8</u> u8INT_Num)
- void INT_vidSetCallBack (u8 u8INT_Num, void(*pvidCallback)(void))

Enumeration Type Documentation

enum INT_tenuPin

Enumerator:

```
INT0
INT1
INT2

19
20
INT0 = (u8) 0u,
21
INT1,
22
INT2
23 }INT tenuPin;
```

enum INT_tenuSenseControl

Enumerator:

```
INT_Low_Level
INT_Logic_Chang
e
INT_Falling_Edge
INT_Rising_Edge
INT2_Falling_Edg
e
INT2_Rising_Edg
e
INT2_Rising_Edg
e
INT2_Rising_Edg
e
INT2_Rising_Edg
```

Function Documentation

void INT_vidDisable (u8 u8INT_Num)

```
111
112
          switch (u8INT Num) {
                                        S GICR->sBits.m_INT0E = LBTY RESET;
S GICR->sBits.m_INT1E = LBTY RESET;
            case \overline{\text{INT0}}:
                                                                                                 break;
113
114
               case INT1:
                                                                                                  break;
115
               case INT2:
                                         S GICR->sBits.m INT2E = LBTY RESET;
                                                                                                  break;
116
               default:
                                        break;
117
118 }
```

void INT_vidEnable (u8 u8INT_Num)

```
98
       switch(u8INT Num){
99
         case INT\overline{0}:
                                S GICR->sBits.m INTOE = LBTY SET;
100
           case INT1:
                                 S GICR->sBits.m INT1E = LBTY SET;
                                                                                break;
101
            case INT2:
                                  S GICR->sBits.m INT2E = LBTY SET;
                                                                                break;
102
            default:
                                 break:
103
104 }
```

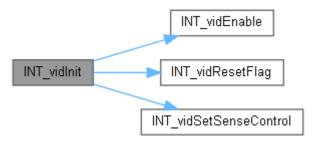
Here is the caller graph for this function:



void INT_vidInit (u8 u8INT_Num)

```
53
54
       switch(u8INT Num){
55
            case INTO:
                GPIO_u8SetPinDirection(INTO PORT, INTO PIN, PIN_INPUT);
INT vidSetSenseControl(u8INT_Num, INTO SC);
57
                INT vidEnable(u8INT Num);
58
59
                INT vidResetFlag(u8INT Num);
60
61
            case INT1:
               GPIO_u8SetPinDirection(INT1 PORT, INT1 PIN, PIN_INPUT);
62
                INT vidSetSenseControl(u8INT_Num, INT1 SC);
63
64
                INT vidEnable(u8INT Num);
                INT vidResetFlag(u8INT_Num);
65
66
               break;
67
            case INT2:
68
               GPIO_u8SetPinDirection(INT2 PORT, INT2 PIN, PIN_INPUT);
69
                INT vidSetSenseControl(u8INT Num, INT2 SC);
                INT vidEnable(u8INT Num);
70
71
                INT_vidResetFlag(u8INT_Num);
72
                break;
73
            default:
74
                break;
75
76 }
```

Here is the call graph for this function:



void INT_vidResetFlag (u8 u8INT_Num)

```
139
140
          switch(u8INT Num){
141
             case INT\overline{0}:
                                           S GIFR->sBits.m INTOF = LBTY RESET;
                                                                                                      break;
                                           S GIFR->sBits.m INT1F = LBTY RESET;
S GIFR->sBits.m INT2F = LBTY RESET;
142
                case \underline{\text{INT1}}:
                                                                                                      break:
                case INT2:
143
                                                                                                      break;
144
                default:
145
          }
146 }
```

Here is the caller graph for this function:



void INT_vidSetCallBack (u8 u8INT_Num, void(*)(void) pvidCallback)

```
153
154
        if(*pvidCallback == LBTY NULL)
155
        switch (u8INT Num) {
156
                                  INTO pvidCallback = pvidCallback;
          case INT\overline{0}:
                                                                                break;
                                  INT1 pvidCallback = pvidCallback;
157
            case <u>INT1</u>:
                                                                                break;
158
            case INT2:
                                  INT2 pvidCallback = pvidCallback;
                                                                                 break;
159
            default:
                                  break;
160
        }
161 }
```

void INT_vidSetFlag (u8 u8INT_Num)

```
125
126
        switch (u8INT Num) {
127
         case <u>INTO</u>:
                                S GIFR->sBits.m_INTOF = LBTY SET;
                                                                              break;
                                 S GIFR->sBits.m INT1F = LBTY SET;
128
            case INT1:
                                                                              break;
           case INT2:
                                 S GIFR->sBits.m INT2F = LBTY SET;
129
                                                                              break;
130
            default:
                                break;
131
132 }
```

void INT vidSetSenseControl (u8 u8INT Num, INT tenuSenseControl u8INT SC)

```
84
        switch (u8INT Num) {
                                       S MCUCR->sBits.m_ISC0 = u8INT_SC;
S MCUCR->sBits.m ISC1 = u8INT SC;
85
             case INT\overline{0}:
                                                                                               break;
86
             case INT1:
                                                                                               break;
87
                                       S MCUCSR->sBits.m_ISC2 = u8INT_SC;
             case INT2:
                                                                                               break;
88
             default:
                                      break;
89
90 }
```

Here is the caller graph for this function:



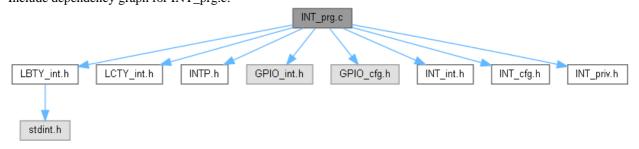
INT_int.h

```
Go to the documentation of this file.1 /*
3 /* ***********
4 /* File Name : INT_int.h
5 /* Author : MAAM
6 /* Version : v01.2
7 /* date : Mar 26, 2023
8 /* *************
11
12 #ifndef INT_INT_H_
13 #define INT INT H
14
16 /* *****
      ************* TYPE_DEF/STRUCT/ENUM SECTION **************** */
18
19 typedef enum {
  \frac{INT0}{INT0} = (\underline{u8}) 0u,
20
21
   INT1,
  INT2
22
23 } INT tenuPin;
24
25 typedef enum{
  \underline{\text{INT Low Level}} = (\underline{u}8)0u,
26
27
   INT Logic Change,
28
   INT Falling Edge,
29
   INT Rising Edge,
30
  <u>INT2 Falling Edge</u> = (\underline{u8}) 0u,
INT2 Rising Edge
31
32
             // Interrupt Sense Control
33 } INT tenuSenseControl;
34
35 /* *****************
37 /*
38
39 /* *****************************
42
46
47 /* **
49
50
56 extern void INT vidInit(u8 u8INT Num);
57
58 /* *****************************
59 /* Description : Set the SenseControl
60 /* Input : u8INT Num, u8INT SC
61 /* Return : void
63 extern void <a href="INT_vidSetSenseControl">INT_vidSetSenseControl</a> (u8 u8INT_Num, <a href="INT_tenuSenseControl">INT_tenuSenseControl</a> u8INT_SC);
64
65 /* *******
66 /* Description : Enable the INT 67 /* Input : USINT_Num 68 /* Return : void
                                       */
70 extern void INT vidEnable(u8 u8INT Num);
```

```
73 /* Description : Disable the INT
74 /* Input : u8INT_Num
75 /* Return : void
76 /* *****************
77 extern void <a href="INT_vidDisable">INT_vidDisable</a> (u8 u8INT_Num);
78
79 /* ************
80 /* Description : Set the INT Flag
81 /* Input : u8INT_Num
82 /* Return : void
83 /* ************
84 extern void INT_vidSetFlag(u8 u8INT_Num);
85
87 /* Description : Reset the INT Flag
88 /* Input : u8INT_Num
89 /* Return : void
90 /* ******************
91 extern void INT vidResetFlag(u8 u8INT_Num);
92
93 /* ************
98 extern void INT vidSetCallBack(u8 u8INT Num, void (*pvidCallback)(void));
99
```

INT_prg.c File Reference

```
#include "LBTY_int.h"
#include "LCTY_int.h"
#include "INTP.h"
#include "GPIO_int.h"
#include "GPIO_cfg.h"
#include "INT_int.h"
#include "INT_cfg.h"
#include "INT_priv.h"
Include dependency graph for INT_prg.c:
```



Functions

- void <u>INT vidInit</u> (<u>u8</u> u8INT_Num)
- void INT_vidSetSenseControl (u8 u8INT_Num, INT_tenuSenseControl u8INT_SC)
- void <u>INT vidEnable</u> (<u>u8</u> u8INT_Num)
- void <u>INT_vidDisable</u> (<u>u8</u> u8INT_Num)
- void <u>INT_vidSetFlag</u> (<u>u8</u> u8INT_Num)
- void <u>INT_vidResetFlag</u> (<u>u8</u> u8INT_Num)
- void INT_vidSetCallBack (u8 u8INT_Num, void(*pvidCallback)(void))
- ISR (EXT_INT0_vect)
- <u>ISR</u> (<u>EXT_INT1_vect</u>)
- ISR (EXT_INT2_vect)

Variables

- static void(* INT0_pvidCallback)(void)
- static void(* INT1_pvidCallback)(void)
- static void(* <u>INT2_pvidCallback</u>)(void)

Function Documentation

void INT_vidDisable (u8 u8INT_Num)

```
111
112
         switch(u8INT Num){
113
              case INT\overline{0}:
                                      S GICR->sBits.m INTOE = LBTY RESET;
              case \overline{\text{INT1}}:
                                      S GICR->sBits.m INT1E = LBTY RESET;
114
                                                                                          break;
115
              case INT2:
                                      S GICR->sBits.m INT2E = LBTY RESET;
                                                                                          break;
116
              default:
                                     break;
117
```

void INT_vidEnable (u8 u8INT_Num)

```
102 default: break;
103 }
104 }
```

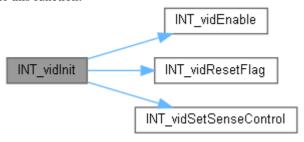
Here is the caller graph for this function:



void INT_vidInit (u8 u8INT_Num)

```
54
        switch (u8INT Num) {
5.5
            case INTO:
56
                 GPIO_u8SetPinDirection(INTO PORT, INTO PIN, PIN_INPUT);
57
                 INT vidSetSenseControl(u8INT Num, INTO SC);
                 INT vidEnable(u8INT Num);
INT vidResetFlag(u8INT Num);
58
59
60
                 break;
             case <u>I</u>NT1:
61
                 GPIO_u8SetPinDirection(INT1 PORT, INT1 PIN, PIN_INPUT);
62
                 INT vidSetSenseControl (u8INT Num, INT1 SC);
INT vidEnable (u8INT Num);
63
64
65
                 INT vidResetFlag(u8INT_Num);
67
            case INT2:
68
                 GPIO u8SetPinDirection(<u>INT2 PORT</u>, <u>INT2 PIN</u>, PIN INPUT);
69
                 INT vidSetSenseControl(u8INT Num, INT2 SC);
70
                 INT vidEnable(u8INT Num);
71
                 INT vidResetFlag(u8INT Num);
72
                 break:
73
            default:
74
                 break;
75
76 }
```

Here is the call graph for this function:



void INT_vidResetFlag (u8 u8INT_Num)

```
switch(u8INT_Num){
140
                                 S GIFR->sBits.m INTOF = LBTY RESET;
141
          case INTO:
                                                                              break;
                                 S GIFR->sBits.m INT1F = LBTY RESET;
142
            case INT1:
                                                                              break;
143
            case INT2:
                                 S GIFR->sBits.m INT2F = LBTY RESET;
                                                                              break;
144
            default:
                                break;
145
146 }
```

Here is the caller graph for this function:



void INT_vidSetCallBack (u8 u8INT_Num, void(*)(void) pvidCallback)

```
154
        if(*pvidCallback == LBTY NULL)
                                             return;
155
        switch(u8INT_Num){
156
            case INTO:
                                 INTO pvidCallback = pvidCallback;
157
                                 INT1 pvidCallback = pvidCallback;
            case INT1:
                                                                               break;
                                 INT2 pvidCallback = pvidCallback;
158
            case INT2:
                                                                               break:
159
            default:
                                 break;
160
        }
161 }
```

void INT_vidSetFlag (u8 u8INT_Num)

```
125
126
          switch(u8INT Num){
127
            case <u>INTO</u>:
                                       S GIFR->sBits.m INTOF = LBTY SET;
                                                                                             break;
              case INT1:
                                       S GIFR->sBits.m INT1F = LBTY SET;
S GIFR->sBits.m INT2F = LBTY SET;
128
                                                                                             break;
129
                                                                                             break;
130
              default:
                                       break;
131
```

void INT_vidSetSenseControl (u8 u8INT_Num, INT_tenuSenseControl u8INT_SC)

```
switch(u8INT Num) {
                                       S MCUCR->sBits.m_ISC0 = u8INT_SC;
S MCUCR->sBits.m_ISC1 = u8INT_SC;
         case \frac{INT0}{INT1}:
85
                                                                                                break;
86
                                                                                                break:
                                       S MCUCSR->sBits.m_ISC2 = u8INT_SC;
87
             case INT2:
                                                                                                break;
88
              default:
                                       break;
89
90 }
```

Here is the caller graph for this function:



ISR (EXT_INTO_vect)

ISR (EXT_INT1_vect)

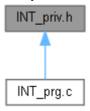
ISR (EXT INT2 vect)

Variable Documentation

```
void(* INT0_pvidCallback) (void) (void)[static]
void(* INT1_pvidCallback) (void) (void)[static]
void(* INT2_pvidCallback) (void) (void)[static]
```

INT_priv.h File Reference

This graph shows which files directly or indirectly include this file:



Data Structures

union MCUCSR_type: Type define of Union bit field of "Control and Status Register"

union MCUCR_type: Type define of Union bit field of "MCU Control Register"

union GIFR_type: Type define of Union bit field of "General INT Flag Register"

union GICR type: Type define of Union bit field of "General INT Control Register"

Macros

- #define <u>S_MCUCSR</u> ((<u>MCUCSR_type</u>* const)0x54U)
- #define MCUCSR (*(volatile <u>u8</u>* const)0x54U)
- #define <u>S_MCUCR</u> ((<u>MCUCR_type</u>* const)0x55U)
- #define MCUCR (*(volatile <u>u8</u>* const)0x55U)
- #define <u>S_GIFR</u> ((<u>GIFR_type</u>* const)0x5AU)
- #define \underline{GIFR} (*(volatile $\underline{u8}$ * const)0x5AU)
- #define <u>S GICR</u> ((<u>GICR type</u>* const)0x5BU)
- #define GICR (*(volatile <u>u8</u>* const)0x5BU)
- #define <u>INTO PORT</u> D
- #define <u>INTO_PIN</u> GPIO_INTO
- #define <u>INTO SC</u> <u>INT Rising Edge</u>
- #define <u>INT1 PORT</u> D
- #define <u>INT1_PIN</u> GPIO_INT1
- #define <u>INT1 SC</u> <u>INT Low Level</u>
- #define INT2 PORT B
- #define <u>INT2 PIN</u> GPIO_INT2
- #define <u>INT2 SC</u> <u>INT2 Falling Edge</u>

Macro Definition Documentation

```
#define GICR (*(volatile u8* const)0x5BU)
#define GIFR (*(volatile <u>u8</u>* const)0x5AU)
#define INT0_PIN GPIO_INT0
#define INT0_PORT D
#define INT0_SC INT Rising Edge
#define INT1_PIN GPIO_INT1
#define INT1_PORT D
#define INT1_SC INT_Low_Level
#define INT2_PIN GPIO_INT2
#define INT2 PORT B
#define INT2_SC INT2_Falling_Edge
#define MCUCR (*(volatile u8* const)0x55U)
#define MCUCSR (*(volatile <u>u8</u>* const)0x54U)
#define S_GICR ((GICR_type* const)0x5BU)
   General Interrupt Control Register
#define S_GIFR ((GIFR_type* const)0x5AU)
   General Interrupt Flag Register
#define S_MCUCR ((MCUCR type* const)0x55U)
   MCU Control Register
#define S_MCUCSR ((MCUCSR_type* const)0x54U)
   MCU Control and Status Register
```

INT_priv.h

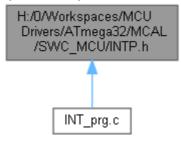
```
Go to the documentation of this file.1 /*
*************
3 /* ***********
4 /* File Name : INT_priv.h
11
12 #ifndef INT_PRIV_H_
13 #define INT PRIV H
14
18
21 typedef union{
 u8 u Reg;
struct {
22
23
24
   ____<u>IO_u8</u>
   <u>IO</u> <u>u8</u> <u>m ISC2</u> : 1; <u>10</u> <u>u8</u> : 1;
25
26 <u>IO</u>
27 }sBits;
28 }MCUCSR type;
29
31
34 typedef union{
  u8 u Reg;
struct {
35
36
37
  38
39 <u>10</u>
}sBits;
42
44
47 typedef union{
  u8 u Reg;
struct {
48
49
  50
51
52
53 <u>IC</u>
54 }sBits;
55 }GIFR type;
56
58
61 typedef union{
62 <u>u8 u Reg;</u>
63 struct {
6.3
   struct {
  ____<u>IO</u> <u>u8</u>
64
   65
66
67 <u>I</u>68 }sBits;
     <u>IO u8 m INT1E: 1;</u>
69 } GICR type;
70
76 #define S_MCUCSR ((MCUCSR_type* const)0x54U)
77 #define MCUCSR (*(volatile u8* const)0x54U)
77 #define MCUCSR
78
          ((MCUCR_type* const)0x55U)
(*(volatile u8* const)0x55U)
80 #define S MCUCR
81 #define MCUCR
82
```

```
84 #define S_GIFR ((GIFR_type* const)0x5AU)
85 #define GIFR (*(volatile u8* const)0x5AU)
86
88 #define S_GICR
         ((GICR_type* const)0x5BU)
89 #define GICR
         (*(volatile u8* const)0x5BU)
90
92
       D
GPIO_INTO
INT_Rising_Edge
93 #define INTO PORT
94 #define INTO_PIN
95 #define INTO_SC
96
        D
GPIO_INT1
97 #define INT1 PORT
98 #define INT1_PIN
99 #define INT1_SC
         INT_Low_Level
100
101 #define INT2_PORT B
102 #define INT2_PIN GPIO_INT2
103 #define INT2_SC INT2_Falling_Edge
104
108
112
116
117
```

main.c File Reference

H:/0/Workspaces/MCU Drivers/ATmega32/MCAL/SWC_MCU/INTP.h File Reference

This graph shows which files directly or indirectly include this file:



Data Structures

union SREG type: Type define of Union bit field of "General INT Control Register"

Macros

```
#define S SREG ((SREG type* const)0x5FU)
#define <u>SREG</u> (*(volatile <u>u8</u>* const)0x5FU)
#define wdr() __asm__ _volatile__ ("wdr")
#define sei() __asm__ _volatile__ ("sei" ::)
#define <u>cli()</u> __asm__ _volatile__ ("cli" ::)
#define reti() __asm__ _volatile__ ("reti" ::)
#define <u>VECTOR(N)</u> _vector_## N
#define ISR BLOCK
#define <a href="ISR_NOBLOCK">ISR_NOBLOCK</a> __attribute__((interrupt))
#define <a href="ISR NAKED">ISR NAKED</a> __attribute__((naked))
#define ISR ALIASOF(v) attribute ((alias( STRINGIFY(v))))
#define ISR(vector, ...)
#define EXT_INTO_vect_VECTOR(1)
                                             /* External Interrupt Request 0 */
#define EXT_INT1_vect _VECTOR(2)
                                             /* External Interrupt Request 1 */
#define EXT_INT2_vect VECTOR(3)
                                             /* External Interrupt Request 2 */
#define <u>TIMER2 COMP vect</u> <u>VECTOR(4)</u>
                                            /* Timer/Counter2 Compare Match */
#define <u>TIMER2_OVF_vect_VECTOR(5)</u>
                                             /* Timer/Counter2 Overflow */
#define TIMER1 CAPT vect VECTOR(6)
                                             /* Timer/Counter1 Capture Event */
#define TIMER1_COMPA_vect _VECTOR(7) /* Timer/Counter1 Compare Match A */
#define TIMER1 COMPB vect VECTOR(8) /* Timer/Counter1 Compare Match B */
#define TIMER1_OVF_vect VECTOR(9)
                                             /* Timer/Counter1 Overflow */
#define TIMERO_COMP_vect _VECTOR(10) /* Timer/Counter0 Compare Match */
#define <u>TIMERO OVF vect</u> <u>VECTOR(11)</u>
                                             /* Timer/Counter0 Overflow */
#define SPI_STC_vect _VECTOR(12) /* Serial Transfer Complete */
#define USART RXC vect VECTOR(13)
                                             /* USART, Rx Complete */
#define <u>USART_UDRE_vect_VECTOR(14)</u>
                                            /* USART Data Register Empty */
#define USART_TXC_vect _VECTOR(15)
                                             /* USART, Tx Complete */
#define ADC vect VECTOR(16)
                                     /* ADC Conversion Complete */
#define EE_RDY_vect _VECTOR(17)/* EEPROM Ready */
#define ANA COMP vect VECTOR(18)
                                             /* Analog Comparator */
#define TWI_vect _VECTOR(19)
                                     /* 2-wire Serial Interface */
#define <a href="mailto:SPM_RDY_vect">SPM_RDY_vect</a> _VECTOR(20)
                                             /* Store Program Memory Ready */
```

Functions

• LCTY_INLINE void INTP_vidEnable (void)

#define VECTORS SIZE 84

Macro Definition Documentation

```
#define _VECTOR( N) __vector_ ## N
#define _VECTORS_SIZE 84
#define ADC_vect _VECTOR(16) /* ADC Conversion Complete */
#define ANA_COMP_vect _VECTOR(18) /* Analog Comparator */
#define cli() __asm__ _volatile__ ("cli" ::)
#define EE_RDY_vect _VECTOR(17) /* EEPROM Ready */
#define EXT_INT0_vect _VECTOR(1) /* External Interrupt Request 0 */
   Interrupt Vectors
#define EXT_INT1_vect _VECTOR(2) /* External Interrupt Request 1 */
#define EXT_INT2_vect _VECTOR(3) /* External Interrupt Request 2 */
#define ISR( vector,
                   ...)
                void vector(void) __attribute__((signal)) __VA_ARGS__; \
   Value:
          void vector(void)
#define ISR_ALIASOF( v) __attribute__((alias(__STRINGIFY(v))))
#define ISR_BLOCK
#define ISR_NAKED __attribute__((naked))
#define ISR_NOBLOCK __attribute__((interrupt))
#define reti() __asm__ _volatile__ ("reti" ::)
#define S_SREG ((SREG_type* const)0x5FU)
   Status Register
```

```
#define sei() __asm__ _volatile__ ("sei" ::)
#define SPI_STC_vect _VECTOR(12) /* Serial Transfer Complete */
#define SPM_RDY_vect <u>VECTOR(20)</u>
                                         /* Store Program Memory Ready */
#define SREG (*(volatile <u>u8</u>* const)0x5FU)
#define TIMER0_COMP_vect _VECTOR(10) /* Timer/Counter0 Compare Match */
                                         /* Timer/Counter0 Overflow */
#define TIMER0_OVF_vect _<u>VECTOR(11)</u>
#define TIMER1_CAPT_vect _VECTOR(6)
                                        /* Timer/Counter1 Capture Event */
#define TIMER1_COMPA_vect _VECTOR(7) /* Timer/Counter1 Compare Match A */
#define TIMER1_COMPB_vect _VECTOR(8) /* Timer/Counter1 Compare Match B */
                                         /* Timer/Counter1 Overflow */
#define TIMER1_OVF_vect _VECTOR(9)
#define TIMER2_COMP_vect _VECTOR(4) /* Timer/Counter2 Compare Match */
#define TIMER2_OVF_vect <u>VECTOR(5)</u>
                                         /* Timer/Counter2 Overflow */
#define TWI_vect _VECTOR(19)
                                  /* 2-wire Serial Interface */
#define USART_RXC_vect <u>VECTOR(13)</u>
                                         /* USART, Rx Complete */
#define USART_TXC_vect _VECTOR(15)
                                         /* USART, Tx Complete */
#define USART_UDRE_vect _VECTOR(14) /* USART Data Register Empty */
#define wdr() __asm__ _volatile__ ("wdr")
Function Documentation
```

LCTY INLINE void INTP_vidDisable (void)

LCTY_INLINE void INTP_vidEnable (void)

INTP.h

```
Go to the documentation of this file.1 /*
******************
2 /* ************************* FILE DEFINITION SECTION ************************
3 /* **********
4 /* File Name : INT.h
11
12 #ifndef INTP H
13 #define INTP H
14
18
21 typedef union{
  u8 u Reg;
struct {
22
23
    ____<u>IO_u8_m_C</u>:1;
24
       10 u8 m Z : 1;

10 u8 m N : 1;

10 u8 m V : 1;
25
26
27
       IO <u>u8</u> <u>m S</u> : 1;
IO <u>u8</u> <u>m H</u> : 1;
28
29
     <u>IO u8 m T</u> : 1;
<u>IO u8 m I</u> : 1;
30
31
31 <u>I</u>
32 }sBits;
33 } SREG type;
34
38
40 #define S SREG ((SREG type* const)0x5FU)
41 #define SREG (*(volatile u8* const)0x5FU)
42
44
                           __asm__ __volatile__ ("wdr")
45 # define wdr()
                           asm volatile ("sei"::)
asm volatile ("cli"::)
asm volatile ("reti"::)
46 # define sei()
47 # define cli()
48 # define reti()
49
50 #ifndef _VECTOR
51 #define _VECTOR(N)
                           vector ## N
52 #endif
53
54 #define ISR_BLOCK
                          __attribute__((interrupt))
55 #define ISR NOBLOCK
56 #define ISR NAKED
                           __attribute__((naked))
                            attribute ((alias( STRINGIFY(v))))
57 #define ISR ALIASOF(v)
5.8
59 #define ISR(vector, ...)
  void vector(void) __attribute__((signal)) __VA_ARGS__; \
void vector(void)
60
61
62 /*
63 #define ISR(vector, ...)
void vector(void) __attribute__ ((signal,used,externally_visible)) __VA_ARGS__;\
void vector(void)
66 */
69 /*
70 Address Labels Code
                                   Comments
             jmp RESET ; Reset Handler
jmp EXT_INTO ; IRQO Handler
jmp EXT_INT1 ; IRQ1 Handler
jmp EXT_INT2 ; IRQ2 Handler
jmp TIM2_COMP ; Timer2 Compare Handler
jmp TIM2_OVF ; Timer2 Overflow Handler
          jmp RESET
71 $000
72 $002
73 $004
74 $006
75 $008
76 $00A
```

```
77 $00C
                 jmp TIM1 CAPT
                               ; Timer1 Capture Handler
                             ; Timer1 CompareA Handler
; Timer1 CompareB Handler
; Timer1 Overflow Handler
; Timer0 Compare Handler
; Timer0 Overflow Handler
78 $00E
                 jmp TIM1_COMPA
                 jmp TIM1 COMPB
79 $010
80 $012
                 jmp TIM1 OVF
                 jmp TIMO_COMP
jmp TIMO_OVF
81 $014
82 $016
                               ; SPI Transfer Complete Handler
; USART RX Complete Handler
; UDR Empty Handler
; USART TX Complete Handler
; ADC Conversion Complete Handler
                 jmp SPI STC
83 $018
                 jmp USART RXC
84 $01A
                 jmp USART UDRE
85 $01C
86 $01E
                 jmp USART_TXC
                 87 $020
88 $022
89 $024
90 $026
                 jmp SPM RDY
91 $028
                                ; Store Program Memory Ready Handler
92 ;
93 $02A
          RESET: ldi r16, high (RAMEND) ; Main program start
          out SPH, r16
ldi r16, low (RAMEND)
94 $02B
                                 ; Set Stack Pointer to top of RAM
95 $02C
96 $02D
                 out SPL,r16
                 sei
97 $02E
                                 ; Enable interrupts
98 $02F
                 <instr> xxx
99 .........
101
                             102 #define EXT INTO vect
                            103 #define EXT_INT1_vect
104 #define EXT_INT2_vect
105 #define TIMER2_COMP_vect
106 #define TIMER2 OVF vect
107 #define TIMER1_CAPT_vect
108 #define TIMER1 COMPA vect
109 #define TIMER1_COMPB_vect
110 #define TIMER1_OVF_vect
111 #define TIMERO COMP vect
112 #define TIMERO_OVF_vect
113 #define SPI STC vect
114 #define USART_RXC_vect
115 #define USART_UDRE_vect
116 #define USART_TXC_vect
117 #define ADC vect
118 #define EE RDY vect
119 #define ANA_COMP_vect
120 #define TWI_vect
121 #define SPM_RDY_vect
122
123 #define VECTORS SIZE
124
128
131 /*
132
135 /* ****************
136
137 LCTY INLINE void INTP vidEnable (void) {
138 <u>S_SREG</u>->sBits.m_I = <u>LBTY_SET</u>;
139
      //sei();
140 }
141
142 LCTY INLINE void INTP vidDisable (void) {
143 <u>S SREG</u>->sBits.m I = <u>LBTY RESET</u>;
144
      //cli();
145 }
146
147 #endif /* INTP H */
```