

BSc. (Hons) Computer Systems Engineering

Year 2 Semester 2

IE2044 – System Modelling And Prototyping

Practical Assignment



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Introduction

This project focuses on designing and implementing a 1-digit decimal up counter (0–9) using D flip-flop ICs following the ripple or asynchronous counter principle. The purpose of this design is to understand digital sequential circuit operation, clock synchronization, and display interfacing through a practical hardware implementation.

The circuit counts from 0 to 9 and then automatically resets back to zero, displaying each number on a seven-segment display. It includes essential control features such as a Manual Reset button to clear the count to zero and a Pause/Resume switch to temporarily halt the counting process. The counting sequence is driven by a 555 Timer-based clock generator, which produces stable timing pulses to advance the counter.

The counter logic is implemented using two 74HC74 D-type flip-flop ICs, forming a 4-bit ripple counter capable of representing binary numbers from 0000 to 1001 (decimal 0–9). The binary outputs are then decoded through a BCD-to-Seven Segment Decoder (SN74LS47N) to drive a common anode seven-segment display.

To ensure reliability and smooth operation, the circuit also includes an automatic reset logic built with NAND gates (74HC00N), which resets the counter automatically after reaching decimal 9 (binary 1001). All parts were designed in EasyEDA, and the full circuit was simulated in Proteus to verify timing accuracy, counting correctness, and display behavior before generating the PCB layout for physical assembly.

This project demonstrates the complete design cycle of a digital prototype from schematic design and simulation to PCB layout and real-world testing bridging theory with practical system modeling and prototyping.

2. Design Methodology

This section explains, step-by-step, how the 0–9 up-counter was designed for PCB implementation in EasyEDA. It follows the same block layout you used in your schematic: Power, Reset (manual + automatic), Pause/Resume clock gating, Clock Generator, 4-bit Ripple Counter, and Output Display Driver. All values, ICs, and signal names match your EasyEDA drawings.

2.1 System Overview

Build a modulo-10 ($0 \rightarrow 9$) ripple counter with push-button Reset and Pause/Resume, and drive a common-anode 7-segment display through a BCD-to-7-segment driver

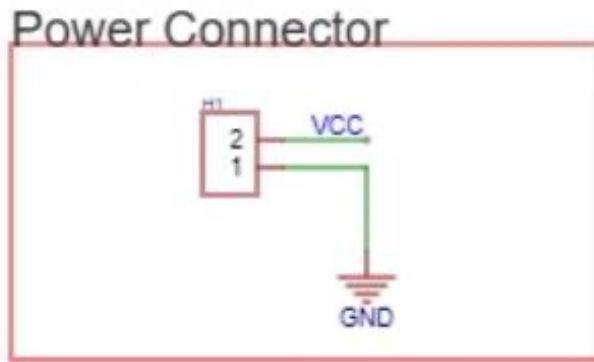
Signal	Source	Purpose
VCC (5 V)	External header H1	Power for all logic ICs and display
GND	External header H1	0 V reference
CLK	555 astable via AND gate (pause)	Primary clock into the counter
CLR	Manual switch + auto-reset (NAND)	Asynchronous clear for all flip-flops
Q1...Q4	Ripple counter (LSB→MSB)	4-bit BCD value to the display driver

2.2 Power Connector & Good-Practice Placement

Stable 5 V rails and clean return paths are critical for reliable digital counting and display brightness.

What we did in EasyEDA

- Added a 2-pin power header (H1): pin-2 = VCC, pin-1 = GND.
- Routed a short, wide 5 V rail to all IC VCC pins.
- Placed 0.1 μ F decoupling capacitors next to each IC's VCC–GND pins (footprints on PCB) to suppress switching noise.
- Kept the GND polygon as a solid plane to minimize loop area.

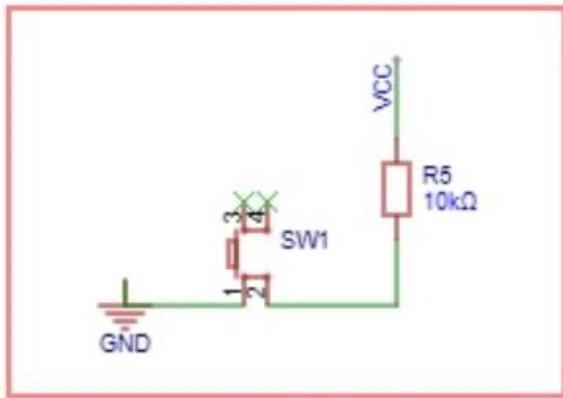


2.3 Reset Network

2.3.1 Manual Reset (push-button, active-low)

- Parts: SW1 (push-button) + R5 = 10 k Ω pull-up to VCC.
- Operation:
 - When idle, R5 keeps CLR = HIGH (no reset).
 - Pressing SW1 pulls CLR LOW → asynchronous clear of all flip-flops to 0000.
- Why active-low: Matches the CLR pins on 74HC74 (active-low asynchronous clear).

Manual Reset Button



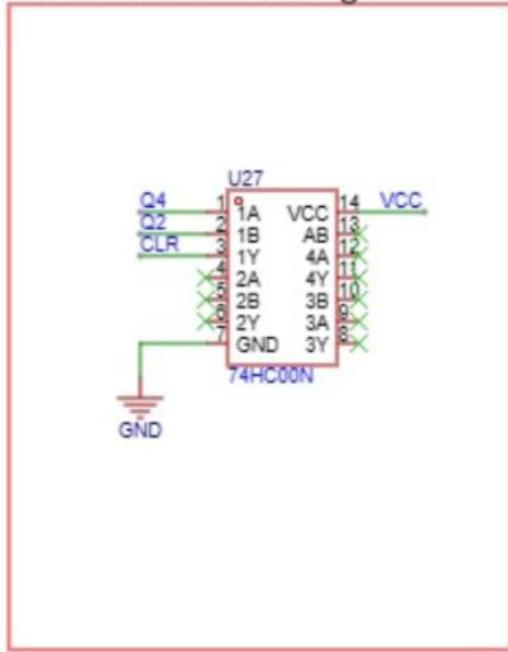
2.3.2 Automatic Reset (force modulo-10)

- IC: 74HC00 (quad NAND).
- Idea: Detect BCD = 1010 (decimal 10) and immediately assert CLR to roll back to 0000, achieving modulo-10.
- Implementation used: feed Q4 (MSB) and Q2 into a NAND stage so that when Q4=1 and Q2=1 (i.e. 1 0 1 0), the NAND output pulses low at the right moment to clear the chain.

This simple logic ensures the counter cycles through $0 \rightarrow 9$ continuously without ever showing 10 on the display.

Q4 (MSB)	Q3	Q2	Q1 (LSB)	Decimal Value	Reset (CLR) Output	Description
0	0	0	0	0	HIGH (inactive)	Counter starts at zero
0	0	0	1	1	HIGH (inactive)	Normal count
0	0	1	0	2	HIGH (inactive)	Normal count
0	0	1	1	3	HIGH (inactive)	Normal count
0	1	0	0	4	HIGH (inactive)	Normal count
0	1	0	1	5	HIGH (inactive)	Normal count
0	1	1	0	6	HIGH (inactive)	Normal count
0	1	1	1	7	HIGH (inactive)	Normal count
1	0	0	0	8	HIGH (inactive)	Normal count
1	0	0	1	9	HIGH (inactive)	Normal count
1	0	1	0	10	LOW (active)	Reset triggered – counter returns to 0000
1	0	1	1	11	-	Never occurs
1	1	0	0	12	-	Never occurs
1	1	0	1	13	-	Never occurs
1	1	1	0	14	-	Never occurs
1	1	1	1	15	-	Never occurs

Automatic Reset Logic



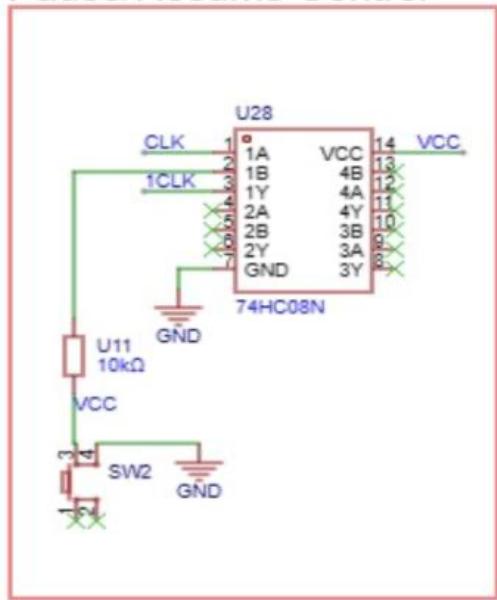
2.4 Pause/Resume Control (Clock Gating)

- IC: 74HC08 (quad AND).
- Control input: a RUN/PAUSE switch (SW2) with a $10\text{ k}\Omega$ bias (U11) to keep logic levels defined.
- Equation: $\text{CLK_OUT} = \text{CLK_555} \text{ AND } \text{RUN}$.
 - $\text{RUN} = 1$: clock passes \rightarrow counter runs.
 - $\text{RUN} = 0$: gated clock = 0 \rightarrow counter pauses without disturbing state.

Why AND-gating?

- It cleanly enables/disables the clock stream without injecting spurious edges into the first flip-flop.

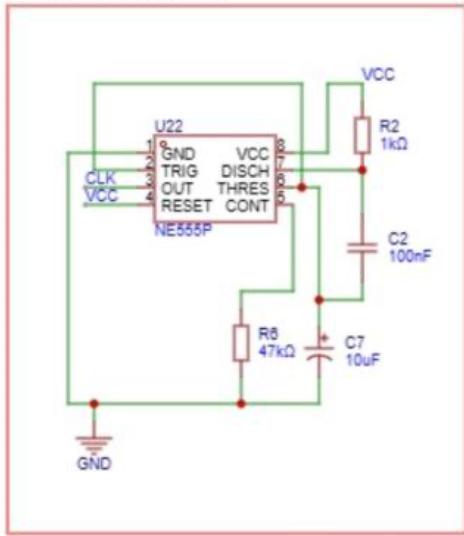
Pause/Resume Control



2.5 Clock Generator (NE555 Astable)

- IC: NE555P in astable mode.
- Values (your schematic): $R_2 = 1 \text{ k}\Omega$, $R_6 = 47 \text{ k}\Omega$, $C_7 = 10 \mu\text{F}$, timing cap $C_2 = 100 \text{ nF}$ for control pin filtering.
- Formulas
 - High time: $T_H = 0.693 (R_1 + R_2) C$
 - Low time: $T_L = 0.693 R_2 C$
 - Frequency: $f = \frac{1}{T_H + T_L} \approx 1.44(R_1 + 2R_2) C$
 $R_1 = 1\text{k}\Omega, R_2 = 47\text{k}\Omega, C = 10\mu\text{F}$
- $T_H \approx 0.333 \text{ s}$
- $T_L \approx 0.326 \text{ s}$
- $f \approx 1.52 \text{ Hz}$

Clock Generator



2.6 4-bit Ripple Counter

- ICs: SN74HC74N × 2 (each has two D flip-flops - total **4 bits**).
- Mode: Convert each D-FF into a T-FF by wiring $D = \bar{Q}$. On every active clock edge, Q toggles.
- Ripple connection:
 - FF1 (LSB, Q1) clocked by gated CLK.
 - FF2 clocked by Q1, FF3 clocked by Q2, FF4 (MSB, Q4) clocked by Q3.
- Asynchronous clear: All CLR# pins are tied to the global CLR from the reset network (manual + automatic).
- Preset pins: Tied HIGH (inactive) for normal operation.

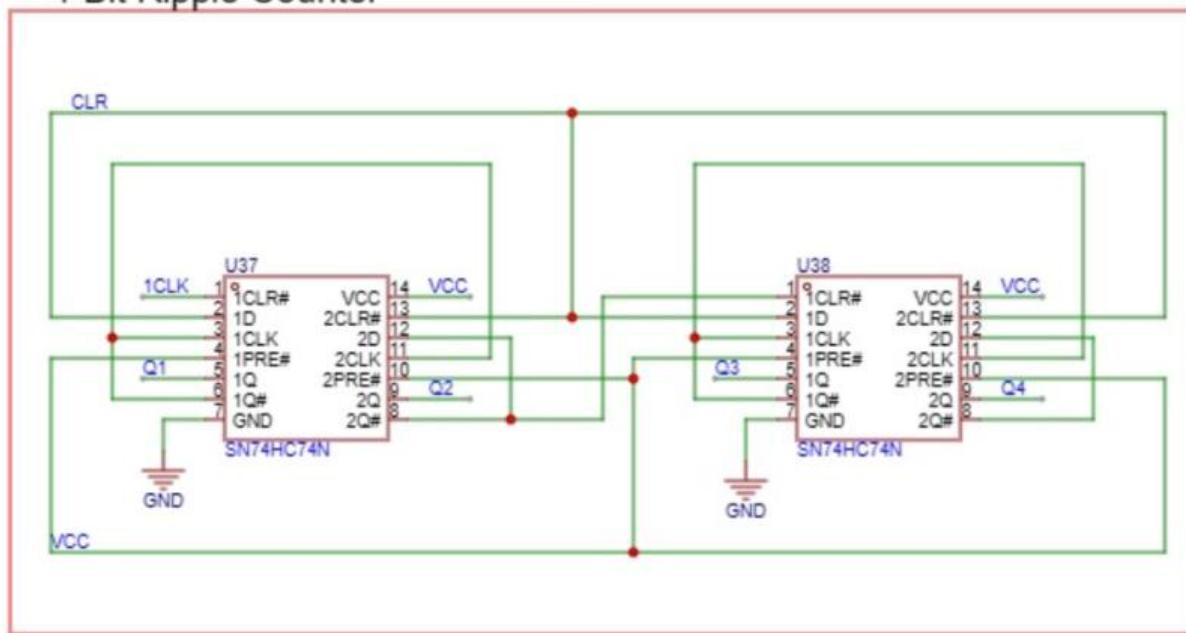
Why ripple?

- Meets module requirement (“asynchronous style”). Simpler wiring, very low part count, and adequate for human-speed clocks.

Pin-planning table

Bit	IC/Section	D wiring	Clock source	CLR#	Q output net
Q1 (LSB)	74HC74 U37-FF1	$D = \bar{Q}$	CLK_OUT	CLR	Q1
Q2	74HC74 U37-FF2	$D = \bar{Q}$	Q1	CLR	Q2
Q3	74HC74 U38-FF1	$D = \bar{Q}$	Q2	CLR	Q3
Q4 (MSB)	74HC74 U38-FF2	$D = \bar{Q}$	Q3	CLR	Q4

4-Bit Ripple Counter

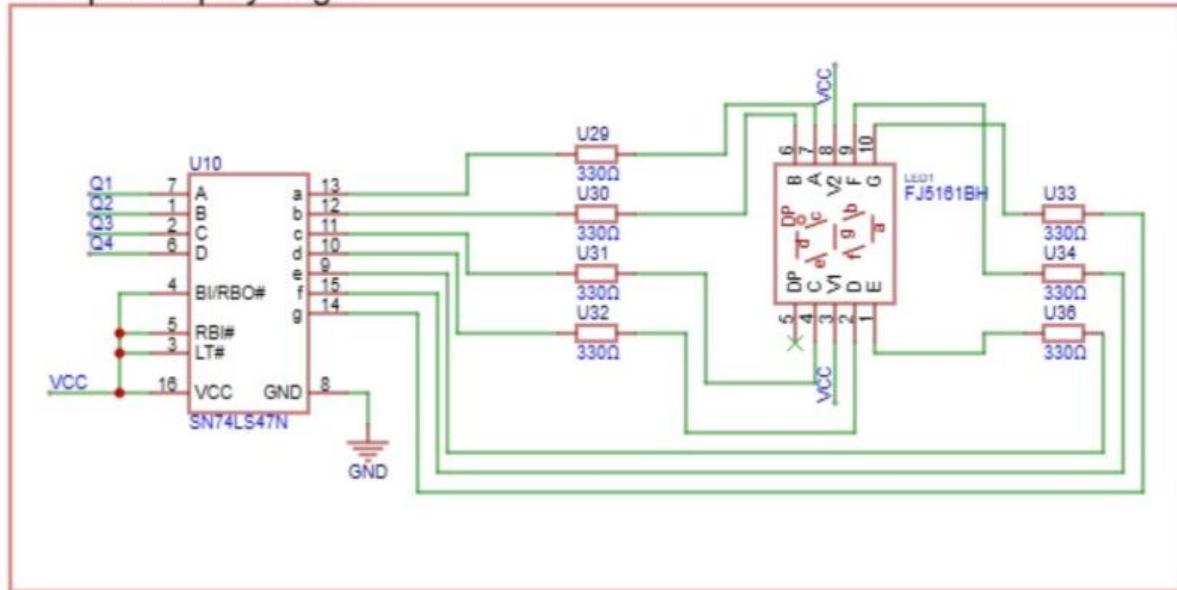


2.7 Output Display Logic (BCD to 7-Segment)

- IC: SN74LS47N (active-LOW outputs for common-anode displays).
- Connections:
 - Inputs A,B,C,D receive Q1 (A/LSB) to Q4 (D/MSB) respectively.
 - LT# (lamp test) and BI/RBO# tied HIGH (disabled) for normal operation; RBI also high.
 - Outputs a–g go through $330\ \Omega$ resistors (R29–R36 in your schematic) to the display pins.
 - The chosen display (FJ5161BH) is common-anode → its COM pins to VCC.

Decimal	Binary (D C B A)	Segments ON	Displayed Digit
0	0000	a b c d e f	0
1	0001	b c	1
2	0010	a b g e d	2
3	0011	a b c d g	3
4	0100	f g b c	4
5	0101	a f g c d	5
6	0110	a f g c d e	6
7	0111	a b c	7
8	1000	a b c d e f g	8
9	1001	a b c d f g	9

Output Display Logic



3. Component Selection

This section explains all the main components used in the EasyEDA circuit and PCB. Each component was carefully selected to meet the functional, electrical, and practical requirements of the assignment.

3.1 Logic ICs

Component	Quantity	Function	Reason for Selection
74HC74 – Dual D Flip-Flop	2	Acts as the 4-bit counter. Each flip-flop toggles its output when $D = \bar{Q}$, forming an asynchronous (ripple) chain.	Required by the assignment to use D flip-flops; 74HC74 provides clean edges, high speed, and operates at 5 V logic level.
74HC00 – Quad 2-Input NAND Gate	1	Forms the automatic reset circuit to detect binary 1010 (= 10) and send a low pulse to CLR.	NAND logic is ideal for easy reset signal generation; single chip gives four gates.
74HC08 – Quad 2-Input AND Gate	1	Implements the Pause/Resume control by gating the 555 clock.	Compact and reliable; CMOS family compatible with other 74HC devices.
74LS47 – BCD to 7-Segment Decoder/Driver	1	Converts the 4-bit counter output (Q_4-Q_1) into signals for the 7-segment display.	Designed specifically for common-anode displays; includes internal current-sink transistors and lamp-test options.

3.2 Timer and Clock Section

Component	Quantity	Function	Reason for Selection
NE555 Timer IC	1	Generates the clock pulses for counting.	Widely used, low-cost, easy frequency adjustment by changing R and C values.
R2 (1 kΩ), R6 (47 kΩ), C7 (10 μF)	1 each	Determine 555 frequency	Produces a comfortable human-visible count rate; components are standard values available in EDA libraries.
C2 (100 nF)	1	Noise-filter capacitor connected to control pin 5 of 555.	Stabilizes output and prevents false triggering.

3.3 Reset and Control Components

Component	Quantity	Function	Reason for Selection
SW1 (Push Button)	1	Manual Reset to clear all flip-flops (CLR = LOW).	Provides immediate reset control for testing or restart.
R5 (10 kΩ Pull-Up)	1	Keeps CLR line HIGH when the button is not pressed.	Prevents floating input and unwanted resets.
SW2 (Toggle Switch)	1	Pause/Resume control.	Lets user stop counting without losing the displayed number.
R11 (10 kΩ)	1	Bias resistor for Pause/Resume input.	Keeps logic level stable when switch is open.

3.4 Display Section

Component	Quantity	Function	Reason for Selection
FJ5161BH 7-Segment Display (Common-Anode)	1	Visually displays digits 0–9.	Bright, through-hole, directly supported by SN74LS47 driver.
R29–R36 (330 Ω)	8	Current-limiting resistors for each display segment.	Maintain safe LED current (~8 mA per segment) and uniform brightness.

3.5 Power and Decoupling

Component	Quantity	Function	Reason for Selection
H1 (2-Pin Header)	1	External 5 V power input (VCC & GND).	Simple, standard connector for breadboard or bench supply.
0.1 μF Ceramic Capacitors	5	One per logic IC, placed between VCC and GND.	Reduce switching noise and ensure stable operation.

4. Results & Testing

The simulation results obtained using Proteus 8 Professional to confirm the functioning of the intended decimal (0–9) up counter circuit are shown in this section. Verifying the accuracy of the seven-segment display output, reset functionality, pause/resume behaviour, and counting sequence accuracy was the aim of this step.

4.1 Configuring the Simulation

Using the same IC models and passive components specified in the EasyEDA schematic, the schematic was replicated in Proteus:

A human-visible counting rate is provided by the Timer IC (NE555) set up in astable mode to produce clock pulses at roughly 1.5 Hz.

The 4-bit asynchronous ripple counter is made up of two 74HC74 D Flip-Flop integrated circuits.

The automatic modulo-10 reset logic is implemented by the 74HC00 NAND gate IC.

Clock gating through the Pause/Resume control is accomplished by the 74HC08 AND gate.

A common-anode 7-segment display is powered by an SN74LS47 BCD to 7-Segment decoder via current-limiting resistors.

For control testing, pushbuttons for manual reset and pause/resume were connected.

A 5 V DC virtual source powered the simulation, and clock and counter outputs were observed using a virtual oscilloscope for validation.

4.2 Functional Testing

Test Case	Action Performed	Expected Outcome	Observed Result
Power ON	Apply 5 V to circuit	Display shows 0	Counter initializes at zero
Automatic Counting	Allow 555 clock to run	Display increments 0→9 cyclically	Observed smooth increment every 0.65 s
Automatic Reset	After reaching '9' (1001)	Counter resets automatically to 0	Works correctly; display rolls over without glitches
Manual Reset	Press Reset button	Counter resets to 0 regardless of current state	Clears all flip-flops; display returns to '0'
Pause/Resume	Toggle pause switch	Counting halts/resumes without errors	No intermediate glitches or false triggers
Display Accuracy	Compare segment patterns with truth table	Correct digits 0–9 displayed	All digits rendered accurately on 7-segment
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Pause/Resume	Toggle pause switch	Counting halts/resumes without errors	No intermediate glitches or false triggers
Display Accuracy	Compare segment patterns with truth table	Correct digits 0–9 displayed	All digits rendered accurately on 7-segment

4.3 Simulation Findings

A ripple delay across each flip-flop output ($Q_1 \rightarrow Q_4$) was verified by the counting waveform, which is in line with asynchronous operation.

When binary 1010 happened, the auto-reset NAND logic generated a brief low pulse, effectively clearing the counter before invalid states manifested.

By employing the 74HC08 AND gate to cleanly gate the clock signal, the Pause/Resume circuit prevented false triggering brought on by switch bounce.

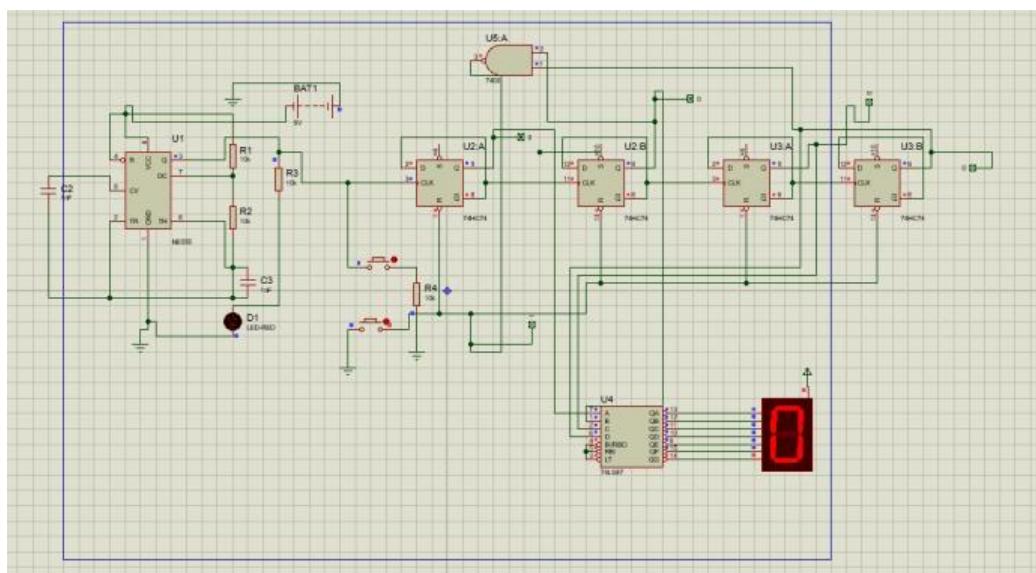
The Manual Reset function showed dependable asynchronous clearing by responding instantly. The 74LS47 driver successfully decoded all seven-segment digits (0–9), and they were all bright.

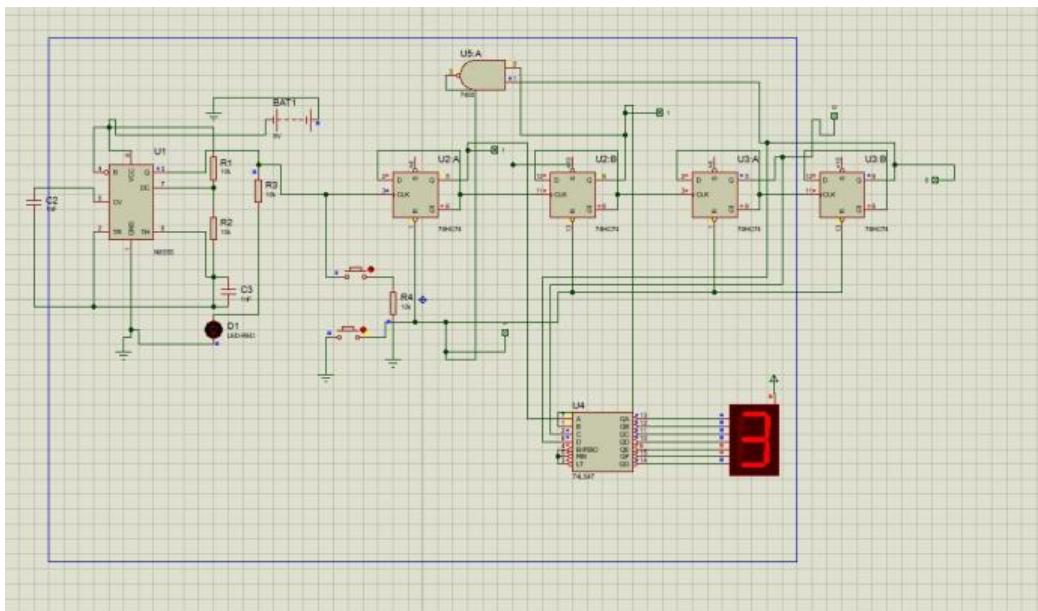
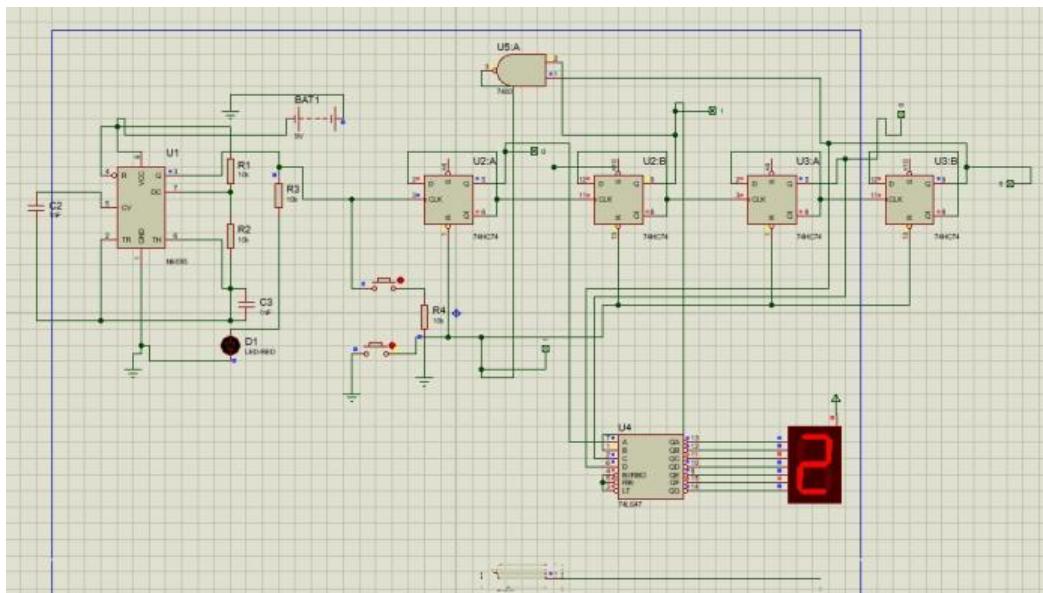
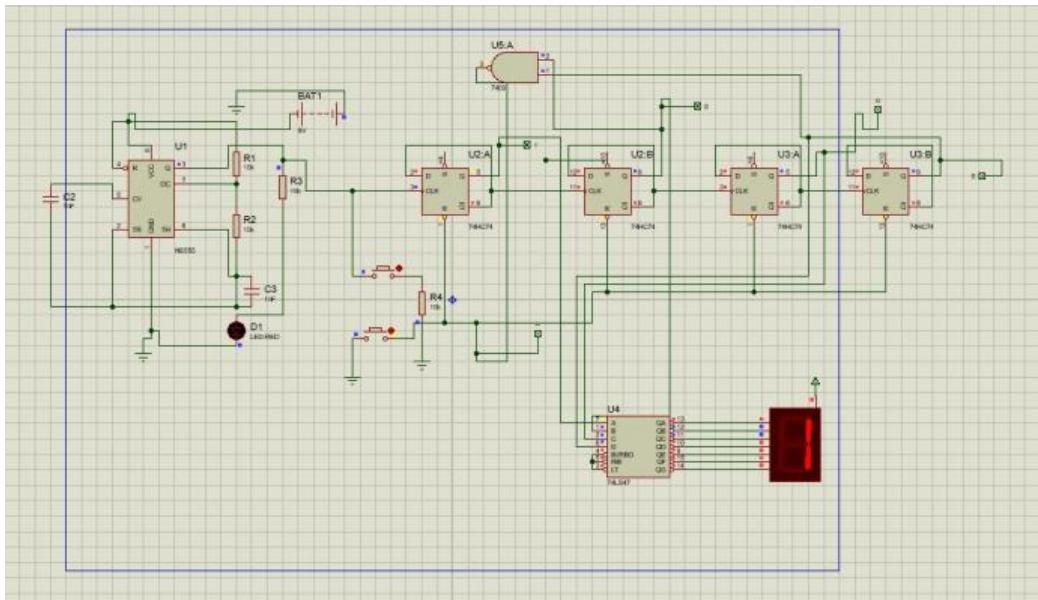
4.4 Verification of the Final Output

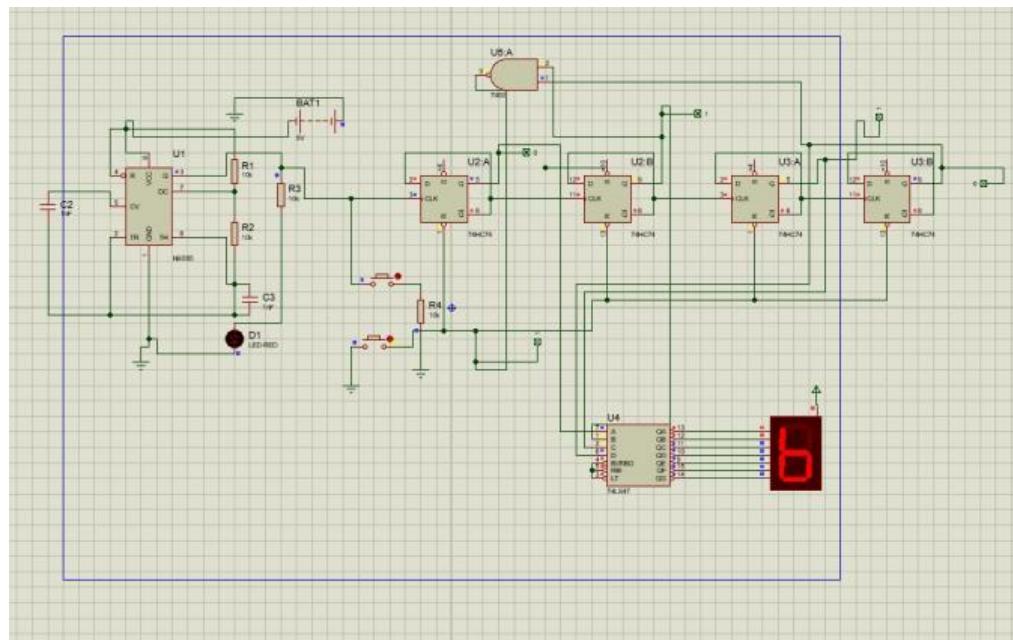
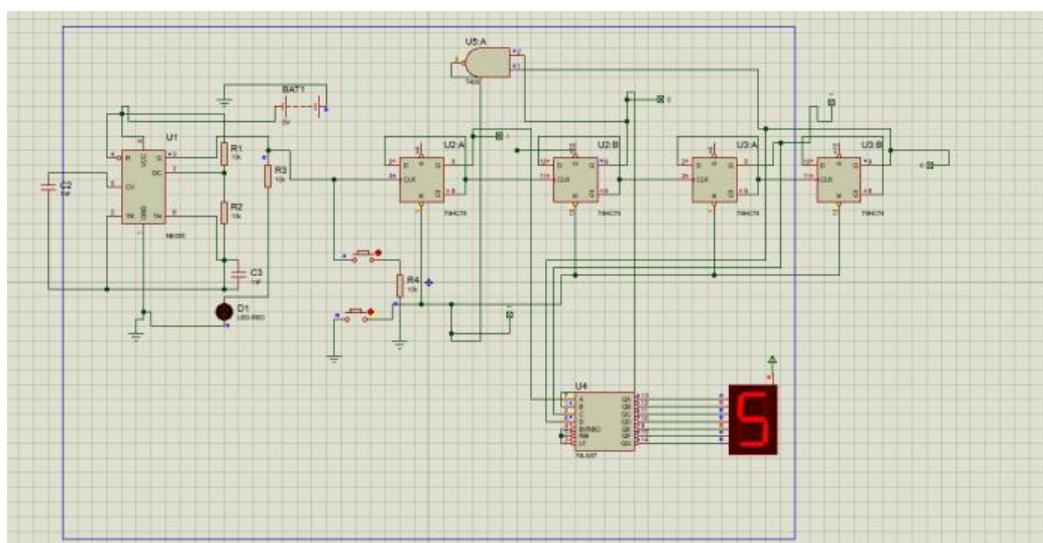
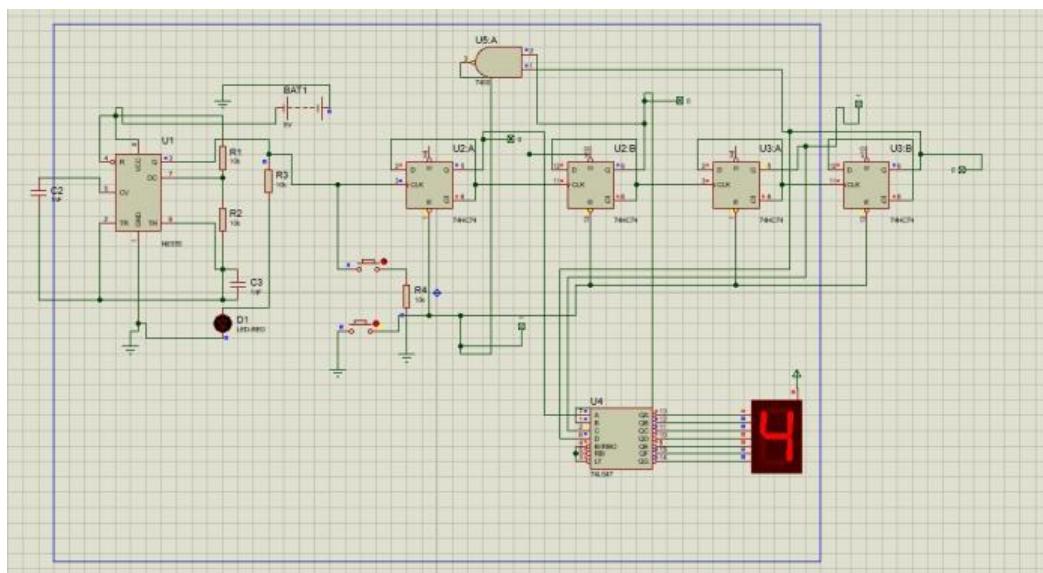
In sync with the 555 timer clock, the seven-segment display repeatedly cycled through the numbers 0 through 9 in the Proteus simulation output.

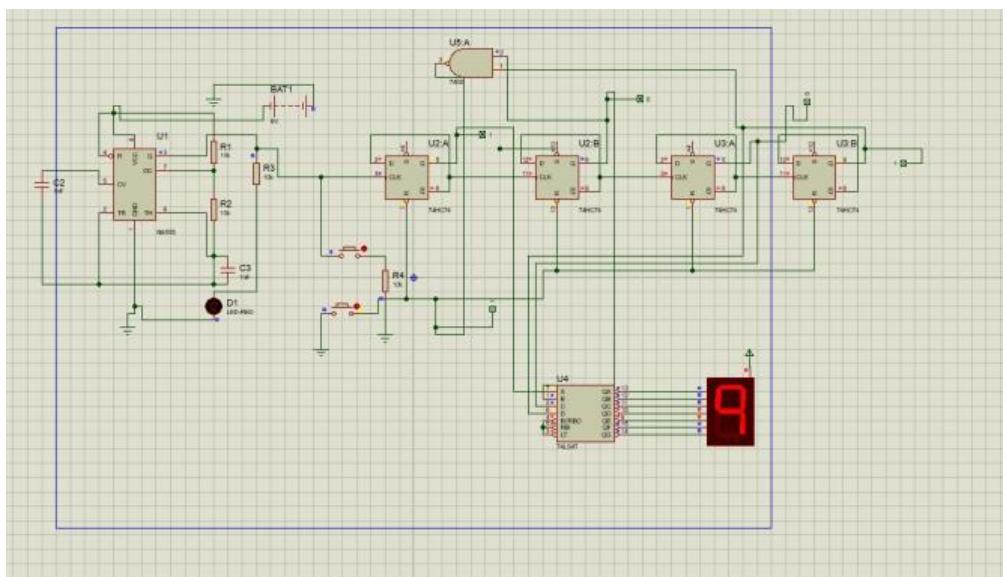
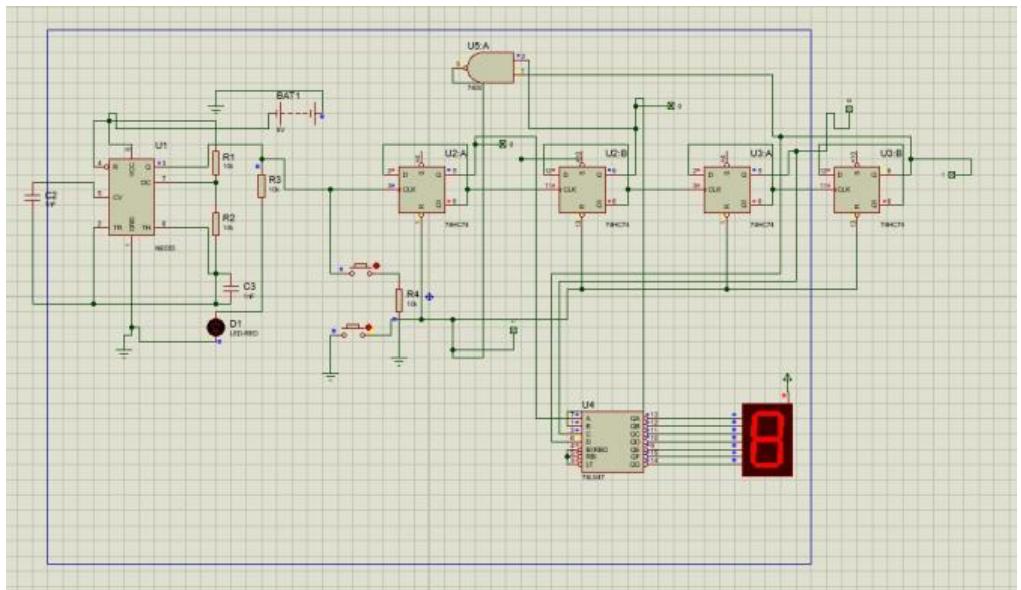
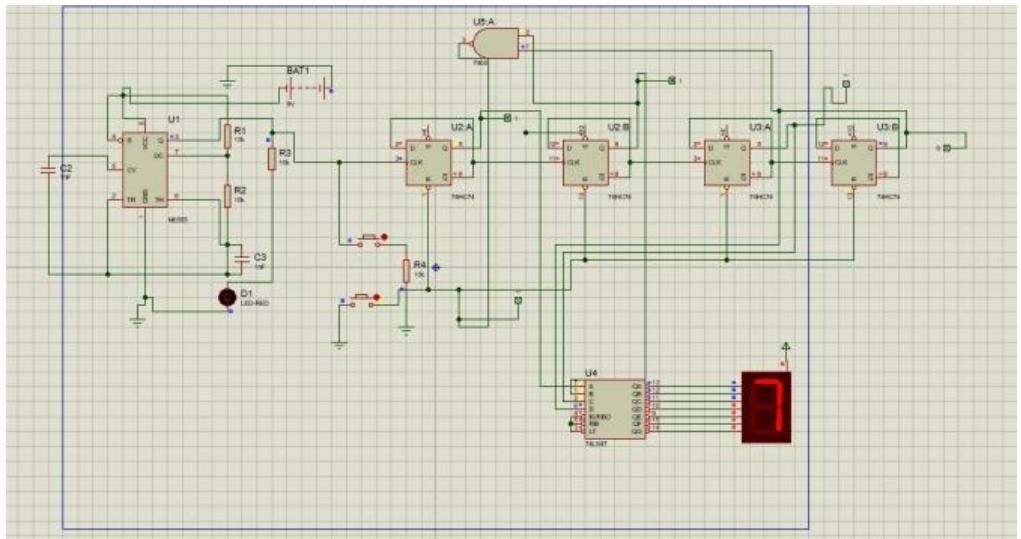
The waveform analysis confirmed that Q_1 toggled at each clock pulse, Q_2 – Q_4 toggled at half the previous bit's frequency, and the reset pulse showed up right after the count hit 9 (binary 1001).

The entire process confirmed that the decoder interface, reset network, and ripple counter all operated as intended and in accordance with theory.



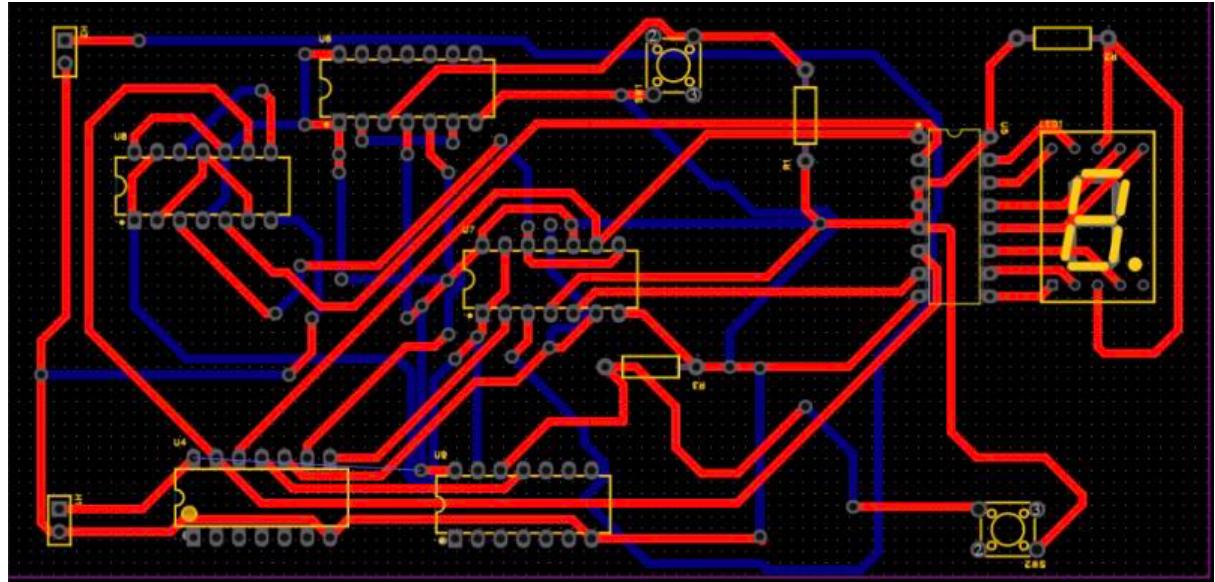






4.5 EasyEDA PCB Design

4.5.1 PCB Layer

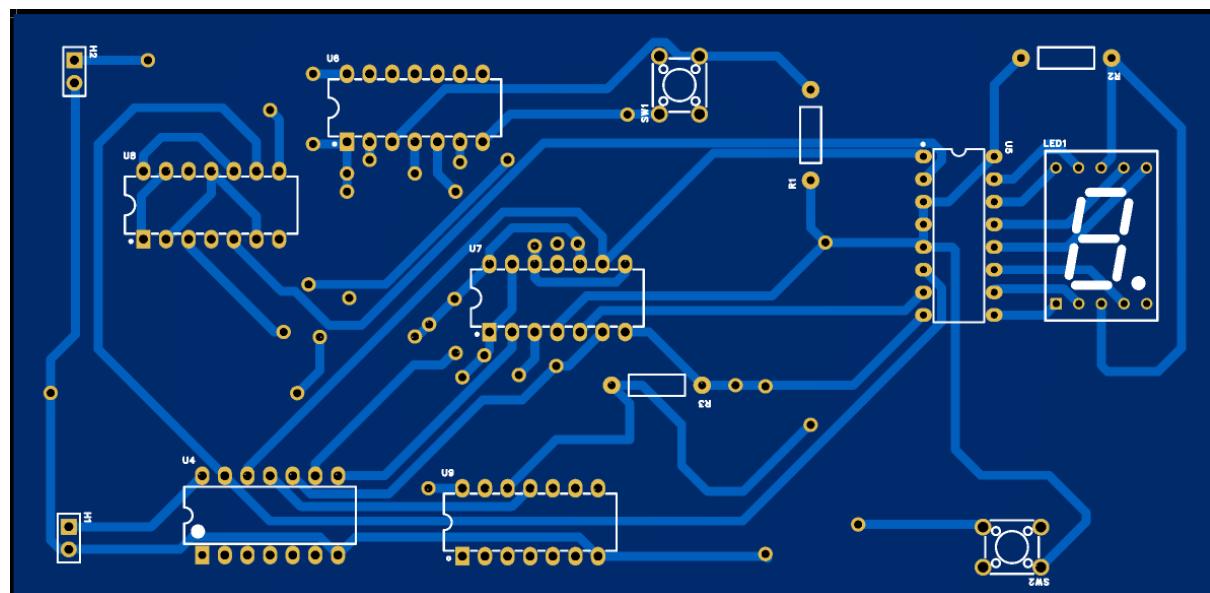


In the PCB layout:

- Red lines represent traces (tracks) on the top layer of the PCB.
- Blue lines represent traces on the bottom layer of the PCB.

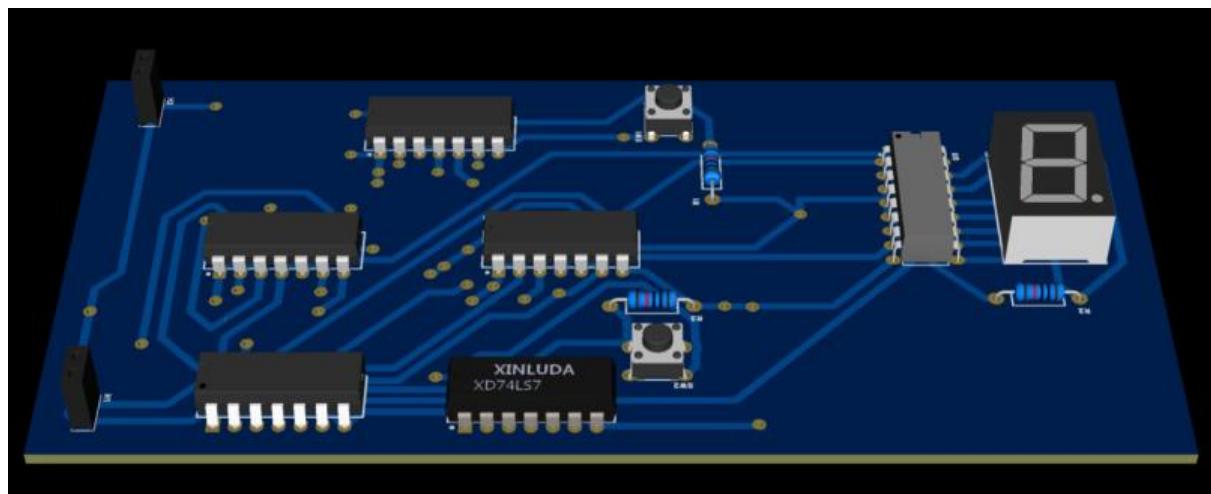
4.5.2 2D PCB Design

2D PCB design shows the electrical connections and physical layout of the circuit on a flat plane before manufacturing.



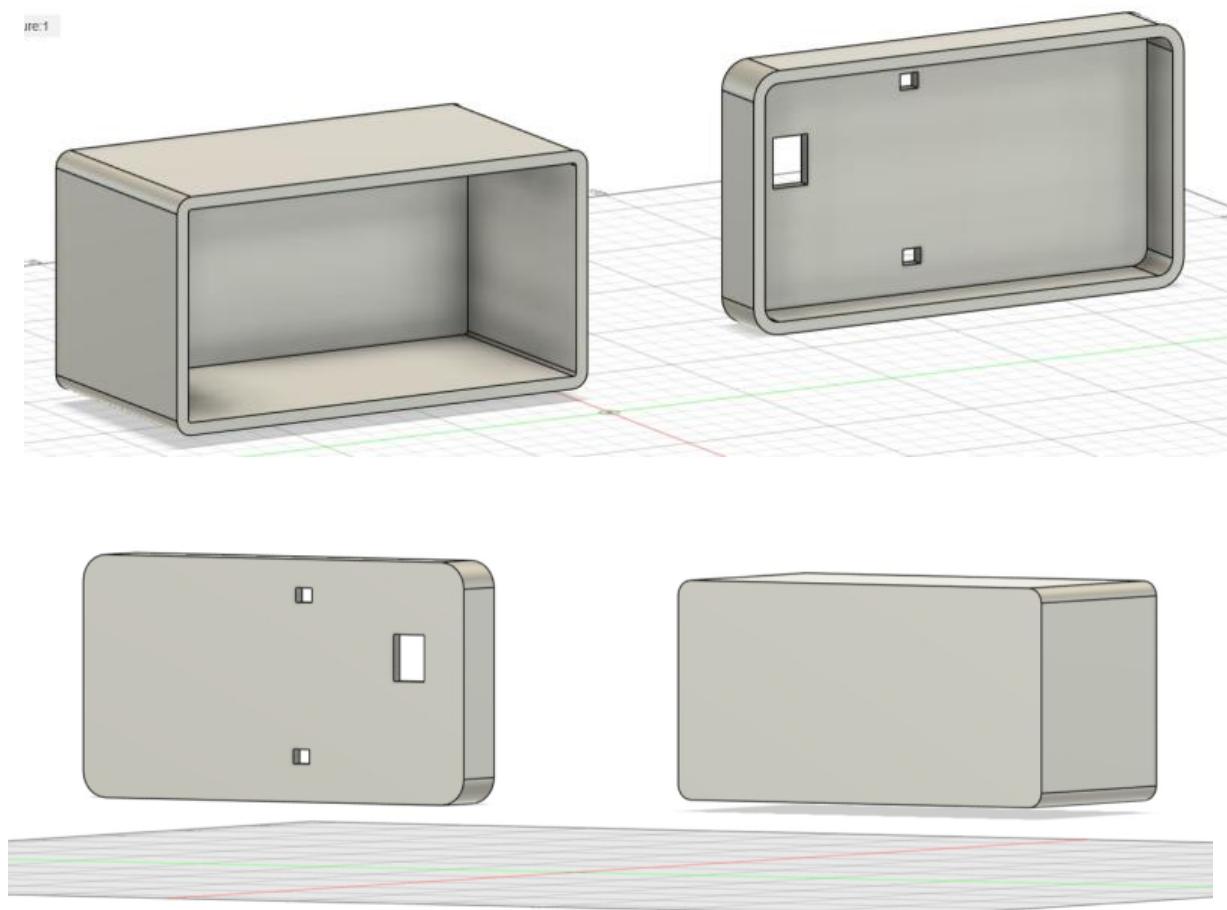
4.5.3 3D PCB Design

The PCB was visualized in 3D to verify component placement, orientation, and spacing, ensuring everything fits correctly before fabrication.



4.5.4 Enclosure Design

It's about designing the physical box or shell that safely holds and supports the electronics.



5. Conversation

The designed one-digit decimal up counter successfully satisfied all functional requirements, as demonstrated by the simulation and testing. Every sub-block of the system operated dependably, confirming the theoretical design and real-world application.

5.1 Timing and Counter Operation

A 4-bit binary sequence from 0000 to 1001 (0–9 decimal) was accurately generated by the 74HC74 D-flip-flops in an asynchronous (ripple) configuration. Proper ripple propagation was confirmed when each subsequent flip-flop toggled at half the frequency of its predecessor. The waveform showed slight propagation delays, which are a feature of asynchronous counters, but these delays were insignificant for human-speed operation powered by the ≈ 1.5 Hz 555 timer clock.

5.2 Modulo-10 Control and Reset

The counter rolled over to 0000 without showing 10 on the 7-segment thanks to the automatic reset logic constructed with a 74HC00 NAND gate, which reliably detected the 1010 state and generated a low-going CLR pulse. For testing and synchronization, the manual reset button offered instantaneous asynchronous clearing. Flexibility and resilience were increased by having both manual and automatic resets available at the same time.

5.3 Pause/Resume Capabilities

The clock signal was cleanly enabled and disabled by clock gating via the 74HC08 AND gate. The display didn't flicker or make any unwelcome changes while the pause was in effect. This demonstrated the efficacy of straightforward logic gating for user control by confirming that the gating technique did not introduce any spurious clock edges or metastability problems.

5.4 Performance of the Display

All BCD outputs were correctly interpreted by the SN74LS47 BCD-to-7-segment decoder, which also showed digits 0–9 with appropriate segment illumination. All of the digits were uniformly bright because segment currents were well-limited by $330\ \Omega$ resistors. During transitions, neither ghosting nor partial segment activation was noticed.

5.5 Integration and System Reliability

Each logic IC had a decoupling capacitor across it to reduce power-rail noise and increase stability. Throughout operation, the 5 V supply stayed constant. There is assurance that the circuit will operate exactly the same when assembled on a PCB because the Proteus simulation verified that all timing and logic interactions worked as anticipated.

5.6 Restrictions and Potential Enhancements

Ripple Delay: For high-frequency applications, a synchronous design could eliminate the inherent slight delays that asynchronous counters have between bit transitions.

Mechanical Bounce: Adding RC debounce filters or Schmitt-trigger inputs could further increase reliability as the push buttons may cause momentary glitches.

Adjustable Clock: By substituting a potentiometer for R6, the counting speed could be changed, increasing the flexibility of the demonstration.

6. Conclusion

This project clearly showed the complete design, simulation, and testing of a 1-digit decimal up counter (0 to 9) using D-type flip-flop ICs based on the ripple (asynchronous) counter principle. The circuit achieved precise decimal counting, automatically reset after reaching nine, and displayed digits smoothly on a common-anode seven-segment display.

In the simulation with Proteus, the counter functioned as expected. It cycled through digits 0 to 9 at a steady frequency generated by the NE555 timer. Adding pause/resume and manual reset controls provided flexibility and allowed full testing of asynchronous clear and clock-gating functions. The automatic reset network, using the 74HC00 NAND gate, effectively enforced a modulo-10 count, ensuring no invalid BCD states appeared.

The project gave hands-on experience in designing and integrating several key digital-system subsystems, including timing generation, sequential logic, display decoding, and user controls, into a single functioning model. The PCB layout in EasyEDA reinforced good design practices such as power-rail decoupling, signal routing, and layout optimization.

Overall, the assignment improved understanding of digital circuit design, system modeling, and prototyping. It connected theoretical logic design concepts to real-world hardware implementation. The final design is strong, efficient, and educationally valuable, meeting all functional and technical requirements specified in the IE2044 System Modeling and Prototyping module.

7. References

1. T. L. Floyd, Digital Fundamentals, 11th ed., Pearson Education, 2015.
2. Texas Instruments, “74HC74 Dual D-type Flip-Flop Datasheet,” Texas Instruments, 2023. [Online]. Available: <https://www.ti.com/lit/ds/symlink/sn74hc74.pdf>
3. Texas Instruments, “74LS47 BCD to 7-Segment Decoder/Driver Datasheet,” Texas Instruments, 2023. [Online]. Available: <https://www.ti.com/lit/ds/symlink/sn74ls47.pdf>
4. EasyEDA Documentation, “EasyEDA Online Circuit Design Tool,” 2024. [Online]. Available: <https://docs.easyeda.com/>
5. Electronics Tutorials, “Asynchronous Counters,” Electronics-Tutorials.ws, 2024. [Online]. Available: <https://www.electronics-tutorials.ws/>