Design and Applications for Embedded Networks-on-Chip on FPGAs

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Dear Editor-in-Chief Dr. Montuschi and Guest Editors Dr. DeMara, Dr. Platzner and Dr. Ottavi,

Thank you for considering our submission to the IEEE Transactions on Computers Special Issue on Innovation in Reconfigurable Computing Fabrics: From Devices to Architectures.

As FPGAs grow in size, complexity and capability, they are being used to implement ever-larger and more complex applications. However, the soft buses currently used for the system-level interconnection of these complex applications are not scalable. They suffer from timing closure problems as well as area and power inefficiencies. Soft buses are also a barrier to modular design which is urgently needed in FPGAs.

In our submission we propose augmenting FPGAs with embedded networks-on-chip (NoCs) to implement system-level communication. Our previous work has shown that embedded NoCs can save area and power compared to soft buses, and can run at much higher frequencies. In this work, we take a close look at the semantics of FPGA-style communication using an embedded NoC. We also define and implement the hardware interfaces that connect an embedded NoC to the FPGA fabric and I/Os. We then develop a cycle-accurate hardware-software simulator to be able to simulate FPGA applications with embedded NoCs. We use this simulator to implement four application case studies that highlight the advantages of using an embedded NoC.

This paper architects embedded NoCs on FPGAs, defines the way to use them, and provides case studies to show their merits. We believe that our work is timely and suitable to the special issue on reconfigurable computing since we discuss new FPGA fabric innovations that will lead to easier, more efficient and more modular design on FPGAs. Thank you for taking the time to review our submission.

Sincerely,

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