AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Electrical and Electronic Engineering

Project Report

Project Title: 10T SRAM Circuit's Implementation and Performance Analysis.

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Submitted by:

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Lab Section : A-2

Year : 4th

Semester : 1st

Title of the project:

10T SRAM Circuit's Implementation and Performance Analysis.

Objective:

In this project analyzed 10T cell topologies of SRAM. All the cells have been designed and implemented using Cadence software (crack version). Their respective delays and power consumption have been calculated in GPDK 90 nm technology.

Circuit Diagram:

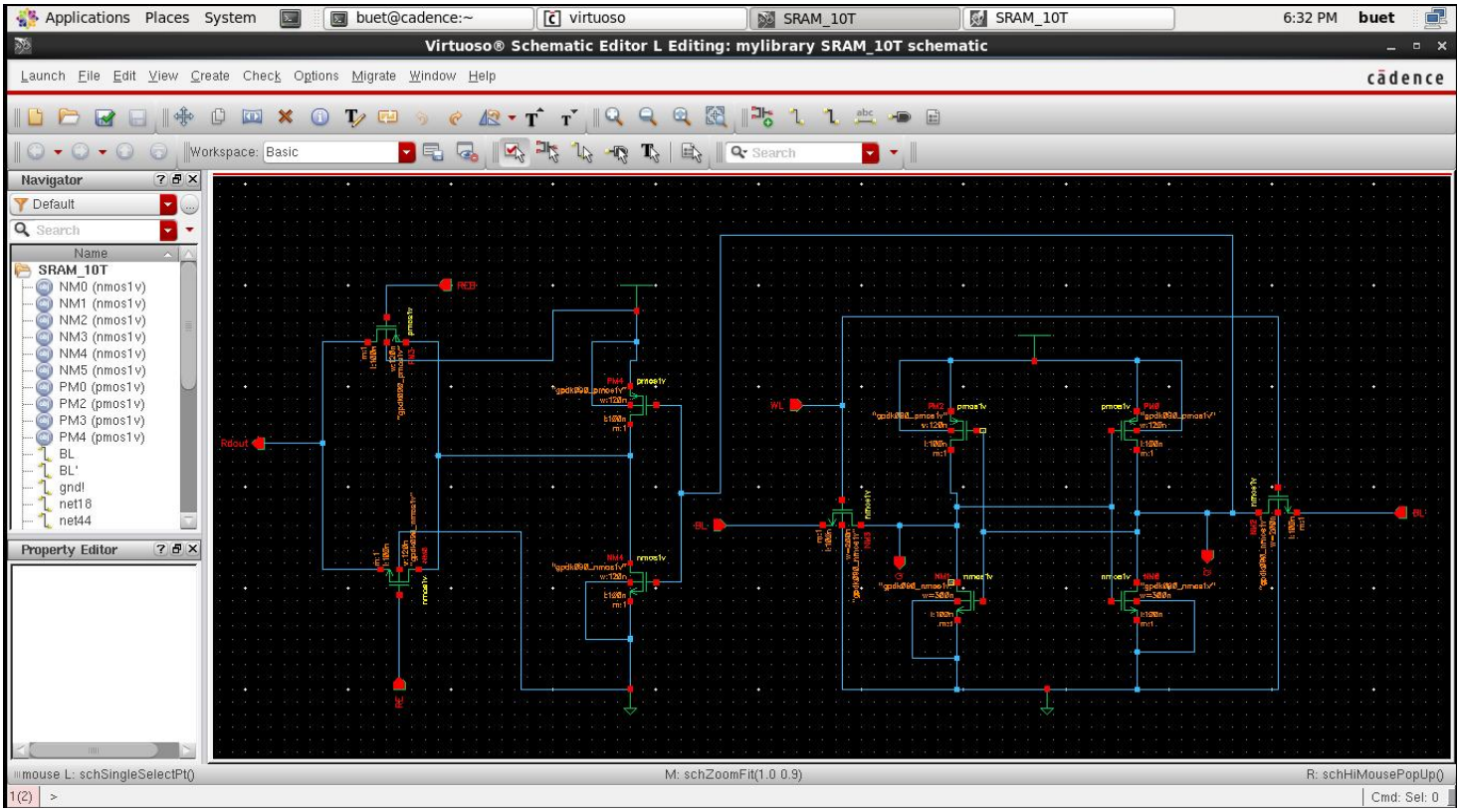


Fig: Circuit Diagram of 10T SRAM

Working Principle:

The 10T SRAM cell has less power and improved data stability. The circuit consists of a memory cell with simple CMOS converters consisting of NMO, NML, NM2, NM3, PMO and PM2. The two write access transistors (NM3 and NM2) are driven by a write signal (WL). Data is stored in this upper memory subcircuit. The subcircuit on the left consists of a conventional converter consisting of PM3, NM4 and a pass-transistor or transmission gate consisting of PM4, NM5.

Write Operation:

During writing the word line (WL) is activated, so the access transistors NM3 and NM2 are conducting. Columns of two-bit lines BL and BL' give complementary values associated with the memory cell composed of simple cross-coupled CMOS converters PM0, NM1 and PM2, NM0. So, the data stored in the memory cell and the data observed by Q & Q'.

Read Operation:

During the write operation, Q' is connected to a conventional inverter consisting of PM3, NM4 and a pass-transistor or pass-gate consisting of PM4, NM5. When Q is '1' and Q' is '0' then PM3 of inverter circuit is on and '1' is passed as input from pass transistors and is read from 'Rdout' while RE is '1' and REB is '0 ' to enable Pass Gate or Transmission Gate. When Q is '0' and Q' is '1' then NM4 is on and '0' is passed as the input of the pass transistors and is read from 'Rdout' while RE is '1' and REB is ' 0' to activate the Pass Gate or the Transmission Gate.

Result:

Truth table:

Operation	WWL	RWL	BL	BLB
Write 1	1	0	1	0
Write 0	1	0	0	1
Read 1	0	1	Discharging	1
Read 0	0	1	1	Discharging
Hold	0	0	1	1

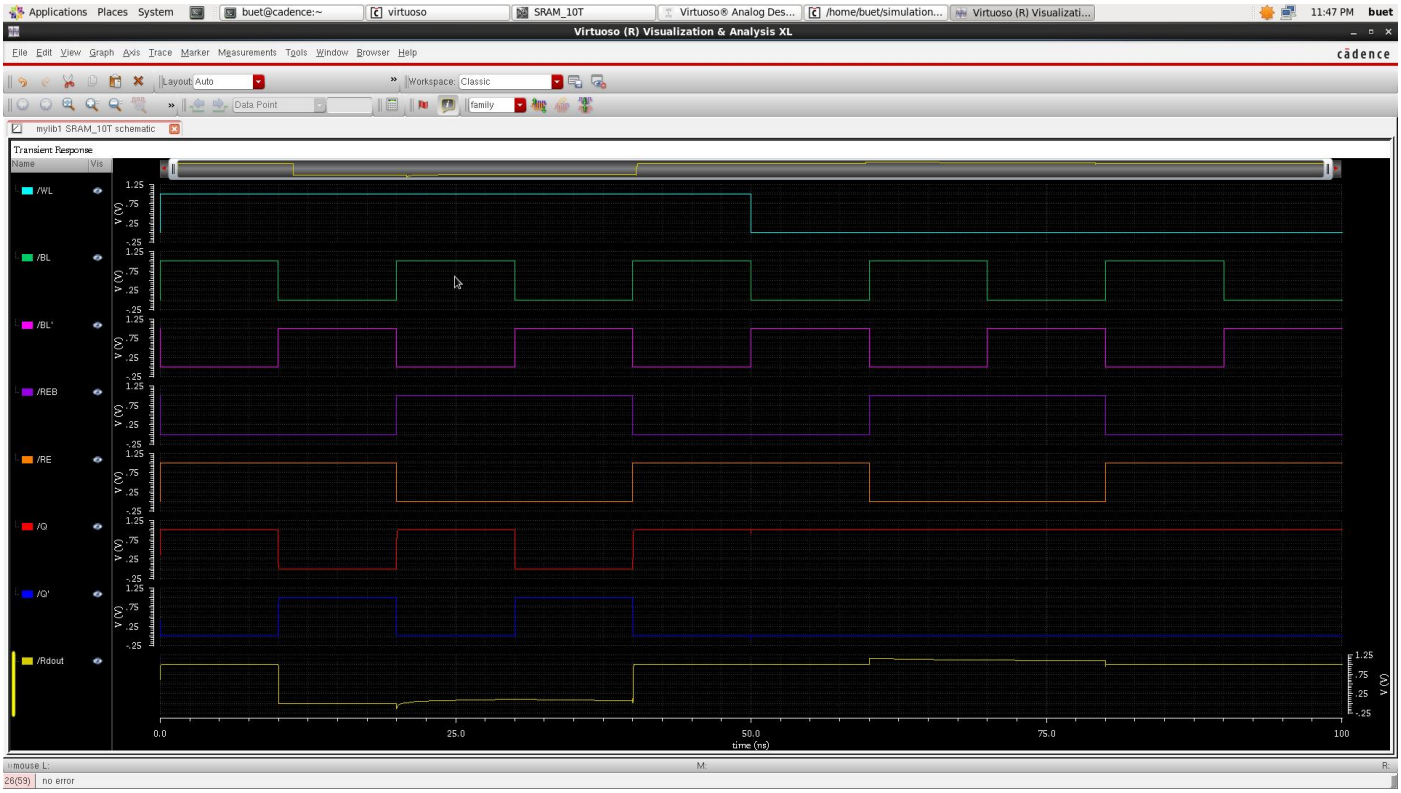


Fig: Input & Output waveform of 10T SRAM

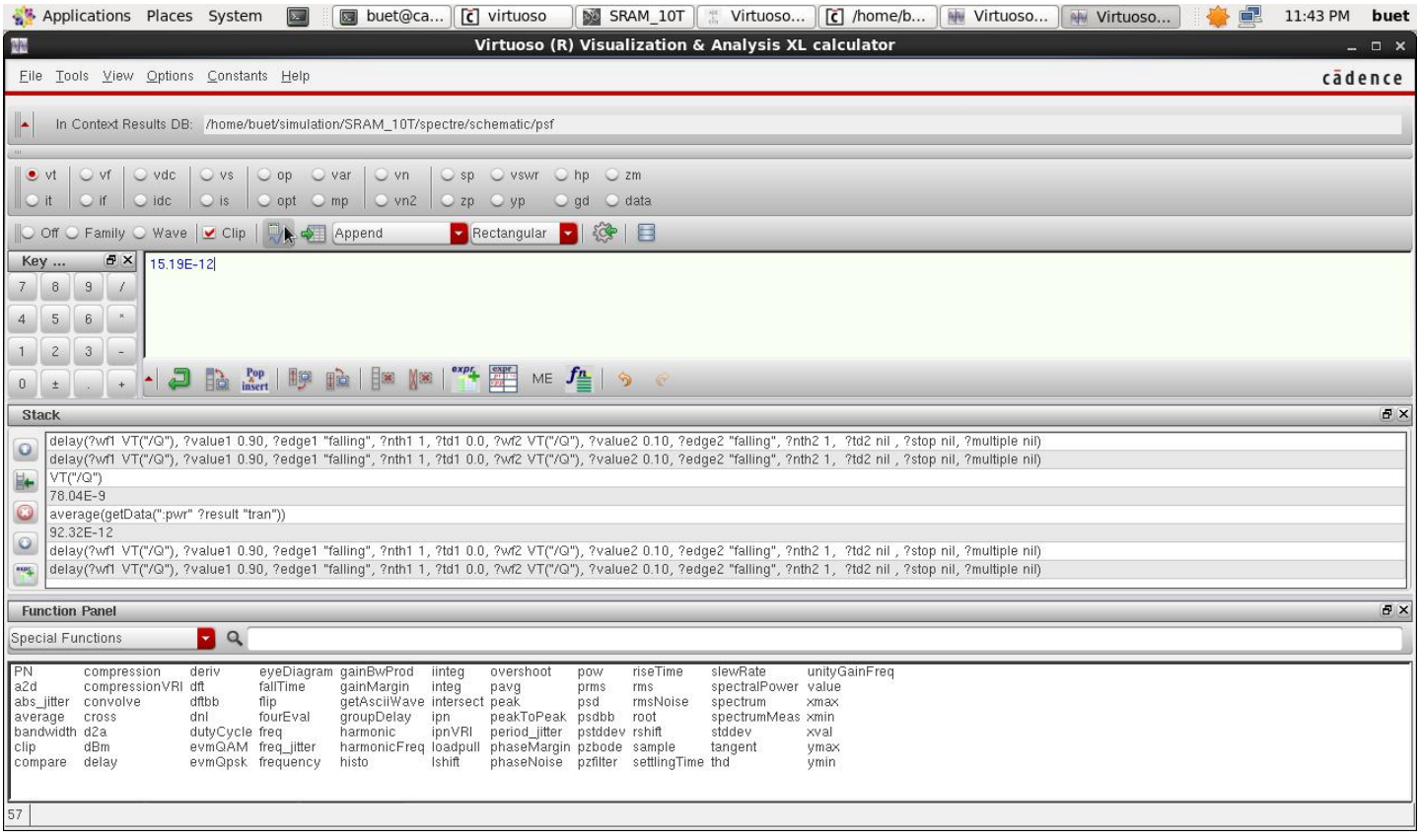


Fig: Propagation Delay of 10T SRAM

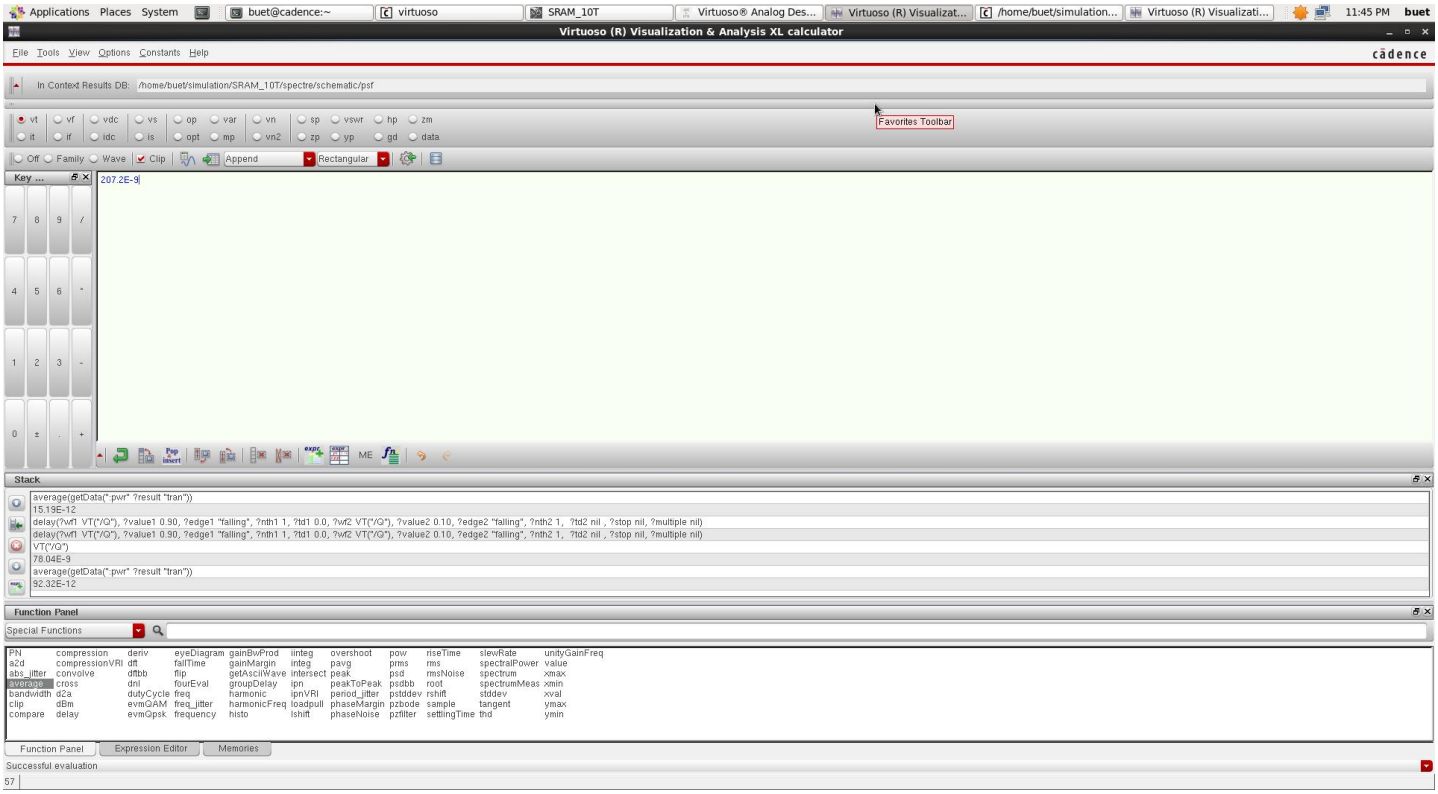


Fig: Average power of 10T SRAM

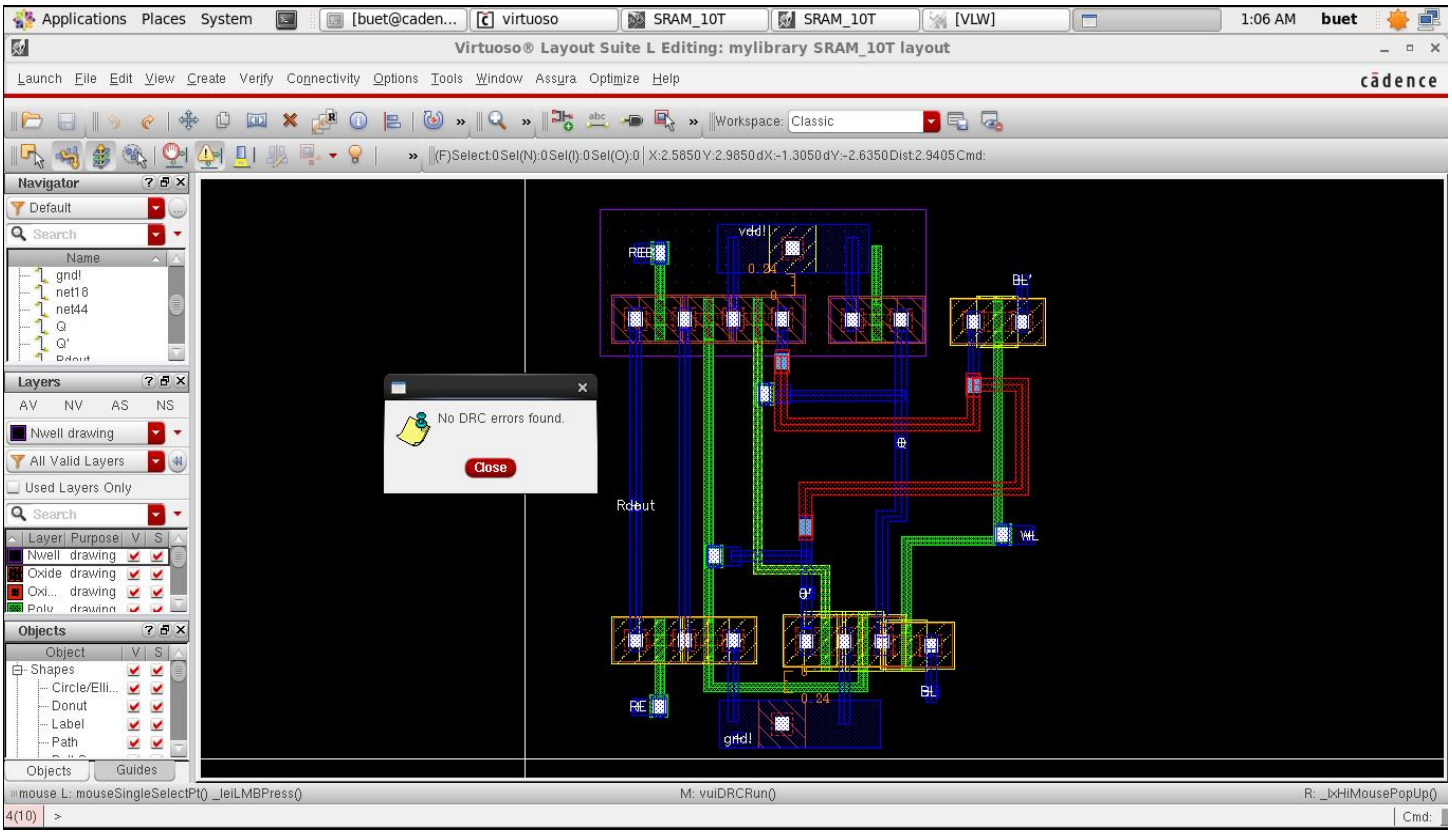
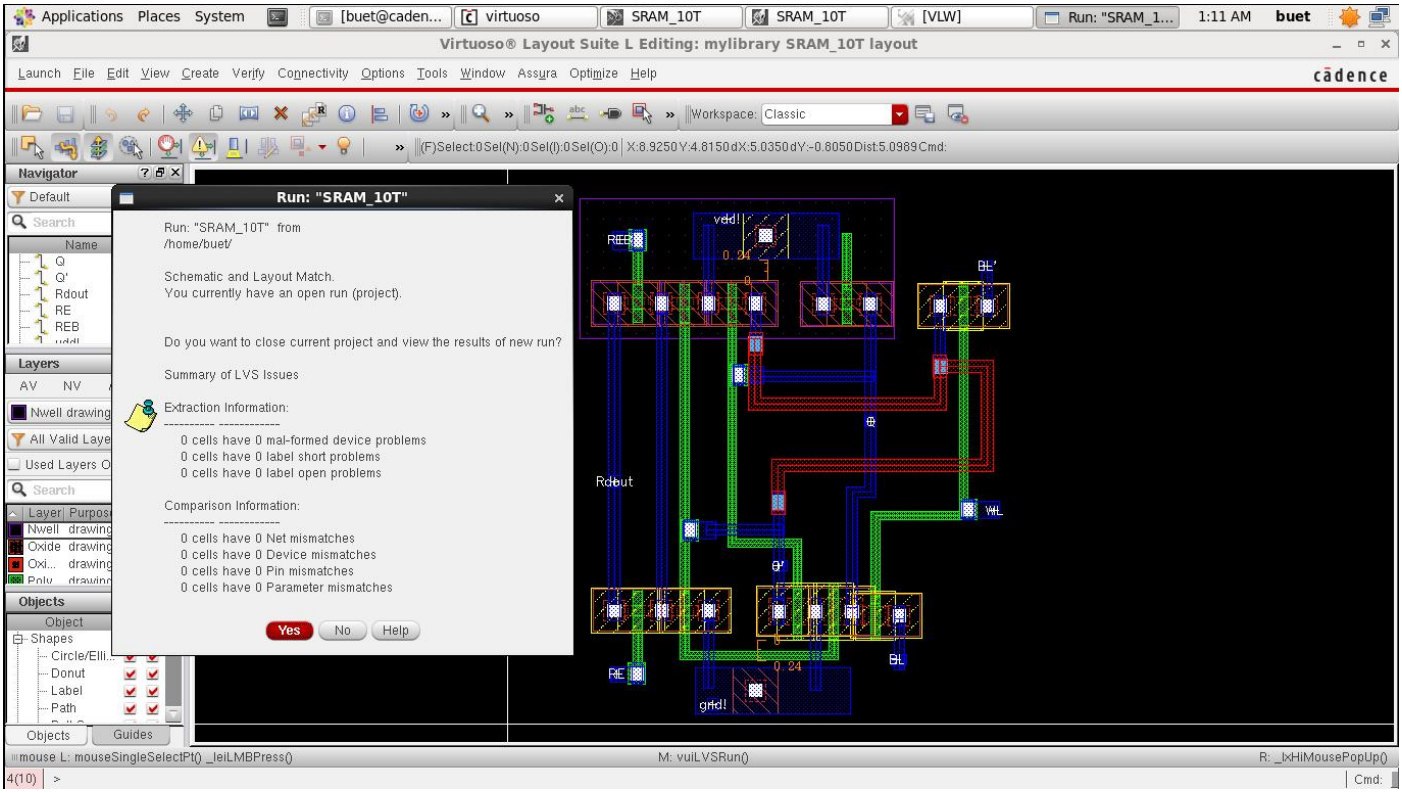


Fig: Layout with no DRC error of 10T SRAM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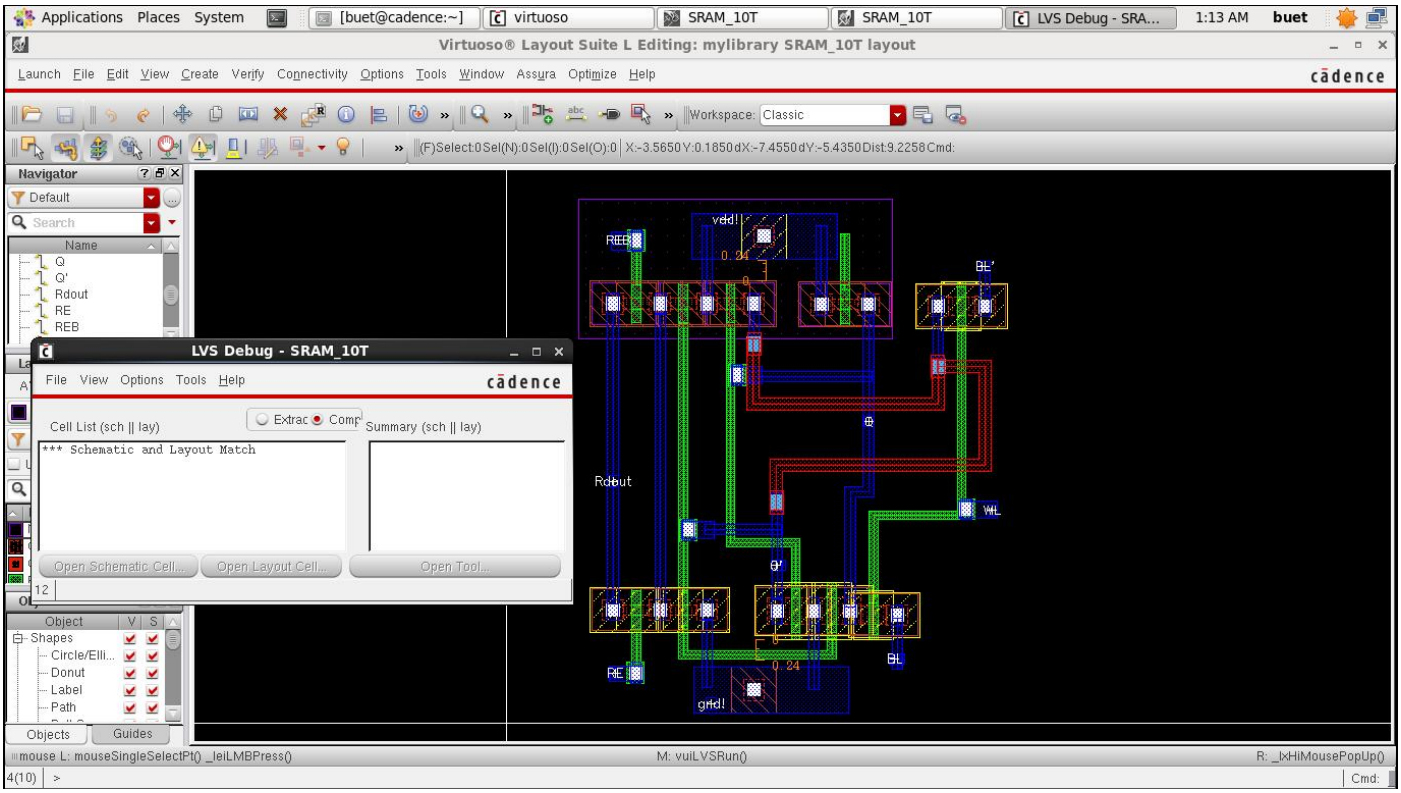
[buet@caden...
virtuoso
SRAM_10T
SRAM_10T
[VLW]
Run: "SRAM_1...
1:11 AM
buet
Virtuoso® Layout Suite L Editing: mylibrary SRAM_10T layout
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize Help
cadence
Workspace: Classic
Navigator
Run: "SRAM_10T"
Run: "SRAM_10T" from
/home/buet/
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
Yes
No
Help
REB
vdd!
BL'
Rdout
WL
Q'
RE
BL
gnd!
0.24


Applications Places System
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Virtuoso® Layout Suite L Editing: mylibrary SRAM_10T layout
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize Help
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File View Options Tools Help
cadence
Cell List (sch || lay)
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Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...
REB
vdd!
BL'
Rdout
WL
Q'
RE
BL
gnd!
0.24

Fig: LVS Run of 10T SRAM

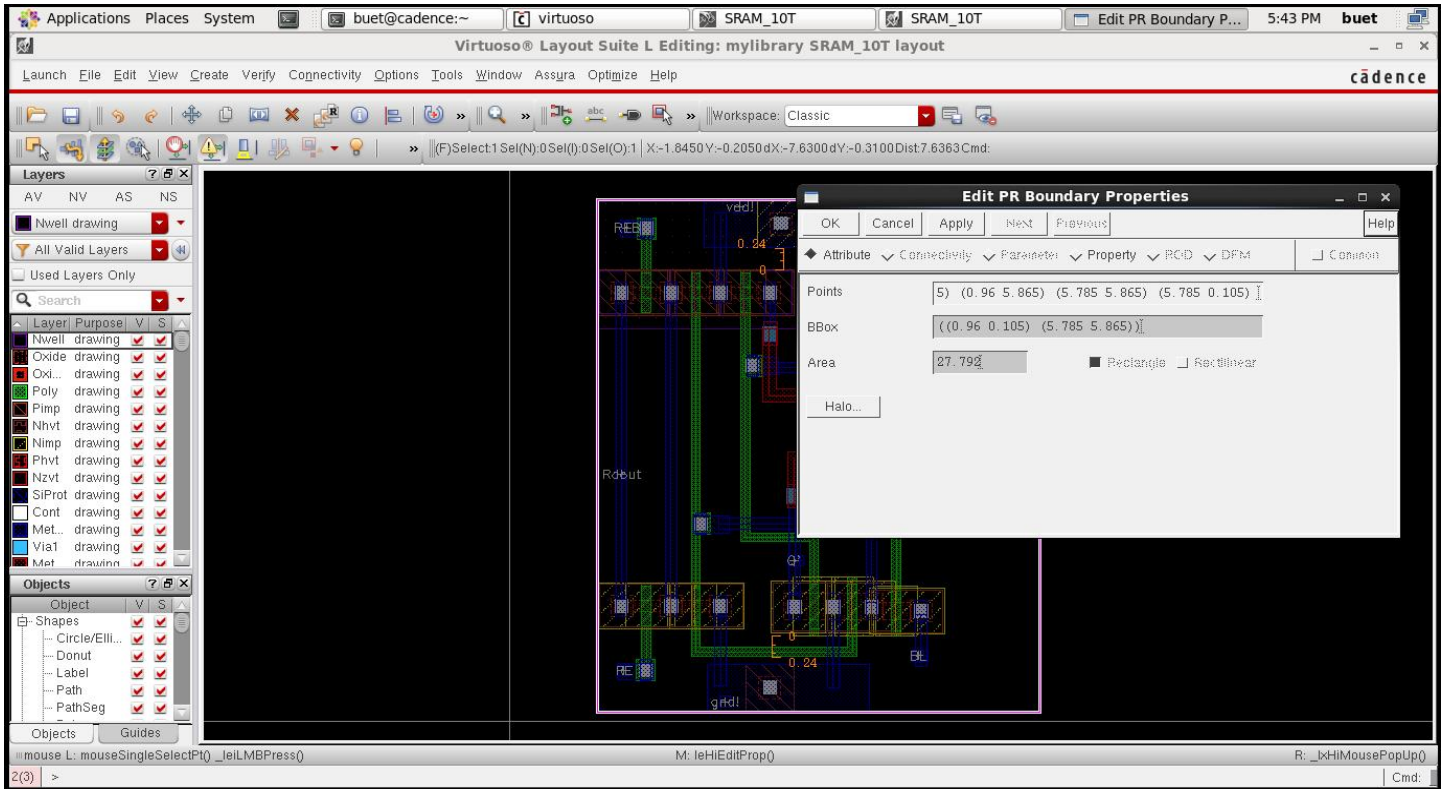

Fig: Layout Area of 10T SRAM

Future Aspects:

The future of 10T-SRAM is looking very exciting, as advancements in technology and research continue to enable better features and capabilities. Many of the features that are expected to become more advanced over time include increased density, improved stability and reliability, faster read and write speeds, and an increased number of systems-on-chip. Additionally, new power management techniques will become available, further increasing the efficiency of 10T-SRAM.

Conclution:

10T-SRAM is a very promising technology, with the potential to significantly improve the performance of systems in a variety of industries. With increased density, improved stability and reliability, faster read and write speeds, and new power management techniques, 10T-SRAM is well-positioned to become a crucial component in the near future.

References:

https://scholar.google.com/scholar?hl=en&as_sdt=0%2C5&q=Parameter+Analysis+of+different+SRAM+Cell+Topologies+and+Design+of+10T+SRAM+Cell+at+45nm+Technology+with+Improved+Read+Speed&btnG=