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# Modeling of KTH UTBSOI MOSFET

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# Modeling of KTH UTBSOI MOSFET

by

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## Abstract

Semiconductor devices such as transistors and integrated circuits are everywhere in our daily lives, it's one of the most important foundations of today's information society. Nanotechnology enables the production of lighter, faster and more efficient components and systems.

Manufacturing technology has improved considerably over the past 40 years, but in recent years, the bulk transistors have reaching the limits of Moore’s law as the size shrinking too few tens of nanometers. The main difficulties are to reduce the power consumption, improve the speed meanwhile maintain the low manufacturing cost.

This has given an opportunity for some emerging semiconductor technologies. One of the most promising approaches is implementation of new device architectures, such as FinFET and UTBSOI.

This bachelor thesis covers the basics of compact modeling of UTBSOI MOSFET, by using the BSIMSOI compact model and SPICE software Cadence to model the KTH Ultra-Thin-Body Silicon-on-Insulator (UTB-SOI) transistor.

The result of this paper shows the accuracy of BSIMSOI and can be used for future extraction work.



## Sammanfattning

Halvledarkomponenter såsom transistorer och integrerade kretsar finns överallt i vår vardag, det är en av de viktigaste grunderna för dagens informationssamhälle. Nanoteknik möjliggör produktion av lättare, snabbare och effektivare komponenter och system.

Tillverkningstekniken har förbättrats avsevärt under de senaste 40 åren, men på de senaste åren har de bulktillverkade transistorerna nått gränserna för Moores lag, när storleken krymper till några tiotal nanometer. De största svårigheterna är att minska energiförbrukningen, förbättra hastigheten samt bevara den låga tillverkningskostnaden.

Detta har gett möjlighet för att utvecklar ny halvledarteknik. En av de mest lovande metoderna är implementering av nya transitor arkitekturer, till exempel FinFET och UTBSOI.

Detta examensarbete omfattar grunderna i modellering av SOIMOSFET, med hjälp av BSIMSOI och SPICE programvara Cadence kan man modellera KTH transistor.

Resultatet av denna studie visar noggrannheten hos BSIMSOI och kan användas för framtida arbete inom ämnet.

## Acknowledgements

First and foremost, I would like to express my deepest gratitude to my thesis supervisor, Docent Per-Erik Hellström, who is a great mentor and provided this thesis opportunity for me. During our meetings, he showed great patience and helped me developed a better understanding of new device structures and compact models.

I am grateful to Professor B Gunnar Malm for his teaching at the semiconductor course IH1611 where I learned the basic knowledge of semiconductor devices and also for serving as the thesis examiner where I got helpful comments on my paper.

I would like to thank KTH Researcher Saul Rodriguez Duenas and PhD student Tingsu Chen for providing assistance of the SPICE tool Cadence Virtuoso. Furthermore, I would also like to thank my thesis opponents Hassan Shafai and Wei Zhao for their valuable comments.

Most importantly, I would like to thank my family for their love, encouragement and support.

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# List of symbols and acronyms

| *Abbrev.* | *Full names* |
|---|---|
| *BOX* | *Buried oxide* |
| *BSIM* | *Berkley short-channel igfet model* |
| *CMOS* | *Complementary metal-oxide-semiconductor* |
| *DG* | *Double gate* |
| *DIBL* | *Drain induced barrier lowering* |
| *DS* | *Dopant segregation* |
| *EOT* | *Equivalent oxide thickness* |
| *FD* | *Fully depleted* |
| *ITRS* | *International Technology Roadmap for Semiconductors* |
| *IV* | *Current Voltage* |
| *MOSFET* | *Metal-oxide-semiconductor field-effect-transistor* |
| *S/D* | *Source/Drain* |
| *SB* | *Schottky barrier* |
| *SCE* | *Short channel effect* |
| *SOI* | *Silicon on insulator* |
| *STL* | *Sidewall transfer lithography* |
| *SPICE* | *Simulation program with integrated circuit emphasis* |
| *UTB* | *Ultra-thin-body* |
| *PD* | *Partial-Depleted* |
| *gm* | *Transconductance* |
| *SOI* | *Silicon on Insulator* |
| *Rds* | *Drain to Source Resistance* |
| *Vdd* | *Power Supply Voltage* |
| *Vth* | *Threshold voltage of Transistor* |

# Chapter 1 Introduction

The development rate of modern electronics has been astonishing ever since the invention of the solid-state transistor in 1947 [1]; Countless applications are made available to the general public. The driving forces behind this rapid progress are the continuous size reduction of the transistor, reduced manufacturing costs and several historical engineering feats: the development of the silicon metal-oxide-semiconductor field-effect-transistor (MOSFET), integrated circuits (IC) and complementary MOSFET (CMOS) circuits. However, the contributions from semiconductor fabrication technologies were equally important and cannot be simply ignored. Without crystal growth, lithography, thin-film deposition, dry reactive ion etching (RIE), ion implantation and so on, the development of modern electronic devices could not have been achievable [2].

The improvement rate of transistor was highlighted by Gordon Moore in 1965, where he observed that the number of transistors on an IC chip doubled every two years [3]. This observation is named “Moore's law” and it has been held true till today; but this law may halt in the future as device scaling become more and more challenging. Fig. 1.1 below illustrates the microprocessor transistor counts from 1970 to 2012 and the continuation of Moore's law.

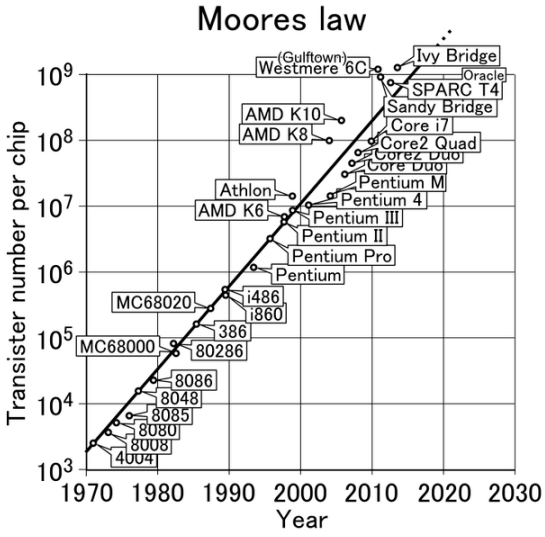


**Figure 1. 1. The transistor counts of microprocessor from 1970 to 2012, from few thousand to billions of transistors. [4]**

## 1.1 Scaling Limits of Planar Bulk-Si Technology

The planar bulk-Si MOSFET has been the workhorse of the semiconductor industry over the last four decades. Higher circuit speed and better power efficiency were achieved by continuously reducing the physical size of Si MOSFETs. In recent years, the scaling of bulk-Si MOSFETs becomes more and more difficult due to a numbers of fundamental physical and manufacturing limits for gate lengths below 20nm [5]. As the gate length ($L_g$) is reduced, the channel potential control from the gate degrades. the potential penetration from drain increase the difficulty for the gate to maintain the electrostatic control over the device, this results in degradation of short-channel effects (SCEs): such as threshold voltage decreases ($V_{th}$ roll-off), subthreshold swing

degradation, drain-induced barrier lowering (DIBL), etc. These problems cause higher OFF-state leakage current which makes the device cannot be turned off easily by lowering the gate voltage ($V_g$). In order to maintain strong gate control of the channel potential, various methods were developed and used, such as thinner gate oxide thickness ($t_{OX}$), shallower source/drain (S/D) junction depth ($x_j$), strained channel, high-κ/metal-gate (HK/MG), etc. Figure 1.2. below shows different improvements introduced at different technological node.

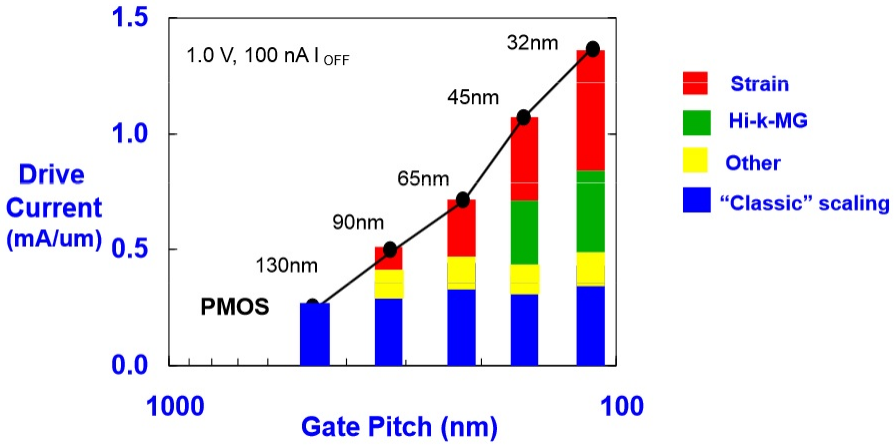


**Figure 1. 2. Different improvements of PMOS. [6]**

High-κ gate dielectric is introduced 45nm node; it's often used to scale down the effective oxide thickness (EOT) without increasing the gate tunneling current. Metal gate electrodes are also used to eliminate the unwanted poly-silicon gate depletion effect. However, these methods are also limited by scaling. Thus, to further maintain the performance improvements by scaling the device dimension, alternative device architectures and new materials has been the subjects of intensive researches around the world.

## 1.2 Advanced MOSFET Structures

Generally, the scale length for conventional bulk device $\lambda_{BULK}$, is indication of the minimum feasible $L_g$ before SCEs becoming excessive. It can be expressed in the following equation [7]:

$$\lambda_{BULK} = 0.1\left(t_{ox}x_j x_{dep}^2\right)^{\frac{1}{3}} \quad \textbf{(1.2.1)}$$

where $t_{ox}$, $X_j$, and $X_{dep}$ are the gate dielectric thickness, source/drain junction depth and channel depletion depth. As transistor dimension shrinking, scaling of $t_{ox}$, $x_j$, and $x_{dep}$ are becoming unfeasible with the conventional fabrication technologies. To circumvent the scaling limits of planar bulk-Si technology, various new MOSFET structures were proposed. The most promising architectures are Ultra-Thin-Body (UTB) Silicon-on-Insulator (SOI) MOSTFET and Multiple-Gate (MG) MOSTFET.

### 1.2.1 Planar Silicon-on-Insulator MOSFETs

Silicon-on-insulator (SOI) is a planar process technology. The essential feature of SOI MOSFETs is that they build on a three layers wafers. Firstly, an insulator layer of silicon dioxide ($SiO_2$) is placed on top of the silicon substrate; the insulator layer is called the buried oxide (BOx). Generally, it's made by oxygen implantation into Si or oxidation of the Si. On top of the buried oxide is a thin surface layer of silicon, this thin film of silicon is often refers as "Si body" or "SOI body". By construction, the buried oxide give SOI MOSFETs various advantages over the conventional bulk-Si counterparts, such as reduced short channel effects, negligible drain-to-substrate capacitance, etc. [8]

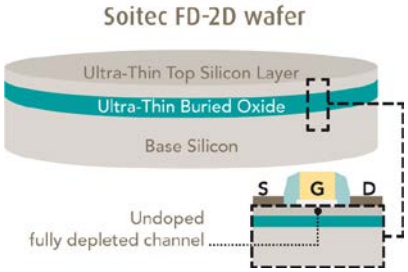


**Figure 1. 3. SOI wafer [9].**

#### 1.2.1.1 Partially-depleted SOI (PD-SOI) and Fully-depleted SOI (FD-SOI) MOSFET

The partially-depleted SOI was the first SOI technology introduced for high performance application because they exhibit significantly reduced source/drain junction capacitance due to layer of the buried oxide (BOX) [10]. This result in increased circuit operating speed compared to conventional bulk-Si MOSFETs. PD-SOI MOSFETs also suffer from "floating-body" effect due to a portion of body is un-depleted and neutral: if the neutral body is not voltage biased when the transistor is in ON-state, then the neutral body will store charge generated by impact ionization. This result in lowering of the threshold voltage, consequently increase on-state current which is dependent on the transistors operating history. For analog devices, the floating body effect known as the kink effect. Moreover, a PD-SOI MOSFET still requires a heavily doped channel region and halo doping for reduction of DIBL and threshold voltage roll-off. Figure 1.4. below illustrate the difference between bulk and SOI structures.

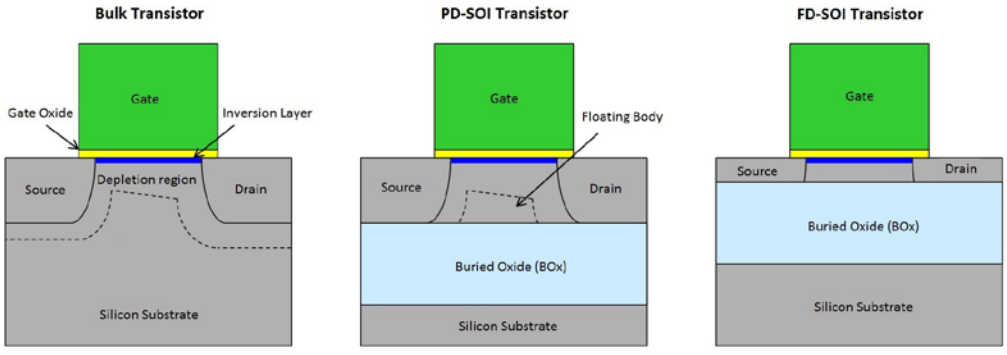


**Figure 1. 4. Comparison between Bulk structure and SOI structures. [11]**

The main feature of an FD-SOI MOSFET is that the depletion region in SOI layer is fully

depleted and reaches all the way down to BOX layer. Therefore, there is no quasi-neutral body and the floating-body effects are negligible. Ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs is a variant of FD-SOI where the SOI layer is extremely thin, unusually several nanometers. The thinner SOI layer eliminates the sub-surface leakage paths, thus SCEs can be significantly suppressed. Moreover, the need for channel doping is lowered, this result in minimization of random dopant fluctuation effect and thus reduced manufacturing variation. Figure 1.5 a) shows a UTB MOSFET with body-bias capability.

### 1.2.2 Multiple-Gate MOSFETs

Multi-gate device architecture is another solution to the scaling problem, the fundamental concept behind multiple-gate MOSFETs is to increase the electrostatic gate control of channel with help of multiple gates. The main advantage of multi-gate is the improved SCEs. The multiple-gate MOSFETs can be divided into two categories; Independent Multi-Gate (IMG) and Common Multi-Gate (CMG) MOSFETs. The independent gate has separate gates biases, gate work function, dielectric thicknesses, etc. Common multi-gate MOSFET is the opposite of IMG. For CMG MOSFETs, the gate share same properties and biases. One of the best known examples of CMG is the FinFET. It's one of the manufacturable versions of new MOSFET structures, where the fin can be constructed neither on SOI or bulk substrates. Figure 1.5 b) and c) below illustrate double-gate MOSFET (IMG) and FinFET (CMG) structure.

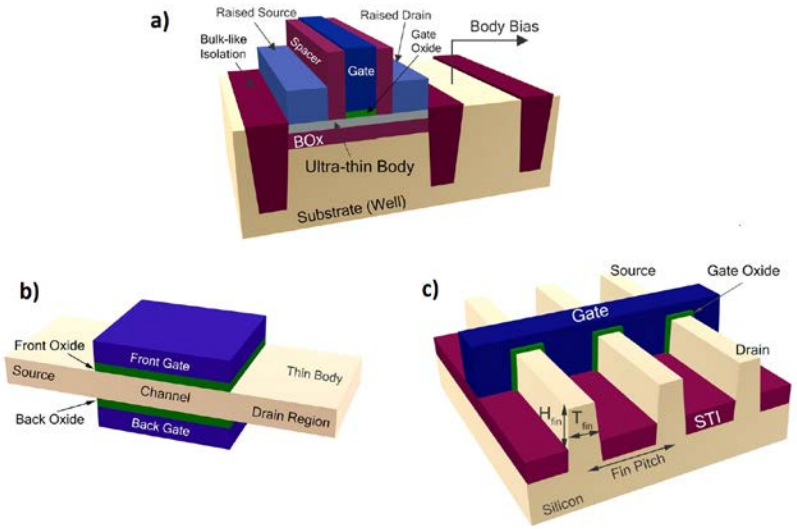


**Figure 1. 5. a) UTB MOSFET, b) double-gate MOSFET and c) Tri-Gate FinFET. [12]**

### 1.2.3 Industry Implementations

In 2012, World's leading integrated circuit (IC) manufacturer Intel started implement FinFET (Tri-Gate) at 22nm node and for their future commercial devices. This event was considered as one of the most dramatic change that has occurred in the IC industry over the past 40 years. The 22nm "Ivy Bridge" processors demonstrated 20-60 percent performance improvement and a reduction of four orders of magnitude in the leakage current compared with the 32-nm planar process [12]. Figure 1.6 below illustrates the structure difference Intel's 32nm planar transistor compared with 22nm FinFET transistors. Nevertheless, FinFET is not the only path ahead; UTB-SOI is also being the subject of intensive research, where monolayer semiconductor such as graphene can be implemented on top of UTB-SOI technology since they naturally form UTB transistors. At present, UTB-SOI transistors are being implemented by ST Microelectronics at 28nm, 20nm and future nodes.

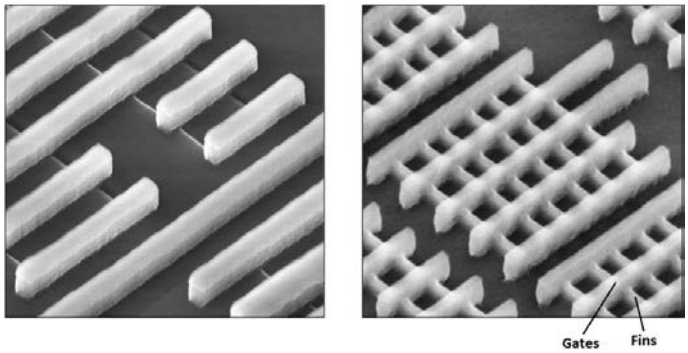


**Figure 1. 6. Intel 32nm planar transistors compared with 22nm Tri-Gate transistors. [11]**

**ITRS (International Technology Roadmap for Semiconductors)** is the roadmap for semiconductors. It's a platform where the industry researchers/companies setting out goals and points out the challenging problems ahead. The ITRS prediction on MPU gate length and compact modeling are shown below in table 1.1

**Table 1. 1. ITRS prediction on MPU (Micro Processing Unit) gate length and Compact modeling of active devices. [13]**

| **ITRS prediction on MPU** | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Year of production | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
| Logic Industry "Node Name" Label | "16/14" | | "10" | | "7" | | "5" | |
| MPU Physical Gate Length (nm) | 20 | 18 | 17 | 15 | 14 | 13 | 12 | 11 |
| **Compact Modeling and Simulation Technology Requirements: Capabilities Near-term Year** | | | | | | | | |
| Year of availability of simulation feature | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
| Active devices | Multi-gate CMOS: Standardize SOI and multi-gate circuit models | | | | Inclusion of influences of variability, reliability and aging | Circuit models for non-Si channels, tunneling, nanowire and compound heterogenous devices | | |

## 1.3 Compact Models for SPICE Simulation

Compact models for a semiconductor device are based on the device physics to describe the device characteristics accurately for all the operation regions, the model equations are long and complex. Furthermore, the accuracy of the models is important thus fitting parameters are introduced. The models are implemented in a computer programming language, such as C or Verilog-A. Some examples of compact models for MOSFET are BSIM, PSP and HiSIM for bulk-Si MOSFETs, HiSIM-HV for high-voltage MOSFETs, BSIM-CMG and BSIM-IMG for common and independent multi-gate MOSFETs, BSIM-SOI and HiSIM-SOI for Silicon-on-Insulator MOSFETs, HICUM and MEXTRAM for Bipolar Transistor [14]. In order to describe the electrostatics and the transport of the channel carriers for an ideal long channel transistor, these compact models consist of a physical core model. They fall under two categories:

- Threshold voltage based model like that in the BSIM3, in this model the $V_{th}$ is unknown for the specific MOSFET. The channel charge is expressed as a function of the terminal voltages and threshold voltage $V_{th}$. Another requirement of threshold voltage based models is the need to bring together the drift and diffusion currents with suitable smoothing functions.
- The MOS11, EKV, PSP and HiSIM models are based on Charge/Surface Potential in the channel. In these models Poisson equation needs to be solved analytically under boundary condition set by the device architecture. Which leads to a implicit equation of the channel charge/surface potential as a function of terminal voltage and other physical device parameters. This implicit equation can be solved by obtain the channel charge/surface potential.

Fig. 1.6 below illustrates the development frame for the BSIM models. Notice the BSIM group support has been discontinued for these the gray named models (BSIM3 and BSIM5). In March 2012, The Compact Model Council (CMC) selected BSIM-CMG as the first and only industry-standard model for the FinFET. BSIM-IMG is now under consideration by CMC as a standard model for UTB-SOI technology.

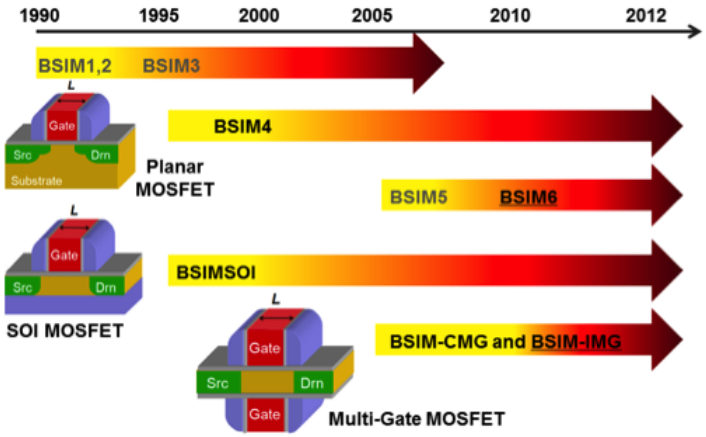


**Figure 1. 7. Timeline of BSIM models. [14]**

## 1.4 Thesis goal and Outline

Department of Integrated Devices and Circuits (EKT) at Royal Institute of Technology (KTH) Kista are developing different advanced CMOS technologies for the future integrated circuits. SOI CMOS baseline process is used to fabricate silicon transistors at the KTH Elektrum laboratory. The manufactured transistors have no calibrated computer model for circuit simulation. The goal of this paper is to present a calibrated SPICE model of the KTH transistors, start with a basic I-V model and work onward. Parameter extraction algorithms are designed from BSIMSOI compact model equations. The algorithms are written in MATLAB and it's designed to extract the basic I-V parameters from the device characteristics data. Subsequently, SPICE simulations are performed in Cadence Virtuoso to verify with the real measurement data.

Chapter 1 explains the motive and purpose of this thesis, presents the background of the problem and the future device architecture and compact models.

Chapter 2 describes The Basic MOSFET fundamentals; introduction of the KTH developed UTB MOSFET in detail and the fabrication process.

Chapter 3 presents the Models of BSIMSOI (Berkley Short-Channel IGFET Model Silicon-On-Insulator) specific for this paper, the understanding of these models is crucial for both extraction and simulation.

Chapter 4 focuses on the extraction and simulation of the UTB-MOSFET, extraction methods will be discussed and modeling result of KTH MOSFET will be presented.

Chapter 5 summarizes the overall work that has been done in this thesis and suggests for future work.

# Chapter 2 KTH UTBSOI MOSFET

KTH Department of Integrated Devices and Circuits (EKT) conduct different research within the European NANOSIL/SINANO Network of Excellence [15]. The network consist of European research laboratories and the main propose of NANOSIL is to strengthen the development of nanoelectronic materials and devices. Within the NANOSIL, KTH EKT conducts research focusing the topics of: New device architectures, High-k/metal gate stacks, High mobility channel materials, Metallic source/drain contacts, etc. The fabricated UTB MOSFET of this thesis is the result of the KTH EKT research. In order to understand the KTH device, the MOSFET fundamentals are presented in the next section. Furthermore, the KTH UTB MOSFET is discussed in section 2.2.

## 2.1 Basic MOSFET theory

The basic MOSFET theory are described in several reference books, the description in this section will focus on the related aspects of this work. For the simplicity, all the equations and calculations in this paper are considered for a NMOS device.

### 2.1.1 MOSFET operation

Some of the new MOSFET structures are discussed in Chapter 1, in this section focusing the basic MOSFET I-V characteristics. For CMOS technology, the transistor should act as a switch. It should have property like large ON-state current ($I_{on}$) and low OFF-state current ($I_{off}$). Depending on the different bias voltages applied to the drain ($V_{ds}$) for fixed gate, source and body biases. The output of a MOSFET device ($I_{ds} - V_{ds}$) can be divided into various operating regimes: Linear region ($0 < V_{ds} < V_{dsat}$), Saturation region ($V_{dsat} \leq V_{ds} < V_{bk}$) and Breakdown region ($V_{ds} > V_{bk}$). Figure 2.1 below divide the operation regimes in detail. The drain current in linear region can be expressed as the following:

$$I_{ds} = \frac{W}{L}\mu C_{ox}\left[(V_{gs} - V_{th})V_{ds} - \frac{m}{2}{V_{ds}}^2\right] \quad \textbf{( 2.1.1 )}$$

where $W$ is the channel width, $L$ is the channel length, $\mu$ is the mobility, $C_{ox}$ is the oxide capacitance and $m$ is the body-effect coefficient, it's defined as $m = 1 + C_{dep}/C_{ox}$. when the device reaches saturation which occur when $\mathrm{V_{ds}} = \mathrm{V_{dsat}}$:

$$\mathrm{V_{dsat}} = \frac{\mathrm{V_{gs}} - \mathrm{V_{th}}}{\mathrm{m}} \quad \textbf{( 2.1.2 )}$$

then the saturation drain current is given by:

$$I_{dsat} = \frac{W}{2mL}\mu C_{ox}(V_{gs} - V_{th})^2 \quad \textbf{( 2.1.3 )}$$

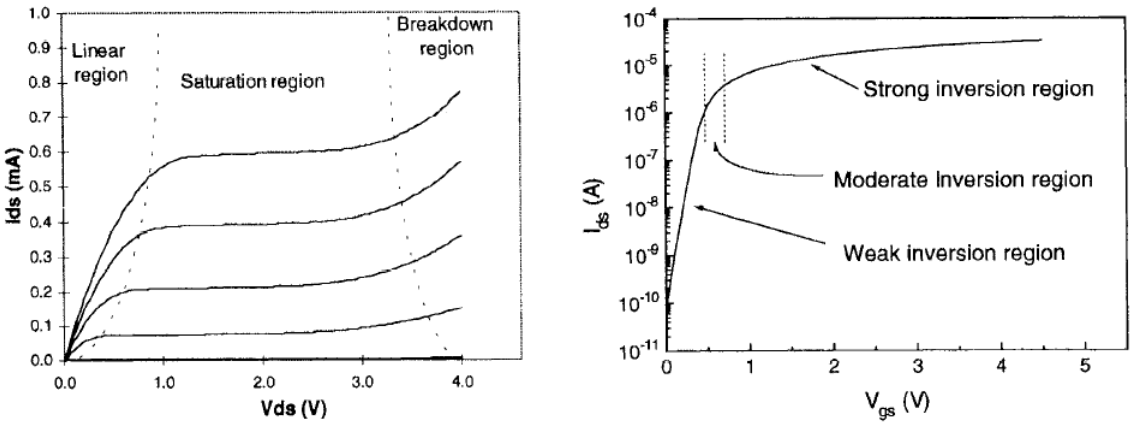


**Figure 2. 1. Device characterizes, Id vs Vds and Log(Ids) vs Vgs.**

Likewise, If the MOSFET drain bias of is fixed and bias voltage is applied to the gate. The $I_{ds} - V_{gs}$ characteristic can be divided into three regimes: weak, moderate and strong inversion region ($V_{th} < V_{gs}$ ).where moderate inversion is transition region between weak and strong inversion regions and weak and moderate together is also known as subthreshold ($0 < V_{gs} < V_{th}$). The subthreshold current is given by:

$$I_{ds} = I_0 e^{q(V_{gs} - v_{th})/mkT} \quad \textbf{( 2.1.4 )}$$

where $I_0$ is the current when $V_{gs} = V_{th}$ . Another important parameter for MOSFETs characteristics is the subthreshold slope (SS), it's defined as the following:

$$SS = \left[\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right]^{-1} \approx 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \quad \textbf{( 2.1.5 )}$$

where $C_{dep}$ is the depletion layer capacitance. A steep subthreshold slop or small SS value is desired for low OFF-state transistor current.

### 2.1.2 Significant Short-Channel Effects

In General, all the undesirable effects induced by short channel length can be categorized as "Short-Channel Effects". Typically, the short-channel effects consists of $V_{th}$ roll-off, drain induced barrier lowering and channel length modulation.

*Drain Induced barrier lowering*

The drain induced barrier lowering is an undesirable phenomenon in small field effect transistor, it occur when the channel length L decreases and the voltage $V_{ds}$ increases. Which cause lower barrier height between source and drain, lesser gate voltage is needed to bring the surface potential to $2\Phi_s$, thus the threshold voltage is lowered. The shorter the channel length is the bigger is the DIBL effect. Fig. 2.3a and 2.3b below illustrates the lowering of the barrier height between source and drain and the DIBL effect in IV plot. The lowering of barrier height cause a

shift in the IV plot, which leads to higher offset current and decrease of threshold voltage $V_{th}$.

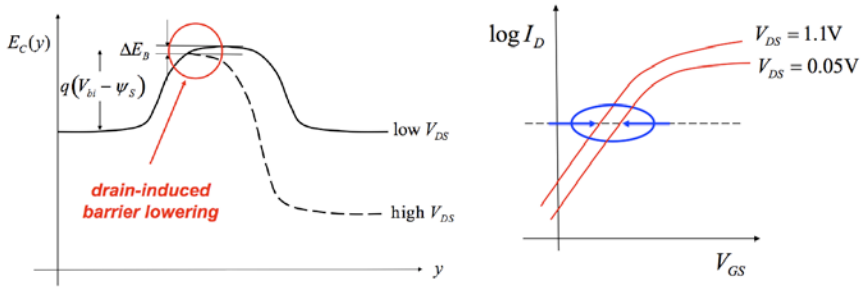


**Figure 2. 2. left) lowering of potential barrier height by drain and right) DIBL effect in Log Id vs Vgs plot.**

*Channel Length Modulation*

When some device operates in the saturation region and the drain current can increase with increasing drain bias. This phenomenon is known as channel length modulation (CLM). This effect is present for both short and long channel devices; however it's more distinct for short channel devices. This physical effect is due to the velocity saturation region grows when the drain bias increases, the device behaves as if the effective channel length has been reduced so the drain current increases.

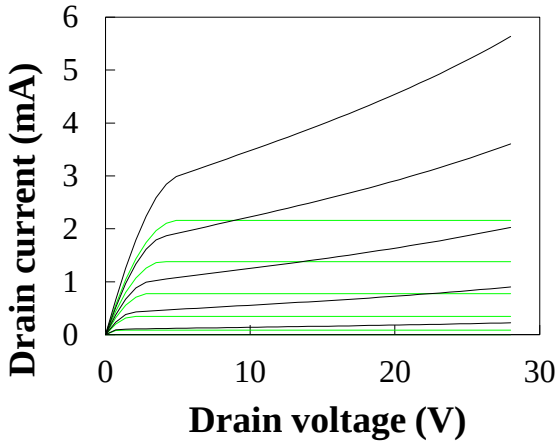


**Figure 2. 3. Ids vs. Vds with channel length modulation and without.**

## 2.2 KTH UTB SB-MOSFETs

In this work, UTB-MOSFET measurements from KTH Electrum laboratory are used for modeling. The Batch ID 308 consist of UTB-MOSFETs fabricated on SOI substrate where PtSi (Platinum silicide) is used as the Source/Drain metal with dopant segregation of B (Boron) and As (Arsenic). On top of SOI layer there is a 5 nm gate oxide, 20 nm TiN metal gate and doped poly-Silicon. A Schottky barrier junction is formed when metallic Source/Drain is used at channel edges, the MOSFET therefore commonly called Schottky barrier (SB) MOSFET. The main advantage of SB MOSFET is the parasitic source/drain resistance decreases by using metallic source/drain instead of doped silicon S/D. The Metal silicides are the most promising approach for implementing SB-MOSFET due to their low formation temperature and self-aligned processing. Figure 2.2. Below illustrate the KTH UTB SB-MOSFET.

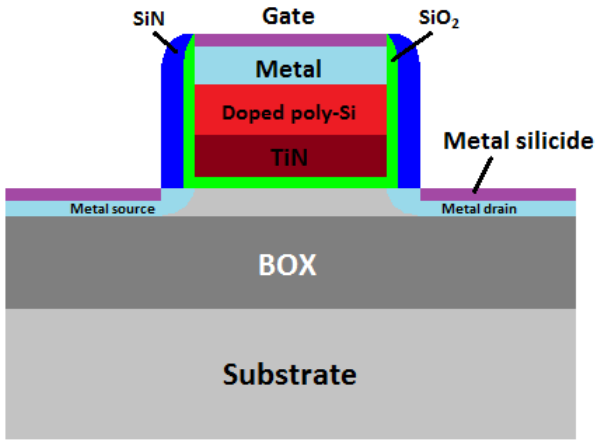


**Figure 2. 4. Illustration of the SB-MOSFET on UTB-SOI substrate with Metal S/D.**

KTH developed spacer patterning technique (STL, also known as Sidewall transfer lithography) are used for the fabrication, It's an important patterning technique to enable the fabrication of future nanoscale structures such as UTB and tri-gate MOSFETs [16].

### 2.2.1 Sidewall transfer lithography

Many pattern reduction technique or immersion lithography is used in the industry, such as EBL, or sidewall transfer lithography (STL). The STL technology consists of many unique features compared to other technologies in fabricating nanowires. For instance, STL automatically yields twin-nanowires if desire and better uniformity in comparison with those fabricated by EBL. An improved Sidewall transfer lithography (also known as spacer patterning) is developed by KTH [17], its important nanoscale patterning technique for the fabrication of nanoscaled KTH UTB and Tri-Gate MOSFETs. Figure 2.3 shows an optimized sidewall transfer lithography process flowchart.

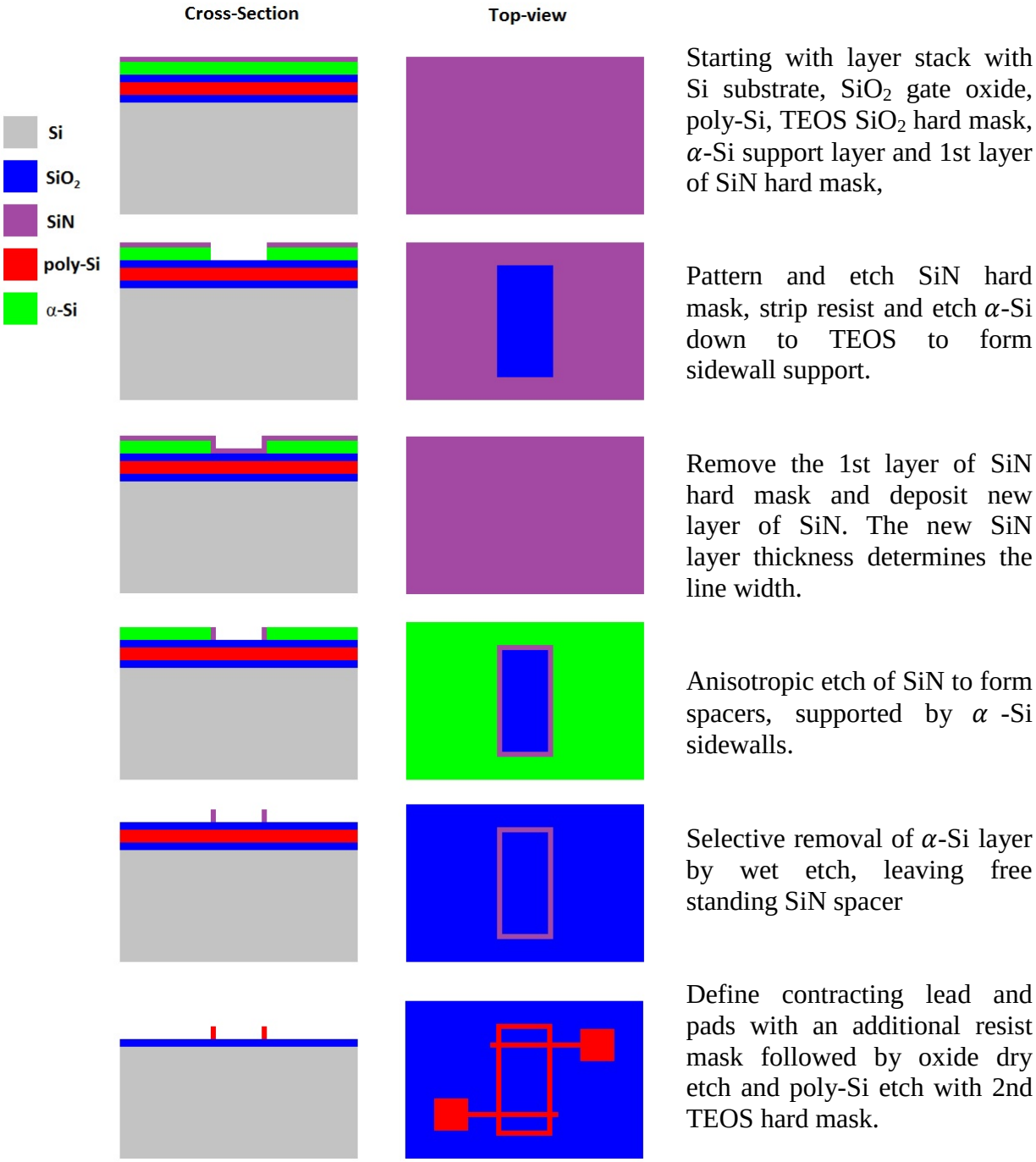


**Figure 2. 5. Schematic flow chart of the KTH improved STL technology, which is used in the fabrication of the SB-MOSFET.**

### 2.2.2 Fabrication process of UTB SB MOSFET

The major process steps of the fabrication process flow are summarized as below:

- Thinning SOI to 20-nm thickness
- Formation of MESA structure
- 5-nm thick gate oxide growth
- 20-nm TiN (Titanium Nitride) and 150-nm poly-Si (Polycrystalline silicon) gate formed by STL process
- Formation 10-nm SiN spacers
- PtSi formation at ≤600 Celsius
- Dopant segregation of Boron (B) and Arsenic (As) implanted
- Rapid thermal anneal at 700 Celsius for 30 second
- TiW/Al contact pad metallization
- Forming gas anneal at 400 Celsius for 30 min

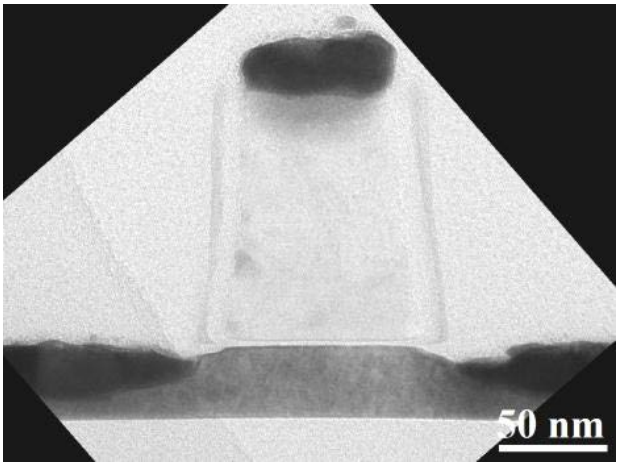


**Figure 2. 6. A cross-sectional transmission electron microscopy (XTEM) micrograph of UTB SB-MOSFET with PtSi S/D and As DS from KTH. [17]**

# Chapter 3 BSIM-SOI: A Compact Model for SOI MOSFETs

Circuit simulation is the bridge that links design and manufacturing worlds of the semiconductor industry. Today, there are numerous commercial SPICE simulators such as Spectre (Cadence) and TCAD (Synopsys). The need for new compact models is increasing as device technology advances. Many compact models for circuit simulation have been proposed in the past. The BSIM series compact models have served the industry for 20 years and The BSIM3v3 was the first selected MOSFET model for standardization by the Compact Model Council (Today know as Compact Model Coalition) [18], the BSIMSOI compact model used in this paper is based on BSIM3, therefore they share various model equations to ensure the compatibility. Compact model parameter extraction for SOI MOSFET is more complex than conventional bulk silicon MOSFET since more physical phenomena are involved; for example, floating body effect. The model parameters are usually extracted by commercial software such as ICCAP (Agilent tech) or BSIMProPlus (PROPLUS). These software products using global optimization to extract all hundreds of parameters at once, but the extracted value may not have any resemblance to the actual physical value.

This chapter presents a brief review of all the BSIMSOI sub-Models, focusing on the essential models for the extraction and simulation of KTH UTBSOI MOSFET.

## 3.1 Threshold Voltage Model

The threshold voltage is one of the key factors when modeling a device's electrical characteristics. it divide the transistor operation into three operational regions, strong inversion, moderate inversion and subthreshold region. In BSIMSOI, a continuous $V_{th}$ model for all operation regions is used and is given by [19]:

$$
\begin{aligned}
V_{th} = {} & V_{th0} + \left(K_{1ox} sqrtPhisExt - K_{1eff}\sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K_{2ox}V_{bseff} \\
& + K_{1ox}\left(\sqrt{1+\frac{LPEB}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + \left(K_3 + K_{3b}V_{bseff}\right)\frac{T_{ox}}{W'_{eff} + W_o}\Phi_s \\
& - D_{VT0w}\left(exp\left(-D_{VT1w}\frac{W'_{eff}L_{eff}}{2l_{tw}}\right) + 2exp\left(-D_{VT1w}\frac{W'_{eff}L_{eff}}{l_{tw}}\right)\right)(\mathrm{V}_{bi} \\
& \qquad - \Phi_s) \qquad \text{( 3.1.1 )} \\
& - D_{VT0}\left(exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2exp\left(-D_{VT1w}\frac{L_{eff}}{l_t}\right)\right)(\mathrm{V}_{bi} - \Phi_s) \\
& - \left(exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right) + 2exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)(\mathrm{E}_{tao} - \mathrm{E}_{tab}\mathrm{V}_{bseff})\mathrm{V}_{ds} \\
& - nv_t \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + e^{-DVTP1 \cdot V_{DS}})}\right) \\
& - \frac{DVTP2}{L_{eff}^{\,DVTP3}} \cdot \tanh(DVTP4 \cdot V_{DS})
\end{aligned}
$$

$$V_{th} = V_{th0} + \left(\Delta V_{th,body\_effect} - \Delta V_{th,reverse\_short\_channel} - \Delta V_{th,narrow\_width} + \Delta V_{th,small\_size} + \Delta V_{th,charge\_sharing} + \Delta V_{th,DIBL}\right)$$

Equation 3.2.1 describes the threshold voltage $V_{th}$ for both PD and FD SOIMOSFETs. It consists of 10 parts, which is used to model different physical effects; such as non-uniform doping, short channel effect, narrow channel effect, etc. In this paper only the first term $V_{th0}$, was considered and modeled. It describes the threshold voltage of a long channel device at zero volt substrate bias and is defined by the following:

$$V_{th0} = V_{FB} + \Phi_s + K_1\sqrt{\Phi_s} \quad \textbf{( 3.1.2 )}$$

Where $V_{FB}$ is the flat-band voltage, $K_1$ is the model parameter for the first order body effect coefficient and $\Phi_s$ is the surface potential at threshold, given by:

$$\phi_s = \frac{k_B T}{q}\ln\left(\frac{N_a}{n_i}\right) \equiv 2\phi_B \quad \textbf{( 3.1.3 )}$$

Notice $V_{th0}$ can be fixed by user, otherwise its calculated. The terms after $V_{th0}$ is not considered in the modeling and will only be explained

"MOSFET Modeling BSIM3 User's guide by Y. Cheng and C.Hu" is required for further reading if one wish to model of these effects, since BSIMSOI user manual have not threshold voltage model.

The second and third terms are used to model the vertical non-uniform doping effect,

$$\Delta V_{th,body\_effect} = \left(K_{1ox}sqrtPhisExt - K_{1eff}\sqrt{\Phi_s}\right)\sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox}V_{bseff}$$

Large reverse bulk-source bias (Vbs) and Heavy channel doping (NCH)

The fourth term is for the lateral non-uniform doping effect,

$$\Delta V_{th,reverse\_short\_channel} = K_{1ox}\left(\sqrt{1 + \frac{LPEB}{L_{eff}}} - 1\right)\sqrt{\Phi_s}$$

Short-channel transistor with large NLX

The fifth term is for the narrow width effect,

$$\Delta V_{th,narrow\_width} = \left(K_3 + K_{3b}V_{bseff}\right)\frac{T_{ox}}{W'_{eff} + W_o}\Phi_s$$

Narrow-width devices

The sixth term is to small size effect in devices with both small channel length and small width.

$$\Delta V_{th,small\_size} = D_{VT0w}\left(exp\left(-D_{VT1w}\frac{W'_{eff}L_{eff}}{2l_{tw}}\right) + 2exp\left(-D_{VT1w}\frac{W'_{eff}L_{eff}}{l_{tw}}\right)\right)(\mathrm{V}_{bi} - \Phi_s)$$

Narrow-width and short-channel transistors

The seventh and eighth terms are related to the short channel effect due to DIBL.

$$\Delta V_{th,charge\_sharing} = D_{VT0}\left(exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2exp\left(-D_{VT1w}\frac{L_{eff}}{l_t}\right)\right)(\mathrm{V}_{bi} - \Phi_s)$$

short-channel transistors

$$\Delta V_{th,DIBL} = \left(exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right) + 2exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)(\mathrm{E}_{tao} - \mathrm{E}_{tab}\mathrm{V}_{bseff})\mathrm{V}_{ds}$$

Short-channel devices under large Vds
the last two is introduces to capture the DIBL variation in longer channel.

$$\Delta V_{th,DIBL} = nv_t \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + e^{-DVTP1 \cdot V_{DS}})}\right) - \frac{DVTP2}{L_{eff}^{\ DVTP3}} \cdot \tanh(DVTP4 \cdot V_{DS})$$

## 3.2 Unified I-V Model

A accurate I-V characteristics is also required for a good compact model. The I-V characteristics are mainly influenced by two key factors, channel charge and mobility. The single drain current equation of BSIMSOI will be introduced after all the sub-models are discussed.

### 3.2.1 Channel Charge Model

BSIMSOI uses the same channel charge model as BSIM3, the unified expression for the channel charge $Q_{ch}$ from strong inversion and subthreshold regions, the channel change density at source end for both subthreshold and inversion region is defined by:

$$Q_{chs0} = C_{ox} V_{gsteff} \tag{3.2.1}$$

where $V_{gsteff}$ is the Effective $V_{gs} - V_t$ function introduced to describe the channel charge characteristics from subthreshold to strong inversion. Effective $V_{gst}$ for all regions (with Polysilicon Depletion Effect) is defined as following:

$$V_{gsteff} = \frac{nv_t \ln\left[1 + \exp\left(\frac{m^*(V_{gs\_eff} - V_{th})}{nv_t}\right)\right]}{m^* + nC_{ox}\sqrt{\frac{2\phi_s}{q\varepsilon_{si}N_{dep}}}\exp\left(-\frac{(1-m^*)(V_{gs\_eff} - V_{th}) - V_{off}}{nv_t}\right)} \tag{3.2.2}$$

$$\text{where } m^* = 0.5 + \frac{\tan^{-1}(MINV)}{\pi} \xrightarrow{MINV=0} m^* = 0.5$$

MINV is $V_{gsteff}$ fitting parameter for moderate inversion, the default value is 0. Equation 3.3.11 without Polysilicon depletion becomes:

$$V_{gsteff} = \frac{2nv_t \ln\left[1 + \exp\left(\frac{(V_{gs} - V_{th})}{2nv_t}\right)\right]}{1 + 2nC_{ox}\sqrt{\frac{2\phi_s}{q\varepsilon_{si}N_{dep}}}\exp\left(-\frac{V_{gs} - V_{th} - 2V_{off}}{2nv_t}\right)} \tag{3.2.3}$$

where $V_{off}$ is the offset voltage in the subthreshold region for large W and L and was added to describe the threshold voltage difference between strong inversion and subthreshold region.

### 3.2.2 Mobility Model

Mobility is one of the key parameters in a MOSFET model. It describes the relation between drift velocity of electrons or holes and an applied electric field in the semiconductor materials.

$$v = \mu \boldsymbol{E} \tag{3.2.4}$$

where $v$ is the drift velocity, $\boldsymbol{E}$ is the electric field and μ is the mobility. This topic has been well studied since the 1970's [20], there are three scattering mechanisms proposed to explain the

surface mobility of the model: Phonon, coulomb and surface roughness scattering. The figure 3.1 below illustrate that each mechanism is dominant under different conditions, such as varying temperature. Other conditions are bias and doping concentration.

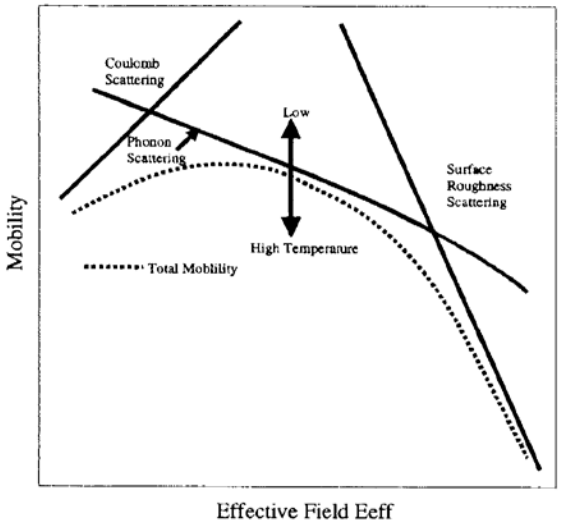


**Figure 3. 1. The three dominant scattering mechanisms affecting the mobility in the inversion layer under different temperature. [20]**

Furthermore, the different process parameters and bias condition also affect the mobility. Such as the gate oxide thickness, doping concentration, threshold voltage etc. In order to simplify the model, an empirical unified formulation based on the concept of an effective field is proposed by [21] to compile all the parameters and biases.

$$E_{eff} = \frac{Q_B + (Q_n/2)}{\varepsilon_{si}} \quad \textbf{( 3.2.5 )}$$

The unified equation of mobility is given below:

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + (\text{E}_{\text{eff}}/\text{E}_0)^{\text{v}}} \quad \textbf{( 3.2.6 )}$$

For a continuous I-V model, a continuous mobility model is required. BSIMSOI use a unified mobility expression based on the $\text{V}_{\text{gsteff}}$ expression of Eq 3.3.7

$$\mu_{eff} = \frac{\mu_0}{1 + \left(U_A + U_C V_{bseff}\right)\left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right) + U_B\left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right)^2} \quad \textbf{( 3.2.7 )}$$

Where $\mu_0$ is the zero-field mobility parameter in the universal mobility formulation when temp = tnom, $U_A$ is model parameter for the first-order mobility degradation, $U_B$ is model parameter for the second-order mobility degradation and $U_C$ is model parameter for the body-effect of mobility degradation. The body effect is not considered in this work; therefore 3.2.7 can be rewritten into 3.2.8.

$$\mu_{eff} = \frac{\mu_0}{1 + U_A\left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right) + U_B\left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right)^2} \quad \textbf{( 3.2.8 )}$$

Equation 3.2.8 will be the mobility equation used in parameter extraction and modeling.

### 3.2.3 Carrier Drift Velocity

Another important parameter in transistor modeling is the carrier drift velocity. Defined in 3.3.9

$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + (E/E_{\text{sat}})}, & \text{E} < \text{E}_{\text{sat}} \\ v_{\text{sat}}, & \text{E} > \text{E}_{\text{sat}} \end{cases} \quad \textbf{( 3.2.9 )}$$

$E_{\text{sat}}$ corresponds to the critical electrical field at which the carrier velocity becomes saturated.

$$E_{\text{sat}} = \frac{2v_{sat}}{\mu_{eff}} \quad \textbf{( 3.2.10 )}$$

The saturation velocity, $v_{\text{sat}}$ , is given by $E_{\text{sat}}$is the critical field for saturation velocity.

### 3.2.4 Bulk Charge Effect

In bulk device, the depletion region thickness will not be uniform along the channel when a non-zero $V_{ds}$ is applied. As result threshold voltage varies along the channel; this effect is called bulk charge effect. BSIMSOI uses parameter $A_{bulk}$ to model the bulk charge effect and is defined as the following equation:

$$A_{bulk} = 1 + \left[\frac{K_{1ox}\cdot\sqrt{1 + LPEB/L_{eff}}}{2\sqrt{(\phi_s + Ketas)} - \frac{V_{bsh}}{1+Keta\cdot V_{bsh}}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{T_{si}X_{dep}}}\left(1 - A_{gs}V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{T_{si}X_{dep}}}\right)^2\right) + \frac{B_0}{W'_{eff} + B_1}\right)\right] \quad \textbf{( 3.2.11 )}$$

Because the architecture difference between UTB-SOI and Bulk devices, this effect can neglected/simplified for UTB-SOI MOSFET modeling. Generally, for Bulk devices the $A_{bulk}$ is close to 1 if the channel length is small and grows as the channel length increases. Which means the bulk charge effect is small when the channel length is small and grows with the channel length. For the modeling of UTB-SOI, $A_{bulk}$ is assumed to be 1, so few parameters need to set to corresponding value. The parameters $A_0$ is Bulk charge effect coefficient for channel length and $B_0$ is Bulk charge effect coefficient for channel width, both will be set to zero so $A_{bulk}$ is equal with 1.

### 3.2.5 The $n$ Parameter for Subthreshold Swing

The subthreshold swing is determined by the swing factor or slope factor $n$, it can be defined as the following:

$$SS = \frac{dV_{gs}}{d \log I_{ds}} \approx 2.3 n v_t \quad \textbf{( 3.2.12 )}$$

The $n$ parameter is the key parameter for the devices subthreshold swing

$$n = 1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \quad \textbf{( 3.2.13 )}$$

in BSIMSOI $n$ is defined by

$$n = 1 + N_{FACTOR} \frac{\varepsilon_{si} / X_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} + \frac{(C_{DSC} + C_{DSCD} V_{ds} + C_{DSCB} V_{bseff}) \left[\exp\left(-D_{VT1} \frac{L_{eff}}{2 l_t}\right) + 2\exp\left(-D_{VT1} \frac{L_{eff}}{2 l_t}\right)\right]}{C_{ox}} \quad \textbf{( 3.2.14 )}$$

where $X_{dep}$ is the width of the channel depletion.

Parameter $N_{FACTOR}$ Introduced to cover for any uncertainty in the calculation of the depletion capacitance and is determined experimentally. $C_{it}$is called the interface depletion capacitance and accounts for the influence of the interface charge density.$C_{DSC}, C_{DSCD}, C_{DSCB}$are parameters to describe the coupling effects between the drain and the channel due to the DIBL effect.In this thesis, the short channel effect parameters are assumed to be equal zero, Eq 2.1.14 can be written as the following expression:

$$n = 1 + N_{FACTOR} \frac{\varepsilon_{si} / X_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} + \frac{(C_{DSC})}{C_{ox}} \quad \textbf{( 3.2.15 )}$$

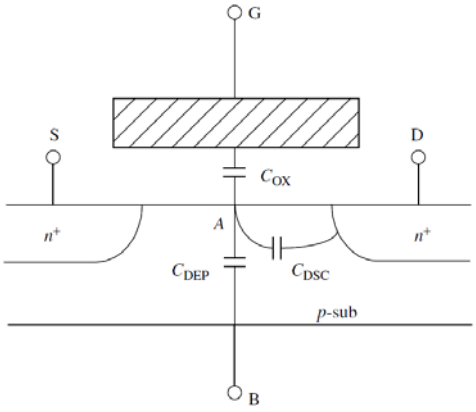


**Figure 3. 2. gate oxide capacitance, channel depletion capacitance and coupling capacitances.**

### 3.2.6 Unified Drain Equation of BSIMSOI

The drain equations in semiconductor courses are often defined as eq. 2.1.1. In BSIMSOI, one single drain current equation is designed to link all the operating regions [23]:

$$I_{ds} = \frac{I_{ds0}}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right) \quad \textbf{( 3.2.16 )}$$

where $\beta$ is given by:

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \quad \textbf{( 3.2.17 )}$$

$I_{ds0}$ is defined as:

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2V_t)}\right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}} \quad \textbf{( 3.2.18 )}$$

and $V_{dseff}$ is the effective source-drain bias (Eq. 3.3.20), $R_{ds}$ is the source/drain series resistance, $\mu_{eff}$ is the effective mobility calculated in Equation: 3.3.8. $V_A$ account for channel length modulation (CLM) and drain-induced barrier lowering (DIBL) and is expressed as the following equation:

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}\right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1} \quad \textbf{( 3.2.19 )}$$

where $V_{ACLM}$ account the effect of channel length modulation and $V_{ADIBLC}$ for drain-induced barrier lowering. $V_{Asat}$ is $V_A$ at saturation point where (Vds=Vdsat).

For intrinsic case ($R_{ds} = 0$), $V_{dsat}$ is define by

$$V_{dsat} = \frac{E_{sat} L_{eff} (V_{gsteff} + 2V_t)}{A_{bulk} E_{sat} L_{eff} + (V_{gsteff} + 2V_t)} \quad \textbf{( 3.2.20 )}$$

where $E_{sat}$ is the critical electrical field at which the carrier velocity becomes saturated.

$$E_{sat} = \frac{2 v_{sat}}{\mu_{eff}} \quad \textbf{( 3.2.21 )}$$

Since CLM and DIBL is not modeled and $E_{sat}$ is assumed to be infinite. As a result parameter $V_A$ will in addition be infinite due to $V_{Asat} = \infty$. The single drain current equation can be simplified to the following:

$$I_{ds} \approx \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} V_{gsteff} \left(1 - \frac{V_{dseff}}{2\left(V_{gsteff} + 2v_t\right)}\right) V_{dseff} \quad \textbf{( 3.2.22 )}$$

and $V_{dseff}$ function is introduced to guarantee continuities of $I_d$ and its derivatives at $V_{dsat}$

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right) \quad \textbf{( 3.2.23 )}$$

where $\delta$ is a user specified parameter with a default value of 0.01.

## 3.3 Model Selector SOIMOD

BSIMSOI is developed with BSIM3 and BSIMPD as foundations, it's a unified model for both PD and FD SOI MOSFET based on the concept of body-source build-in potential lowering [22]. It's a concept that unify both PD and FD SOI modeling, where the difference between the PD and FD is modeled by build-in potential lowering $\Delta V_{bi}$, as an indication for the degree of depletion.

There are four modes in BSIMSOI: BSIMPD (soiMod = 0) is for PD-SOI MOSFETs modeling, unified SOI model (soiMod = 1), ideal FD model (soiMod = 2) is used to model FD device. There is no body node and the body current/charge calculation is skipped. Furthermore, the body voltage $V_{bs}$ is pinned at $\Delta V_{bi} = V_{bs0}$.

$$\begin{aligned} \Delta V_{bi} = V_{bs0} = {} & \frac{C_{si}}{C_{Si} + C_{BOX}} \cdot \left(\phi - \frac{qN_{ch}}{2\varepsilon_{Si}} \cdot {T_{si}}^2 + V_{nonideal} + \Delta V_{DIBL}\right) \\ & + \eta_e \frac{C_{BOX}}{C_{Si} + C_{BOX}} (V_{es} - V_{FBb}) \end{aligned} \quad \textbf{( 3.3.1 )}$$

where

$$C_{si} = \frac{\varepsilon_{si}}{T_{si}}, C_{BOX} = \frac{\varepsilon_{OX}}{T_{BOX}}, C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}}$$

$V_{nonideal}$ is the offset voltage due to non-idealities, $\Delta V_{DIBL}$accounts the short channel effect on $\Delta V_{bi}$ and $\eta_e$ for the short channel effect on the backgate coupling. These three values is assumed to be zero when modeling, the new $\Delta V_{bi}$

$$\Delta V_{bi} = V_{bs0} = \frac{C_{si}}{C_{Si} + C_{BOX}} \cdot \left(\phi - \frac{qN_{ch}}{2\varepsilon_{Si}}\right) \quad \textbf{( 3.3.2 )}$$

where

$$\phi = \Phi_{ON} - \frac{C_{OX}}{C_{OX} + \left({C_{Si}}^{-1} + {C_{BOX}}^{-1}\right)^{-1}} \cdot N_{OFF,FD} v_t \cdot \ln\left(1 + exp\left(\frac{V_{th,FD} - V_{gs\_eff} - V_{OFF,FD}}{N_{OFF,FD} v_t}\right)\right) \quad \textbf{( 3.3.3 )}$$

$N_{OFF,FD}$ and $V_{OFF,FD}$ are model parameters to improve the transition between subthreshold and strong inversion regions, $v_t$ is the thermal voltage and the surface band bending at strong inversion, $\Phi_{ON}$ is given by:

$$\Phi_{ON} = 2\Phi_B \quad \textbf{( 3.3.4 )}$$

## 3.4 Real Device effects

Real physical device effects are important for representing the output characteristics of SOI MOSFETs. The real device effects considered in BSIM-SOI are listed in table below [23]; some of them are modeled in this paper, for further reading about these real device effects, references are listed in Appendix B.

**Table 2. 1. Real device effect modules in BSIMSOI**

| | Real device effect module |
|---|---|
| **1** | Short Channel Effects |
| **2** | Vth roll-off |
| **3** | Subthreshold Swing Degradation |
| **4** | Drain Induced Barrier Lowering |
| **5** | Channel Length Modulation |
| **6** | Source/Drain Series Resistance |
| **7** | Parasitic Capacitance |
| **8** | Mobility Degradation |
| **9** | Poly Depletion Effect |
| **10** | Velocity Saturation |
| **11** | Velocity Overshoot |
| **12** | Gate Induced Drain Leakage |
| **13** | Source/Drain Junction Leakage |
| **14** | Impact Ionization |
| **15** | Temperature effects and self-heating |

# Chapter 4 Parameter Extraction and Modeling of KTH MOSFET

Parameter extraction is an important part of device modeling. Depending on the model, there is different methodology used for the extraction. In this section, the BSIMSOI suggested extraction method will be reviewed. Furthermore, the parameter extraction result will be presented.

## 4.1 Overview

There are several extraction and optimization methods when it comes to extraction of model parameters. The commercial extraction software often use global optimization to extract all the model parameters at once, the one set of parameters will fit all the experimental data but the globally optimized parameters often doesn't have any resemblance to its actual physical value. Opposite of global optimization there is local optimization. Local optimization is performed for different operation regions where different device behaviors are dominant. The locally optimized parameters don't fit well with the experimental data in all device operating regions. However they show close resemblance to the physical value.

Furthermore, there are also device geometry related methods for the parameter extraction: Single device extraction and group device extraction. The first method use only one type of device geometry to extract all of the model parameters, the extracted values fit only to the same type of device very well and don't fit with other device geometries. This method is often used in the early days, when the device geometry had little effect on the device models. It is no longer practical since extraction with only one channel length and width cannot determine parameters with channel length and channel width dependencies, such as short channel effects and narrow width effects. Nowadays, group extraction method is often used in model parameter extraction where experimental data from multiple devices with different length and width are used. The advantage of this method is it can fit many devices with different geometries.

BSIMSOI is based on the BSIM3 core models [24]; therefore the extraction routines are almost identical. One start with a combination of local optimization and group device extraction strategy to obtain the preliminary parameters, then a global optimization can be used to improve the overall accuracy between the model and the measurement. In this paper, due to lack of group device measurements, a local optimized and single device extraction is performed to illustrate the basic models in BSIMSOI and modeling of KTH MOSFET.

### 4.1.1 Optimization method

The optimization process used in this paper is a combination of Newton-Raphson iteration and a linear least-square fit routine. The model equation with one, two, or three variables need to be first arranged in a form suitable for the iteration equation 4.2.1 given by [25]:

$$f_{exp}(P_{10}, P_{20}, P_{30}) - f_{sim}\left({P_1}^{(m)}, {P_2}^{(m)}, {P_3}^{(m)}\right) = \frac{\partial f_{sim}}{\partial P_1}\Delta {P_1}^{m} + \frac{\partial f_{sim}}{\partial P_2}\Delta {P_2}^{m} + \frac{\partial f_{sim}}{\partial P_3}\Delta {P_3}^{m} \quad \textbf{( 4.1.1 )}$$

where f() is the function to be optimized, parameters $P_1, P_2$ and $P_3$ are to be extracted,

$P_{10}, P_{20}$and $P_{30}$are the true physical values. $P_1{}^{(m)}$, $P_2{}^{(m)}$and $P_3{}^{(m)}$ are the parameter values after the m-th iteration. Figure 4.1 below describe the procedures of the optimization.

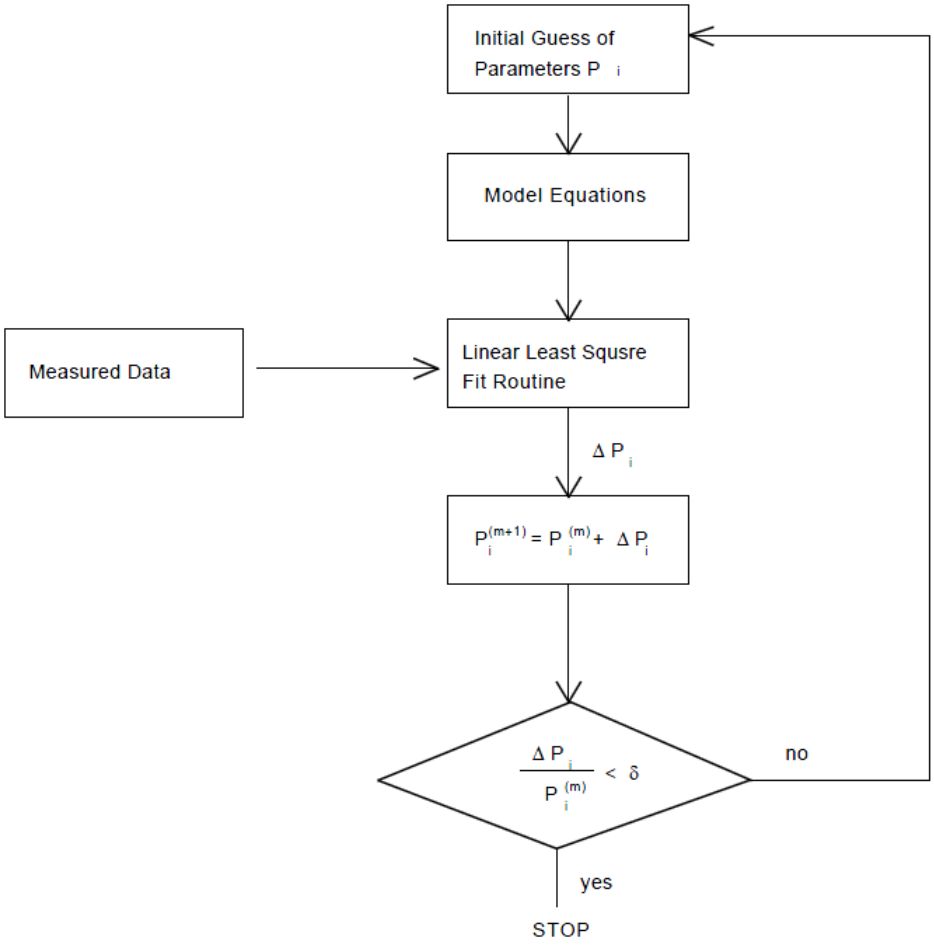


**Figure 4. 1. Flowchart of the optimization process [25]**

### 4.1.2 Process parameters and I-V Measurements

The Table 4.1 below is the process parameters for the KTH UTBSOI MOSFET.

**Table 4. 1. KTH transistor parameters**

| Parameter | Physical meaning | Value | Unit |
|---|---|---|---|
| $T_{ox}$ | Thickness of gate oxide | 5x10^-9 | m |
| $T_{si}$ | Thickness of silicon film | 2x10^-8 | m |
| $T_{box}$ | Thickness of buried oxide | 1.45x10^-7 | m |
| $N_{ch}$ | Doping concentration in channel | 1x10^+15 | $1/cm^3$ |
| $N_{sub}$ | Doping concentration in substrate | 6x10^+16 | $1/cm^3$ |
| $L$ | Channel length | 1x10^-6 | m |
| $W$ | Channel width | 1x10^-5 | m |
| $X_j$ | Junction depth | $T_{si}$ | m |

The BSIMSOI manual suggested I-V measurement for basic MOS I-V parameters:

- $I_{ds}$ vs. $V_{gs}$ @ Small $V_{ds}$ and $V_{es} = 0$V.
- $I_{ds}$ vs. $V_{gs}$ @ $V_{ds} = V_{dd}$ and $V_{es} = 0$V.
- $I_{ds}$ vs. $V_{ds}$ @ with different $V_{gs}$ and $V_{es} = 0$V.

Drain was biased to Vds, Gate was biased to Vgs, Source was biased to zero and Substrate is biased to zero. Figure 4.2 illustrate the transistor schematic simulated in cadence. Where G is gate, D is drain, S is source and E is the body bias.

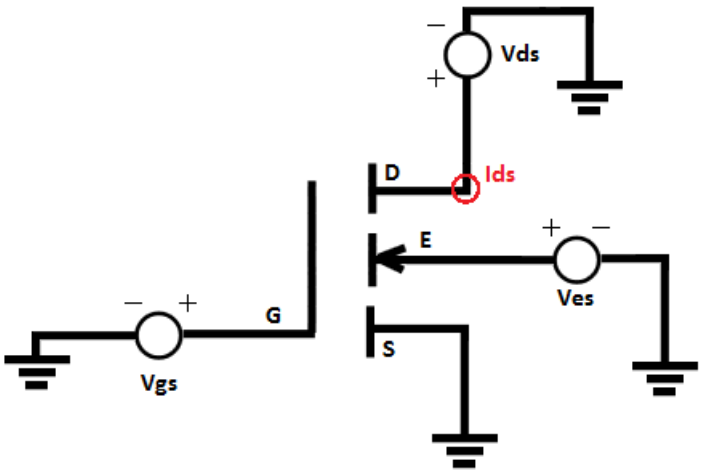


**Figure 4. 2. Schematic of Cadence simulation**

## 4.2 Extraction of the threshold voltage

The extrapolation in linear region method is the most popular threshold-voltage extraction method, it consist of finding the gate-voltage intercept at Id=0 of the extrapolated maximum first derivative slope. The numbers of steps are described below:

1. Measure $I_{ds} - V_{gs}$ characteristics at low $V_{ds}$(<0.1V)
2. Determine the maximum slope of $I_{ds} - V_{gs}$ curve, at the maximum $g_m$ point.
3. Extrapolate $I_{ds} - V_{gs}$ from the maximum $g_m$ point to $I_{ds} = 0$.
4. Find the corresponding extrapolated $V_{gs}$ value ($V_{gs0}$) for $I_{ds} = 0$.
5. Calculate $V_{th}$ according to $V_{th} = V_{gs0} - 0.5\, V_{ds}$.

The Matlab script function ExtractVth (see appendix A) follows the extraction steps, extract the threshold voltage value for specific drain current and print out a figure with maximum slope. Figure 4.3 below illustrate the Ids-Vgs curve, transconductance curve and the maximum slope.

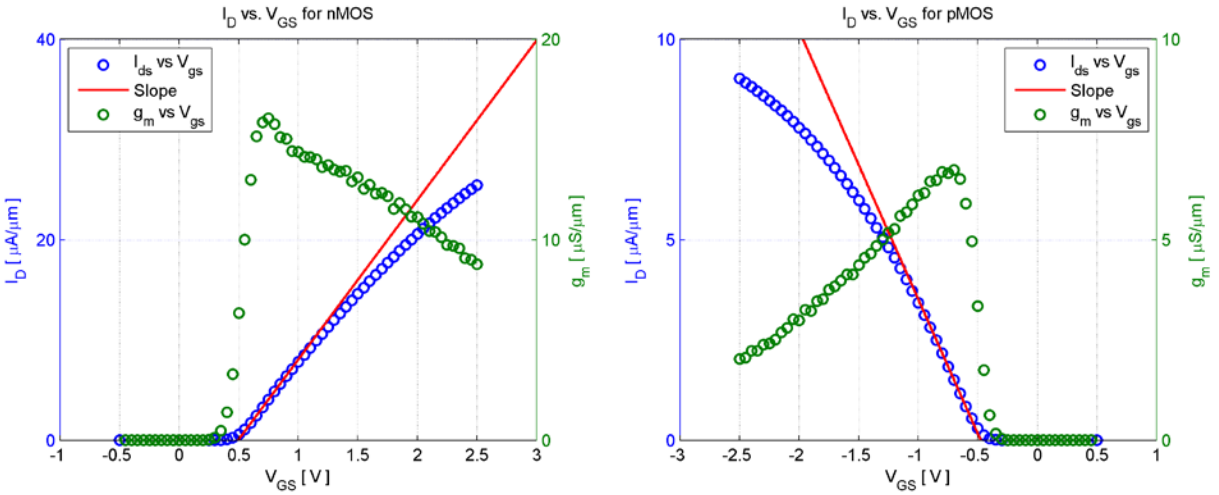


**Figure 4. 3. linear region drain current Id, transconductance gm vs Vgs and maximum slope curve. Symbols: KTH measurements, Lines: Matlab fit**

The Extracted threshold voltage values are shown below in Table 4.1.

**Table 4. 2. Extracted threshold voltages**

| | $V_{th}$ NMOS | $V_{th}$ PMOS |
|---|---|---|
| Extracted value | 0.443 V | -0.426 V |
| Reference data | 0.51±0.023 V | -0.49±0.036 V |

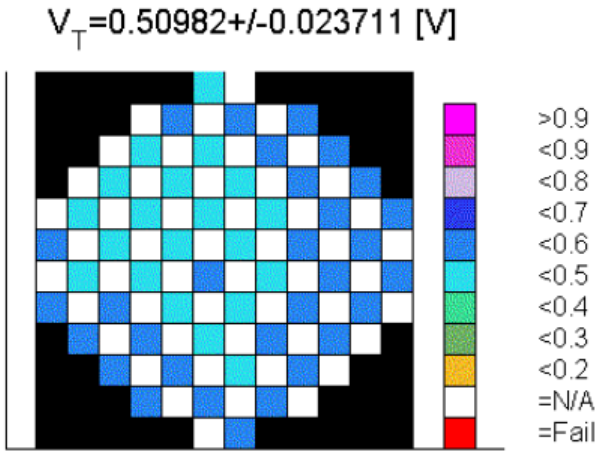


**Figure 4. 4. NMOS 308 Batch**

The same batch of transistors has the average threshold voltage value as 0.51+/-0.023.

## 4.3 Extraction of the mobility parameters

The fitting target data for the mobility parameters is the strong inversion region. The body effect is assumed to be negligible, thus the body-effect of mobility degradation coefficient Uc is equal zero. The new effective mobility equation shows below:

$$\mu_{eff} = \frac{\mu_0}{1 + U_A\left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right) + U_B\left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right)^2}$$

Equation 2.5.10 can rewrite as the following relations:

$$\mu_{eff}\frac{V_{gsteff}+2V_{th}}{T_{ox}} = A, \quad \left(\frac{V_{gsteff}+2V_{th}}{T_{ox}}\right)^2 = A^2 = B \tag{4.3.1}$$

$$\mu_{eff} = \frac{\mu_0}{1 + U_A A + U_B B} \tag{4.3.2}$$

$$\mu_{eff} = \mu_0 - \mu_{eff}U_A A - \mu_{eff}U_B B \tag{4.3.3}$$

Rewrite the equations 4.3.3 to fit inside the optimizing equation 4.1.1:

$$f_{sim} = \mu_0 - \mu_{eff}U_A A - \mu_{eff}U_B B - \mu_{eff} = 0$$

$$\frac{\partial f_{sim}}{\partial \mu_0} = 1, \qquad \frac{\partial f_{sim}}{\partial U_A} = -\mu_{eff}A, \qquad \frac{\partial f_{sim}}{\partial U_B} = -\mu_{eff}B$$

$$f_{exp}(\mu_{00}, U_{A0}, U_{B0}) - f_{sim}\left(\mu_0{}^{(m)}, U_A{}^{(m)}, U_B{}^{(m)}\right) = \Delta\mu_0{}^m + -\mu_{eff}A\Delta U_A{}^m - \mu_{eff}B\Delta U_B{}^m \tag{4.3.4}$$

There are three unknown parameters and the laboratory data have more than three strong inversion measurement points. Therefore the parameter can be extracted by the solving the following over-determined equation system:

$$\begin{bmatrix}\mu_0\\ U_A\\ U_B\end{bmatrix} = \begin{bmatrix}1-\mu_{eff(1)}A_{(1)}-\mu_{eff(1)}B_{(1)}\\ 1-\mu_{eff(2)}A_{(2)}-\mu_{eff(2)}B_{(2)}\\ 1-\mu_{eff(3)}A_{(3)}-\mu_{eff(3)}B_{(3)}\\ \vdots\\ 1-\mu_{eff(n)}A_{(n)}-\mu_{eff(n)}B_{(n)}\end{bmatrix}^{-1}\begin{bmatrix}\mu_{eff(1)}\\ \mu_{eff(2)}\\ \mu_{eff(3)}\\ \vdots\\ \mu_{eff(n)}\end{bmatrix} \quad \textbf{( 4.3.5 )}$$

The parameter value $\mu_0$ after (m+1) th iteration are given by:

$$\mu_0{}^{(m+1)} = \mu_0{}^{(m)} + \Delta\mu_0{}^{(m)} \quad \textbf{( 4.3.6 )}$$

The iteration is terminated when the increments of all three parameter are less than limit given by user. The extracted value is show in table 4.3.

**Table 4. 3. Extracted Mobility Parameters**

| | NMOS | PMOS |
|---|---|---|
| $\mu_0$ | 0.0258 | 0.0121 |
| $U_A$ | 3.3756e-10 | 4.7573e-10 |
| $U_B$ | 5.5816e-19 | 1.6858e-18 |

## 4.4 Cadence verification

The Cadence Virtuoso is used to simulate the circuit from figure 4.2 and the results are exported to Matlab for plot and error calculation.

### 4.4.1 Result for NMOS

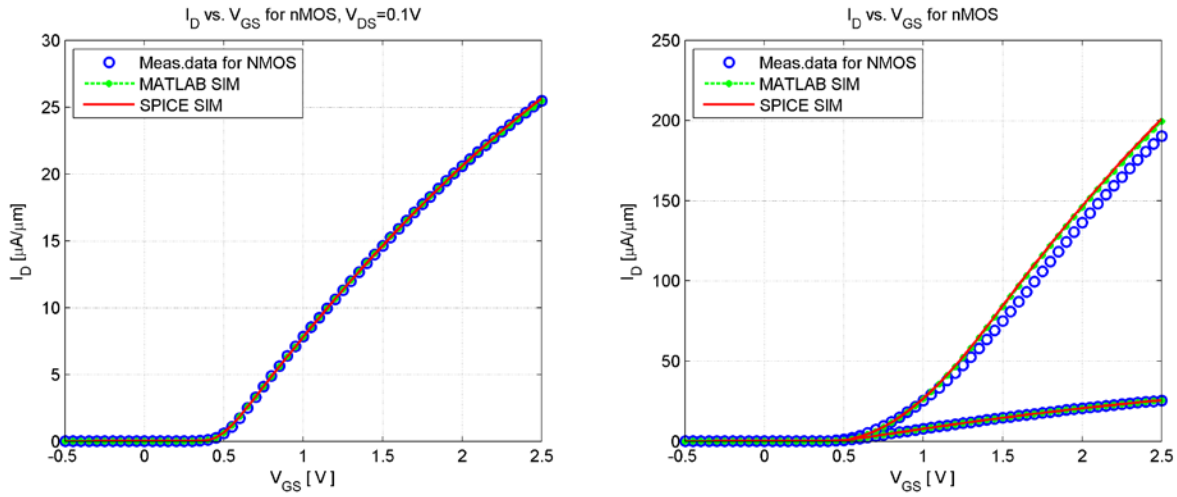


**Figure 4. 5. Measured and simulated $I_d$-$V_{gs}$ under different drain bias voltages ( $V_{ds}$) 0.1V and 1V. (Left figure) only linear region (0.1V), right figure consist of (0.1V) and (1V).**

Figure 4.5 left) show the drain current for linear region fit well with the extracted mobility

parameters, in the right figure the drain current for saturation region does not fit well with the measurement data. A closer look in the mobility curve reveals the bad fiting

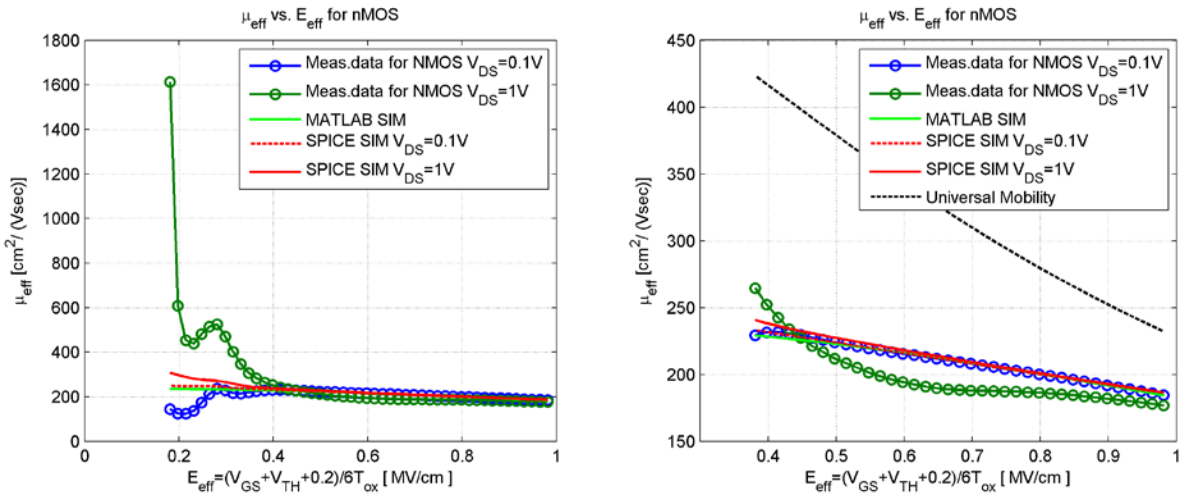


**Figure 4. 6. Measured and simulated mobility versus effective field under different drain bias voltages ($V_{ds}$) 0.1V and 1V.**

The main reason behind this is that the drain current for linear region is ideal MOSFET where mobility is constant. For saturation region other device effects will affect the drain current, such as velocity saturation, channel length modulation, drain induced barrier lowering and parasitic S/D resistance. These effects were not modeled during the simulation therefore because the high difference of the drain currents. Equations below showed in red illustrate parts of the equations which were no considered. They simulate the following effects.

Parasitic S/D resistance:

$$I_{ds} = \frac{I_{ds0}}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right) \quad (4.4.1)$$

Velocity saturation:

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2V_t)}\right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}} \quad (4.4.2)$$

$V_A$, which account for channel length modulation (CLM) and drain-induced barrier lowering (DIBL):

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}\right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1} \quad (4.4.3)$$

The universal mobility model has become a norm against which engineers compare their mobility data. As mentioned, the "universal" property of the mobility is based on many assumptions. One need not be alarmed if the optimized U0 which best fits the I-V data of a

device is not close to 670 cm2/V-s (for NMOS). It is not uncommon to see values between 350 and 700 cm2/V-s. In fact, the U0 in a sample NMOS model card provided in the official BSIM3 website has a value of 388cm2/V-s. For the subthreshold region, the initial fitting is illustrate by figure 4.7 left), its shifted due to threshold voltage or short channel effects. The theoretical threshold voltages $V_{th,sub}$ for subthreshold current is different from the threshold voltage that is used to fit strong inversion I-V characteristics. Therefore BSIMSOI account this with Voff parameter, and the threshold voltage for subthreshold current is given by:

$$V_{th,sub} = V_{th} + V_{off} \qquad (4.4.4)$$

$V_{off}$ is determined experimentally from measured I-V characteristics and is expected to be negative. the recommended range for $V_{off}$ is between -0.06 and -0.12 V. For the KTH MOSFET the Voff is determined around -0.22 V. Figure 4.7 right) show the logarithmic plot of Ids versus Vgs with the consideration of Voff.

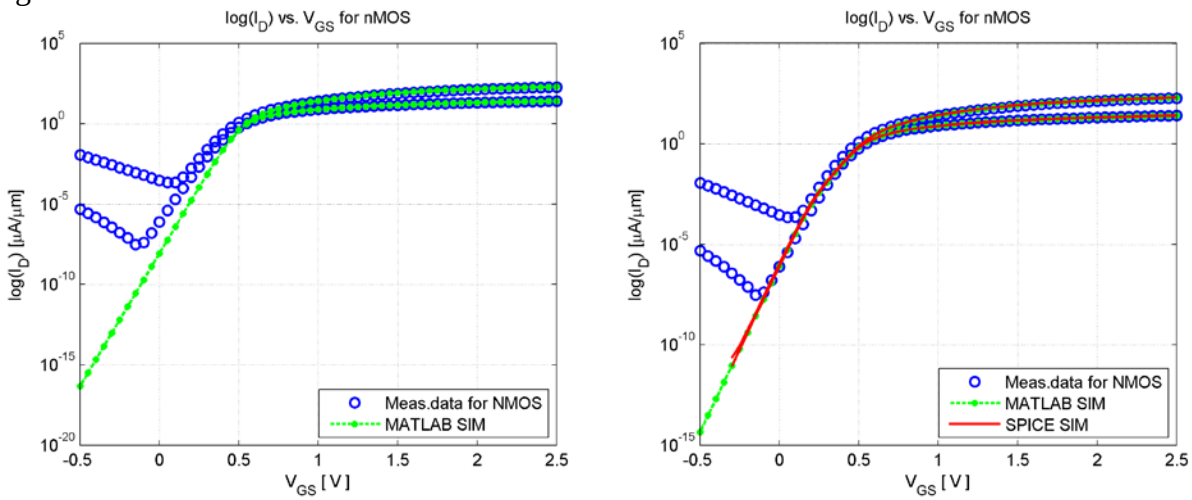


**Figure 4. 7. Drain current versus gate voltage at 0.1V and 1V drain voltage. (Symbols: Measurements; Dot Lines: Matlab simulation; Lines: Model simulated with Cadence)**

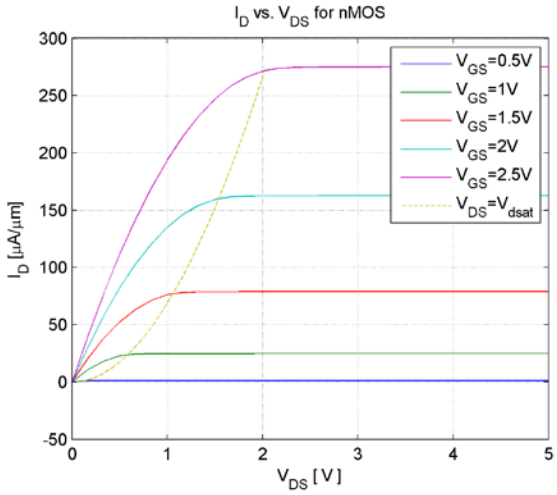


**Figure 4. 8: Drain current versus drain voltage for different front-gate bias.**

### 4.4.2 Result for PMOS

The results of PMOS are illustrated below in Matlab simulation.

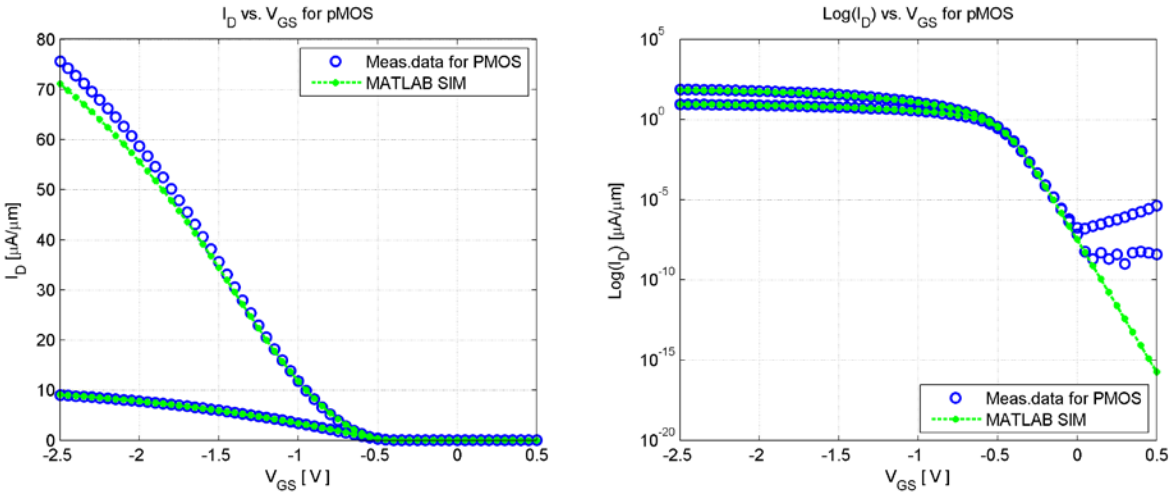


**Figure 4. 9. Measured and simulated $I_d$-$V_{gs}$ under different drain bias voltages ( $V_{ds}$) -0.1V and -1V. (Left figure) normal plot (Right figure) logarithmic plot**

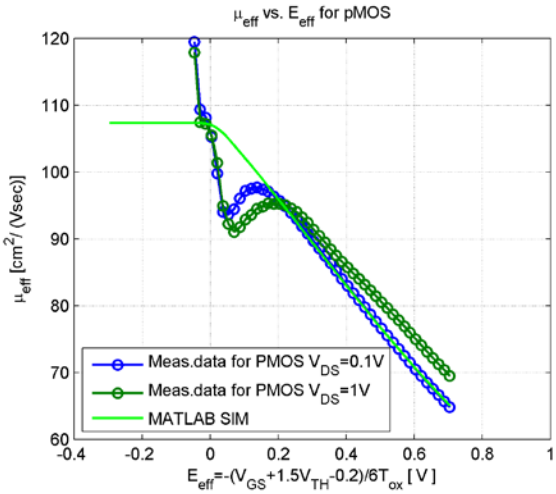


**Figure 4. 10. Mobility versus gate voltage for -0.1V and -1V drain bias**

### 4.4.3 Error analysis

The error between measurement data and simulation is calculated with the RMS Error equation below Mean absolute error and root mean square error:

$$R.A\ Error = \frac{1}{n}\sum_{i=1}^{n}\left(y_{sim\_i} - y_{meas\_i}\right)^2 \quad (4.4.5)$$

$$R.M.S\ Error = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(y_{sim\_i} - y_{meas\_i}\right)^2} \quad (4.4.6)$$

**Table 4. 4. Error analysis of the simulated drain current**

| NMOS | Matlab simulation data | | Cadence simulation data | |
|---|---|---|---|---|
| Drain Current | MA Error | RMS Error | MAE Error | RMS Error |
| Linear Vds=0.1V | 0.022 | 0.035 | 0.027 | 0.049 |
| Saturation Vds=1V | 4.050 | 5.855 | 4.469 | 6.468 |

The error in linear region and small $V_{gs}$ value of saturation is in good levels the square root of the mean/average of the square of all of the error. Another way to verify the simulation is to take the first derivate of ids vs Vgs curve, which gives the transconductance. Figure 4.11 compare the transconductance between the simulations and laboratory measurements.

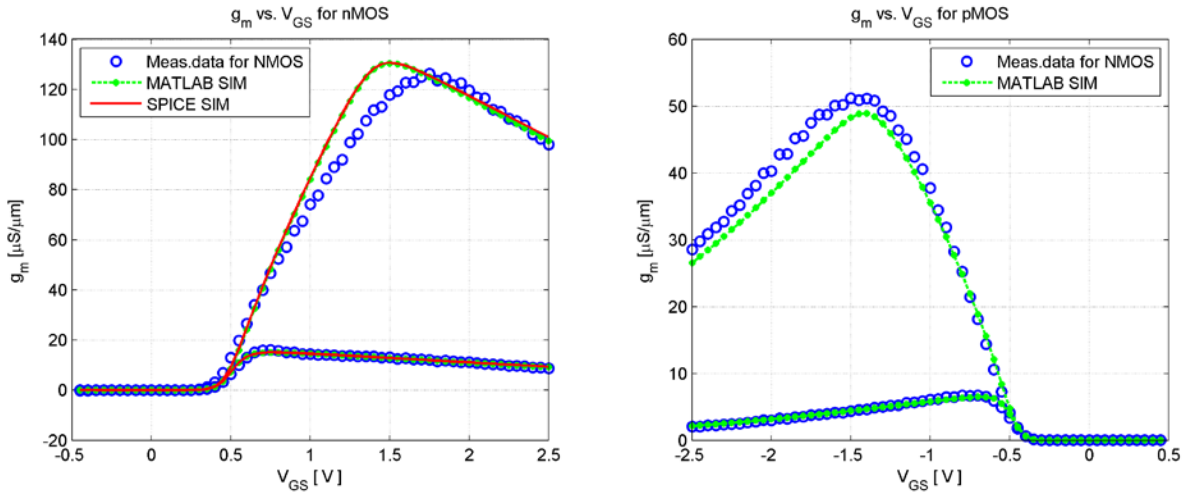


**Figure 4. 11. NMOS transconductance versus gate voltage at 0.1V and 1.0V drain voltage.**

**Table 4. 5. Error analysis of the simulated Transconductance**

| NMOS | Matlab simulation data | | Cadence simulation data | |
|---|---|---|---|---|
| Transconductance | MA Error | RMS Error | MAE Error | RMS Error |
| Linear Vds=0.1V | 0.206 | 0.329 | 0.227 | 0.350 |
| Saturation Vds=1V | 4.374 | 7.153 | 4.457 | 7.389 |

The higher error in Cadence is expected due to other default parameters are considered and cannot simply shut off in BSIMSOI.

# Chapter 5 Conclusion and Future work

In this section, the work of this paper is summarized and future work directions are suggested.

## 5.1 Conclusion

The semiconductor industry has made great progress since the creation of solid state transistor in 1947; great innovations are needed to ensure the continuity of Moore's law. As the transistor scaling becomes more difficult new technology arises, thin-body transistor structures such as FDSOI MOSFET and FinFET. Compact modeling is the bridge between the world of design and manufacturing, compact modeling of FDSOI and multi-gate FET is essential for future device fabrication.

This thesis focused on the modeling of KTH FDSOI transistor, with help of BSIMSOI compact model, a basic simulation result of I-V characteristic have been obtained. Nevertheless, the simulation fit only with some portion of KTH measurement. Therefore, more model parameters are needed to ensure the perfect fitting of the transistor.

## 5.2 Future work

UTBSOI MOSFET is an excellent candidate for advanced technology nodes, where superior control of short-channel effects. Furthermore there is a possibility where back-gate bias is introduced into UTBSOI, where double-gate is formed.

This thesis work covered the basic I-V characteristic of BSIMSOI compact model. The future work includes:

- Extraction of more models parameters
- C-V characteristics.

Although this work only discusses the BSIMSOI compact model for UTB MOSFETs, there is newer models such as BSIM-IMG. It's a production ready UTBSOI Model under standardization at Compact Model Council which may be more suitable for future modeling of UTBSOI.

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# Appendix A Matlab Code

This appendix contains the code written in MATLAB, which was used for parameter extraction.

## A.1 ExtractVth

This script of function is used to extract the threshold voltage for given type of mosfet, ids, vgs, and vds.

```
function [ Vth ] = ExtractVth( Type,Ids,Vgs,Vds )

clf
width = 5;     % Width in inches
height = 4;    % Height in inches
alw = 0.75;    % AxesLineWidth
fsz = 15;      % Fontsize
lw = 1.5;      % LineWidth
msz = 6;       % MarkerSize

if Type == 1;
Gm=diff(Ids);

[num idx] = max(Gm(:));
i = ind2sub(size(Gm),idx+1);

figure
[hAx,hLine1,hLine2] = plotyy(Vgs,Ids,Vgs(2:61),abs(Gm));

set(hLine1,'LineStyle','O','LineWidth',lw,'MarkerSize',msz)
set(hLine2,'LineStyle','O','LineWidth',lw,'MarkerSize',msz)

hold on

Slope = fit( Vgs(i-1:1:i+1), Ids(i-1:1:i+1), 'poly1');
hold on
c=coeffvalues(Slope);
plot(Slope);
grid on

VGs0=(-c(2)/c(1));

Vth=VGs0-0.5*Vds;

xlabel('V_{GS} [ V ]');
ylabel('I_D [ \muA/\mum ]');
y2label= get(hAx(2),'ylabel'); % name the second axis y-label
set(y2label,'String','g_m [ \muS/\mum ]')% the important part is 'String' to
recognize the text that follows


title('I_D vs. V_{GS} for nMOS');
% Move the legend to the top left corner.
h = legend( 'I_{ds} vs V_{gs}','Slope','g_{m} vs V_{gs}','Location',
```

```
'NorthWest' );

% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);

% Save the file as PNG
print('NMOSVth','-dpng','-r300');
else
Gm=diff(Ids);

[num idx] = max(Gm(:));
i = ind2sub(size(Gm),idx+1);

figure
[hAx,hLine1,hLine2] = plotyy(Vgs,Ids,Vgs(2:61),abs(Gm));

set(hLine1,'LineStyle','O','LineWidth',lw,'MarkerSize',msz)
set(hLine2,'LineStyle','O','LineWidth',lw,'MarkerSize',msz)

hold on
Slope = fit( Vgs(i-1:1:i+1), Ids(i-1:1:i+1), 'poly1');
hold on
c=coeffvalues(Slope);
plot(Slope);
grid on

VGs0=(-c(2)/c(1));

Vth=VGs0-0.5*Vds;

xlabel('V_{GS} [ V ]');
ylabel('I_D [ \muA/\mum ]');
y2label= get(hAx(2),'ylabel'); % name the second axis y-label
set(y2label,'String','g_m [ \muS/\mum ]')% the important part is 'String' to
recognize the text that follows


title('I_D vs. V_{GS} for pMOS');
% Move the legend to the top left corner.
h = legend( 'I_{ds} vs V_{gs}','Slope','g_{m} vs V_{gs}','Location',
'NorthEast' );

% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
```

```
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);

% Save the file as PNG
print('PMOSVth','-dpng','-r300');


return
end
```

### A.2 NMOS

This script fits the I-V measurement to the BSIMSOI model equations and extract the mobility parameters.

```
clear all, load Data.mat,load measurement.mat,  format long
% Vgs for NMOS: -0.5V to 2.5V
% Ids for NMOS @ Vds=0.1V

global NMOS_Idlin
global NMOS_Idsat

Vth=ExtractVth(1,NMOS_Idlin,VGn,0.1);

for i=25
i2=(61-i)+1;
for n1=10
for n2=20
for n3=30

Voff=-0.24;
Vds=0.1;
Idlin=NMOS_Idlin(i:61)*1e-6;
VGs=VGn(i:61);
 % Constants %
Tox = 5e-9;                 % Oxide Thickness [M]
T = 300;                    % Temperture [K]
q = 1.602176565e-19;        % [C]
kB = 1.3806488e-23;         % Boltzmanns Constant [eV/K]
vt = (kB*T)/q;              % Thermal Voltage [mV]
epsilon0  = 8.854e-12;       % [F/m]
epsilonox = 3.9 * epsilon0; % [F/m]
epsilonsi = 11.68 * epsilon0; % [F/m]
Cox = epsilonox/Tox;
W=1e-6;                     %[m]
L=1e-6;                     %[m]
delta = 0.01;               %

ni=1e16; %[cm^-3]
Nch=1e21; %[cm^-3]

phis=2*vt*log(Nch/ni);
sqrtphi = sqrt(phis)
```

```
Xdep=sqrt((2*epsilonsi)/(q*Nch))*sqrtphi;
Cdep=epsilonsi/Xdep;
Nfactor=1;
Cdsc=0;
Cit=0;
n=1+Nfactor*(Cdep/Cox)+(3*Cdsc)/Cox+Cit/Cox;


Esat=8e99;
Abulk=1;

% effective Vgs
Vgsteff= (2.*n.*vt.*log(1+exp((VGs-
Vth)/(2.*n.*vt)))./(1+2.*n.*Cox.*sqrt((2*phis)./(q.*epsilonsi.*Nch)).*exp(-
(VGs-Vth-2*Voff)./(2.*n.*vt)));
% saturation current
Vdsat = (Esat*L*(Vgsteff + 2*vt))./(Abulk*Esat*L+(Vgsteff + 2*vt));
%
Vdseff = Vdsat-0.5.*(Vdsat-Vds-delta+sqrt((Vdsat-Vds-
delta).^2+4*delta*Vdsat));
% mobility
ueff = Idlin./(Cox *(W/L) .* Vgsteff .* (1-(Vdseff./(2.*Vdsat))).* Vdseff);


% linear least square
n1= n1;
n2= n2;
n3= n3;
u1 = ((Vgsteff(n1) + 2*Vth)/Tox);
u2 = ((Vgsteff(n2) + 2*Vth)/Tox);
u3 = ((Vgsteff(n3) + 2*Vth)/Tox);
a=ueff(n1);
b=ueff(n2);
c=ueff(n3);
A=[1 -a*u1 -a*u1^2;
   1 -b*u2 -b*u2^2;
   1 -c*u3 -c*u3^2];
B=[ueff(n1);ueff(n2);ueff(n3)];
C=mldivide(A,B);

u0=C(1);
ua=C(2);
ub=C(3);
%x=[u0 ua ub]';
i2=(61-i)+1;
% u0=0.067; ua=1e-9; ub=1e-19;
x=[u0 ua ub]'

% Newton Raphson iteration +
for iter=1:5              % 5 iteration steps

    A=((Vgsteff+2*Vth)./Tox);

    f=u0-ueff-(ueff.*ua.*A)-(ueff.*ub.*A.^2);
```

```
    disp(norm(f));          % check that the norm(f) degrad to a minimum

    J=[ones(i2,1) -ueff.*A  -ueff.*A.^2];

    dx=-J\f; x=x+dx;

    u0=x(1); ua=x(2); ub=x(3);

end

Vth

x, iter


% calculate the Id
Vgsteff= (2.*n.*vt.*log(1+exp((VGn-
Vth)/(2.*n.*vt)))./(1+2.*n.*Cox.*sqrt((2*phis)./(q.*epsilonsi.*Nch)).*exp(-
(VGn-Vth-2*Voff)./(2.*n.*vt)));
Vdsat = Vgsteff + 2*vt;
Vdseff = Vdsat-0.5.*(Vdsat-Vds-delta+sqrt((Vdsat-Vds-
delta).^2+4*delta*Vdsat));
ueff1=u0./(1+ua.*((Vgsteff+2*Vth)./Tox)+ub.*(((Vgsteff+2*Vth)./Tox).^2));
Id1 = ueff1.*(Cox *(W/L) .* Vgsteff.* (1-(Vdseff./(2.*Vdsat))).* Vdseff)./1e-
6;

Vds1=1;
Vdseff = Vdsat-0.5.*(Vdsat-Vds1-delta+sqrt((Vdsat-Vds1-
delta).^2+4*delta*Vdsat));
Id2 = ueff1.*(Cox *(W/L) .* Vgsteff.* (1-(Vdseff./(2.*Vdsat))).* Vdseff)./1e-
6;


% calculate errors
difflin=NMOS_Idlin-(Id1);
diffsimlin=NMOS_Idlin-(lin35./1e-6);
diffsat=NMOS_Idsat-(Id2);
diffsimsat=NMOS_Idsat-(sat35./1e-6);

MAElin=mean(abs(difflin))
MAEsimlin=mean(abs(diffsimlin))
MAEsat=mean(abs(diffsat))
MAEsimsat=mean(abs(diffsimsat))

rmslin=sqrt(mean((difflin).^2))
rmssimlin=sqrt(mean((diffsimlin).^2))
rmssat=sqrt(mean((diffsat).^2))
rmssimsat=sqrt(mean((diffsimsat).^2))

output=[u01' ua1' ub1'];
u01(n1)=x(1);
ua1(n1)=x(2);
ub1(n1)=x(3);
```

```
PrintPNG(1,VGn,lin35./1e-6,sat35./1e-6,Id1,Id2)

end
end
end
end
```

### A.3 PrintPNG

this script of function is used to plot and export PNG file of the figures used in this paper.

```
function [ Y ] = PrintPNG(Type,VGn,Idlin,Idsat,Matlin,Matsat)
%UNTITLED3 Summary of this function goes here
%   Detailed explanation goes here

global NMOS_Idlin
global NMOS_Idsat
global PMOS_Idlin
global PMOS_Idsat

width = 5;     % Width in inches
height = 4;    % Height in inches
alw = 0.75;    % AxesLineWidth
fsz = 11;      % Fontsize
lw = 1.5;      % LineWidth
msz = 6;       % MarkerSize

% PMOS or NMOS, 1 = NMOS else is PMOS
if Type == 1;


% Semiplot
clf
measlin=semilogy(VGn,NMOS_Idlin,'bo','LineWidth',lw,'MarkerSize',msz);
hold on;
semilogy(VGn,NMOS_Idsat,'bo','LineWidth',lw,'MarkerSize',msz);
hold on;
matsim=semilogy(VGn,Matlin,'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
semilogy(VGn,Matsat,'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
spicesim=semilogy(VGn,Idlin,'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
semilogy(VGn,Idsat,'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
grid;
xlabel('V_{GS} [ V ]');
ylabel('log(I_D) [\muA/\mum]');
title('log(I_D) vs. V_{GS} for nMOS');
legend([measlin,matsim,spicesim],'Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','SouthEast');
% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
```

```
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);
% Save the file as PNG
print('NMOSsemiplot','-dpng','-r300');


% Normal Plot
clf
measlin=plot(VGn,NMOS_Idlin,'bo','LineWidth',lw,'MarkerSize',msz);
hold on;
plot(VGn,NMOS_Idsat,'bo','LineWidth',lw,'MarkerSize',msz);
hold on;
matsim=plot(VGn,Matlin,'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
plot(VGn,Matsat,'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
spicesim=plot(VGn,Idlin,'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
plot(VGn,Idsat,'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
grid;
xlabel('V_{GS} [ V ]');
ylabel('I_D [\muA/\mum]');
title('I_D vs. V_{GS} for nMOS');
legend([measlin,matsim,spicesim],'Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','NorthWest');
% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);
% Save the file as PNG
print('NMOSplot','-dpng','-r300');


% linear ids plot
clf
measlin=plot(VGn,NMOS_Idlin,'bo','LineWidth',lw,'MarkerSize',msz);
hold on;
matsim=plot(VGn,Matlin,'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
spicesim=plot(VGn,Idlin,'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
grid;
xlabel('V_{GS} [ V ]');
ylabel('I_D [\muA/\mum]');
title('I_D vs. V_{GS} for nMOS, V_{DS}=0.1V');
legend([measlin,matsim,spicesim],'Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','NorthWest');
```

```
% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);
% Save the file as PNG
print('NMOSlin','-dpng','-r300');


% plot of gm
clf
measlin=plot(VGn(1:60),diff(NMOS_Idlin),'bo','LineWidth',lw,'MarkerSize',msz)
;
hold on;
plot(VGn(1:60),diff(NMOS_Idsat),'bo','LineWidth',lw,'MarkerSize',msz);
hold on;
matsim=plot(VGn(1:60),diff(Matlin),'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
plot(VGn(1:60),diff(Matsat),'g--*','LineWidth',lw,'MarkerSize',4);
hold on;
spicesim=plot(VGn(1:60),diff(Idlin),'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
plot(VGn(1:60),diff(Idsat),'r-','LineWidth',lw,'MarkerSize',msz);
hold on;
grid;
xlabel('V_{GS} [ V ]');
ylabel('I_D [\muS/\mum]');
title('I_D vs. V_{GS} for nMOS');
legend([measlin,matsim,spicesim],'Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','NorthWest');
% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);
% Save the file as PNG
print('NMOSgm','-dpng','-r300');


% PMOS
else

semilogy(VGn,PMOS_Idlin,'bo',VGn,PMOS_Idsat,'bo',VGn,Matlin,'r-
',VGn,Matsat,'g-','LineWidth',lw,'MarkerSize',msz);
grid;
xlabel('V_{GS} [ V ]');
ylabel('Log(I_D) [\muA/\mum]');
title('I_D vs. V_{GS} for pMOS');
h = legend('Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','SouthWest');
```

```
% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);

% Save the file as PNG
print('PMOSsemiplot','-dpng','-r300');

clf

plot(VGn,PMOS_Idlin,'bo',VGn,PMOS_Idsat,'bo',VGn,Matlin,'r-',VGn,Matsat,'r-
','LineWidth',lw,'MarkerSize',msz);
grid;
xlabel('V_{GS} [ V ]');
ylabel('I_D [\muA/\mum]');
title('I_D vs. V_{GS} for pMOS');
h = legend('Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','NorthEast');

% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);

% Save the file as PNG
print('PMOSplot','-dpng','-r300');

clf

plot(VGn,PMOS_Idlin,'bo',VGn,Matlin,'r-','LineWidth',lw,'MarkerSize',msz);
grid;
xlabel('V_{GS} [ V ]');
ylabel('I_D [\muA/\mum]');
title('I_D vs. V_{GS} for nMOS, V_{DS}=0.1V');
h = legend('Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','NorthEast');

% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);
```

```
% Save the file as PNG
print('PMOSlin','-dpng','-r300');

clf

plot(VGn(1:60),diff(Matlin),'r-',VGn(1:60),diff(Matsat),'r-
',VGn(1:60),diff(PMOS_Idlin),'bo',VGn(1:60),diff(PMOS_Idsat),'bo','LineWidth'
,lw,'MarkerSize',msz);
grid;
xlabel('V_{GS} [ V ]');
ylabel('I_D [\muA/\mum]');
title('I_D vs. V_{GS} for pMOS');
h = legend('Meas.data for NMOS','MATLAB SIM','SPICE
SIM',4,'Location','NorthEast');

% Here we preserve the size of the image when we save it.
set(gcf,'InvertHardcopy','on');
set(gcf,'PaperUnits', 'inches');
papersize = get(gcf, 'PaperSize');
left = (papersize(1)- width)/2;
bottom = (papersize(2)- height)/2;
myfiguresize = [left, bottom, width, height];
set(gcf,'PaperPosition', myfiguresize);

% Save the file as PNG
print('PMOSgm','-dpng','-r300');
end
end
```

## Appendix B Cadence Simulation Parameter List

The parameter list below contains the essential ones which are used in this work, for full parameter list of BSIMSOI; please check the BSIMSOI user manual. Other parameters which is not included in this list is in default value.

| Symbol used in SPICE | Description | Unit | Default | Used in this work |
|---|---|---|---|---|
| soiMod | SOI model selector (instance) SoiMod=0: BSIMPD SoiMod=1: unified model for PD&FD. SoiMod=2: ideal FD. SoiMod=3: auto selection by BSIMSOI | | 0 | 1 |
| mobmod | Mobility model selector | | 1 | 1 |
| Tsi | Silicon film thickness | m | 1e-7 | 2e-8 |
| Tbox | Buried oxide thickness | m | 3e-7 | 1.45e-7 |
| tox | Gate oxide thickness | m | 1e-8 | 5e-9 |
| vth0 | Threshold voltage @$V_{bs}$=0 for long and wide device | | 0.7 | Vth extrated |
| k1 | First order body effect coefficient | | 0.6 | 0 |
| Dvt0 | first coefficient of short-channel effect on Vth | | 2.2 | 0 |
| dvt1 | Second coefficient of short-channel effect on Vth | | 2.2 | 0 |

| | | | | |
|---|---|---|---|---|
| u0 | Mobility at Temp = Tnom<br>NMOSFET<br>PMOSFET | $cm^2/(Vsec)$ | 670<br>250 | 258<br>121 |
| ua | First-order mobility degradation coefficient | m/V | 2.25e-9 | 3.3756e-10 |
| ub | Second-order mobility degradation coefficient | $(m/V)^2$ | 5.9e-19 | 5.5816e-19 |
| uc | Body-effect of mobility degradation coefficient | 1/V | -.0465 | 0 |
| vsat | Saturation velocity at Temp=Tnom | m/sec | 8e4 | 8e8 |
| voff | Offset voltage in the subthreshold region for large W and L | V | -0.08 | -0.22 |
| A0 | Bulk charge effect coefficient for channel length | | 1 | 0 |

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