## Computer Architectures Exam of 12/02/2025

## Question 2 (6 points)

Consider a processor connected to 128 KB of memory and equipped with a set-associative cache consisting of 8 sets of 4 lines each, for a total of 32 different lines, each of 32 bytes. Assuming that:

- The cache is initially not empty, and its configuration is reported in the Cache table.
- The adopted replacing algorithm is the Least Recently Used (LRU). In the Cache table, blocks are marked with an ascending label indicating when they were inserted or accessed. Specifically, the most recently used block is marked with 0, while the least recently used block is marked with 3.

Given the sequence of memory accesses shown in the Accesses table, determine the corresponding set and line being accessed. Use the Cache table to help you calculate the line involved in each operation. This way, you will get the final cache status. Finish by providing the total number of hits and misses that occurred.

## Accesses

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Block	Block (Binary)	Accessed Set	Accessed Line	H/M								
2633	1010 0100 1001											
345	0001 0101 1001											
1750	0110 1101 0110											
3675	1110 0101 1011											
677	0010 1010 0101											
995	0011 1110 0011											
854	0011 0101 0110											
4056	1111 1101 1000											
1860	0111 0100 0100											
117	0000 0111 0101											
818	0011 0011 0010											
3520	1101 1100 0000											
388	0001 1000 0100											
3093	1100 0001 0101											
167	0000 1010 0111											
1475	0101 1100 0011											
1359	0101 0100 1111											
1750	0110 1101 0110											
3594	1110 0000 1010											
808	0011 0010 1000											

## Cache

	Set 0			Set 2			Set 4			Set 6	
Line 0	0	3	Line 8	2698	0	Line 16	388	2	Line 24	774	1
Line 1	3520	1	Line 9	154	2	Line 17	3172	0	Line 25	2566	3
Line 2	4056	0	Line 10	818	1	Line 18	1492	3	Line 26	350	2
Line 3	2000	2	Line 11	3506	3	Line 19	1444	1	Line 27	1750	0
	Set 1			Set 3			Set 5			Set 7	
Line 4	257	3	Line 12	995	1	Line 20	117	0	Line 28	3239	2
Line 5	345	1	Line 13	2915	3	Line 21	677	2	Line 29	167	0
Line 6	3385	2	Line 14	1475	0	Line 22	3765	1	Line 30	1111	3
Line 7	2777	0	Line 15	579	2	Line 23	3493	3	Line 31	4007	1
Line /	2111										
Line /	2111	Ŭ	2000 10								

Number of hits: \_\_\_\_

Number of misses: