# Content Index



# Note

**NOTE 1:**
**Component parameter description**

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

**NOTE 2:**
Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.

**Bill of Materials**

**Header:**

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

**Combined property string:**

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note

Option

Description

Remind

| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 01.Index | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 1 of 21 |

这个页面可以由PCB LAYOUT工程师修改

| | |
|---|---|
| 散热片 | |
| 定位标记 | T1 MARK T2 MARK T3 MARK T4 MARK T5 MARK T6 MARK<br>MARK MARK MARK MARK MARK MARK |
| 序列号粘贴框 | PCBA SN H1 30X10 SN&MAC H2 10X10 |
| 板上字符 | 板卡编号 ZK3326-SB-V1 ZK3326-SB-V1 工程版本 A20xxx A20xxx 中科编号 SB_MB_PCBA_V10 SB_MB_PCBA_V10<br>SMT DIP ROHS H11 Signway H3 Pb-Free H4 防静电 |
| 定位孔 | H8 HOLE M2_2X4_5 H9 HOLE M2_2X4_5 H10 HOLE M2_2X4_5 |

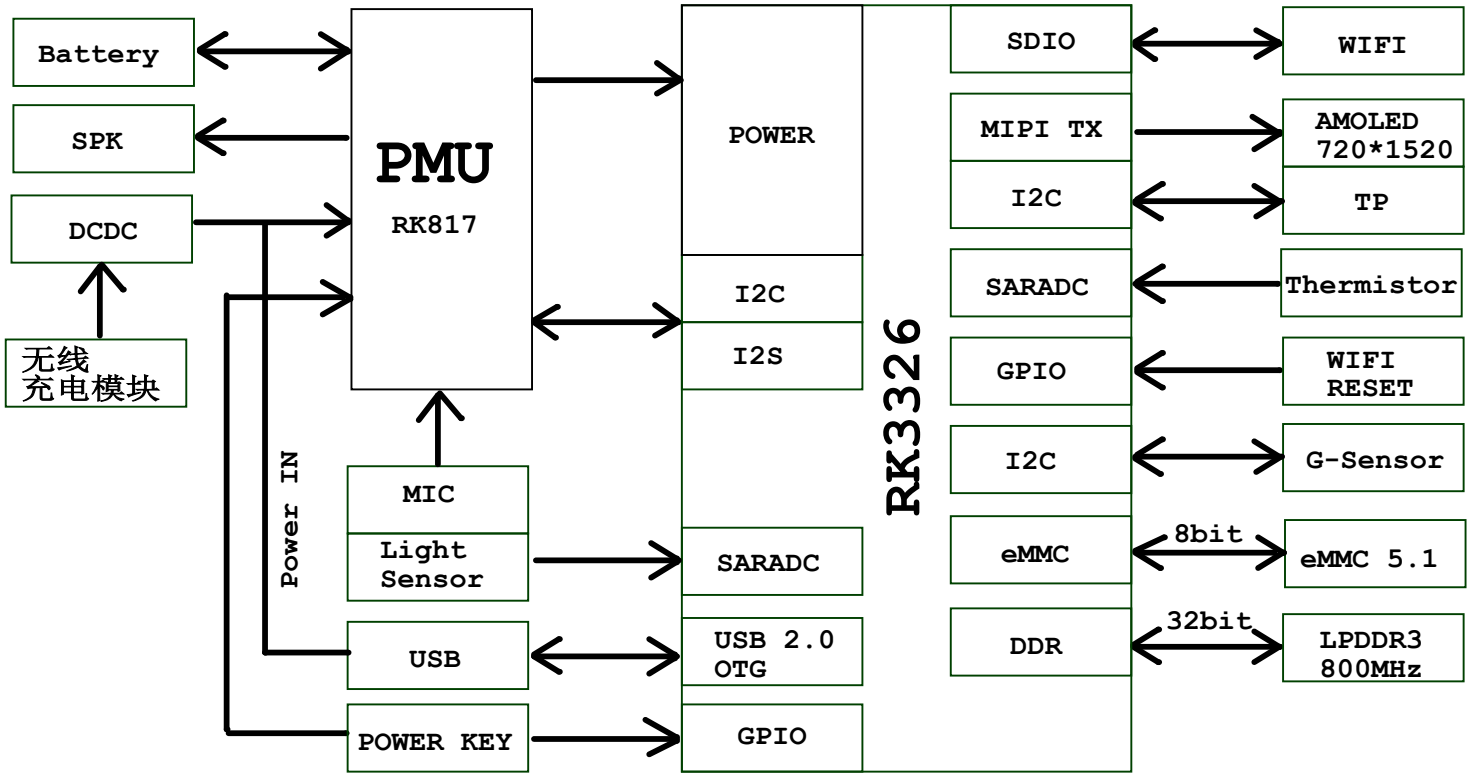
| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 02.Msc | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 2 of 21 |

# Revision History

| Version | Date | Author | Change Note | Approved |
|---|---|---|---|---|
| V1.0 | 2020.03.09 | YangYin | First Edition | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 03.Revision History | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 3 of 21 |

# Block Diagram




| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 04.Block Diagram | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 4 of 21 |

# I2C MAP

| Port | Pin name | Domain | Bus name | Pull-up voltage | Slave Device | Slave Addr (MS 7Bits) | Note | Slave Bus Capability |
|---|---|---|---|---|---|---|---|---|
| I2C0 | I2C0_SCL/GPIO0_B0_u<br>I2C0_SDA/GPIO0_B1_u | PMUIO2 | I2C0_SCL<br>I2C0_SDA | VCC3V0_PMU | Rockchip RK817 | 0x20 | PMIC | 100kHz,400kHz,1MHz |
| | | | | | | | | |
| I2C1 | I2C1_SCL/GPIO0_C2_u<br>I2C1_SDA/GPIO0_C3_u | PMUIO2 | I2C1_SCL<br>I2C1_SDA | VCC3V3 | GT9886 | 0xba | TP of MIPI Panel | 100kHz,400kHz |
| | | | | | LSM6DSL | 0xd4 | Accelerometer+Gyroscope | 100kHz,400kHz |
| I2C2 | I2C2_SCL/GPIO2_B7_u<br>I2C2_SDA/GPIO2_C0_u | VCCIO3 | I2C2_SCL<br>I2C2_SDA | VCC1V8_DVP | Not Used | | | |
| | | | | | Not Used | | | |

| | |
|---|---|
| Project: | RK3326_TABLET_REF |
| File: | 05.I2C MAP |
| Date: | Monday, March 16, 2020 |
| Rev: | <V1.0> |
| Designed by: | Yangyin |
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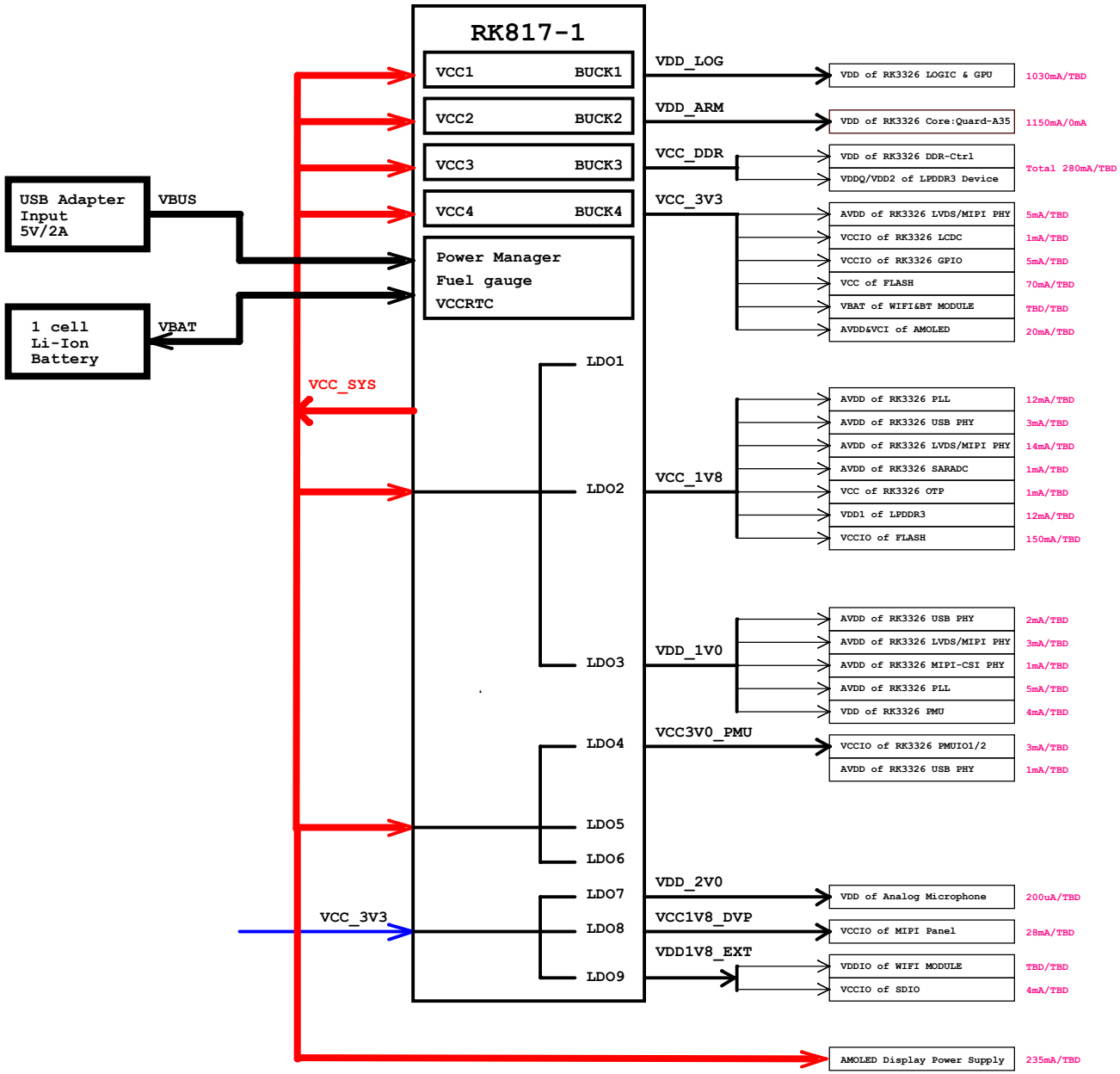
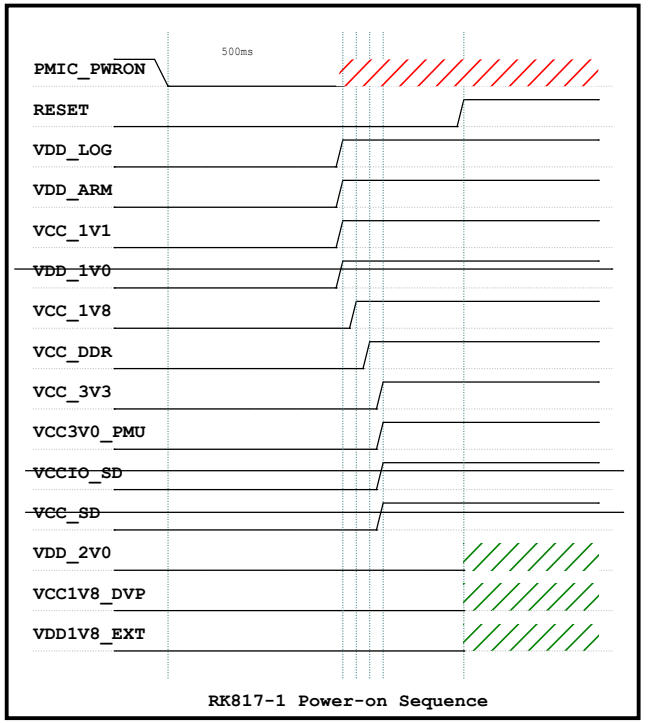
# RK817-1 Power Diagram and Sequence

Note:Power parameter shows the Peak value of system consumption.1st is normal work and 2nd is sleep mode.
功耗参数体现的是系统峰值功率，数据中的前者是工作状态峰值数据，后者是休眠状态峰值数据；




RK817-1 Power-on Sequence

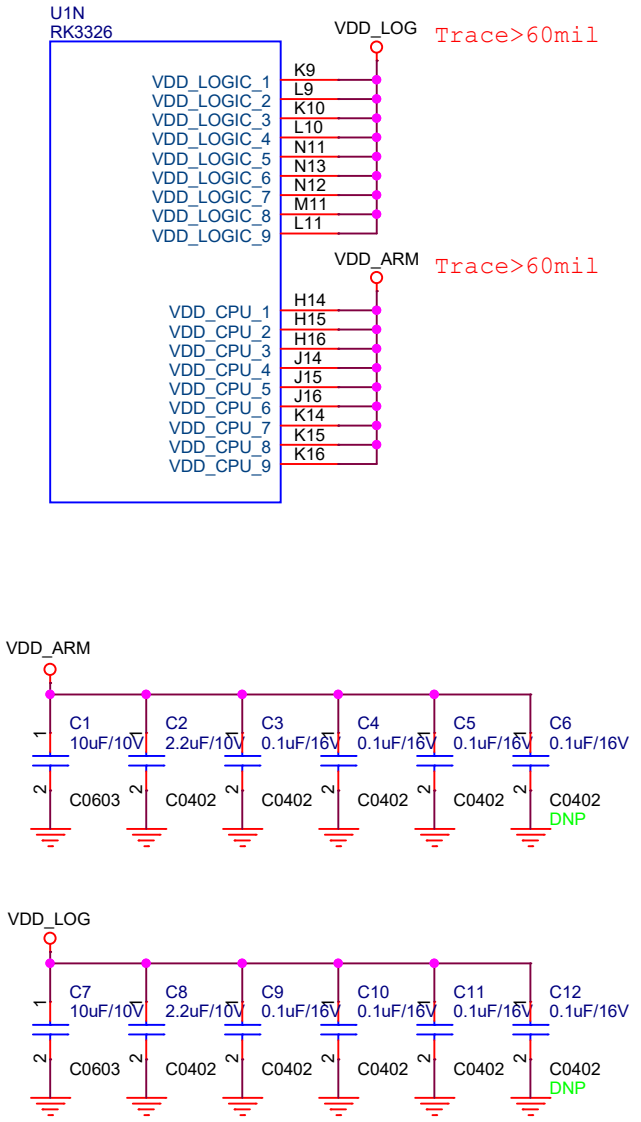
| PowerName | PMIC Channel | Time Slot (step 2mS) | Default voltage | Supply Limit | Default ON/OFF | Sleep ON/OFF |
|---|---|---|---|---|---|---|
| VDD_LOG | BUCK1 | Slot:1 | 1.1V | 2.5A | ON | OFF |
| VDD_ARM | BUCK2 | Slot:1 | 1.1V | 2.5A | ON | ON |
| VCC_DDR | BUCK3 | Slot:3 | FB=0.8V | 1.5A | ON | ON |
| VCC_3V3 | BUCK4 | Slot:4 | 3.0V | 1.5A | ON | ON |
| / | LDO1 | Slot:1 | 1.0V | 500mA | ON | ON |
| VCC_1V8 | LDO2 | Slot:2 | 1.8V | 500mA | ON | ON |
| VDD_1V0 | LDO3 | Slot:1 | 1.0V | 500mA | ON | ON |
| VCC3V0_PMU | LDO4 | Slot:4 | 3.0V | 100mA | ON | ON |
| / | LDO5 | Slot:4 | 3.0V | 500mA | ON | |
| / | LDO6 | Slot:4 | 3.0V | 500mA | ON | |
| VCC2V8_DVP | LDO7 | N/A | 2.8V | 500mA | OFF | OFF |
| VCC1V8_DVP | LDO8 | N/A | 1.8V | 500mA | OFF | OFF |
| VDD1V8_EXT | LDO9 | N/A | 1.5V | 500mA | OFF | OFF |
| RESET | RESETB | Slot:10 | OD | | | |




RK817-1 Power-on Sequence

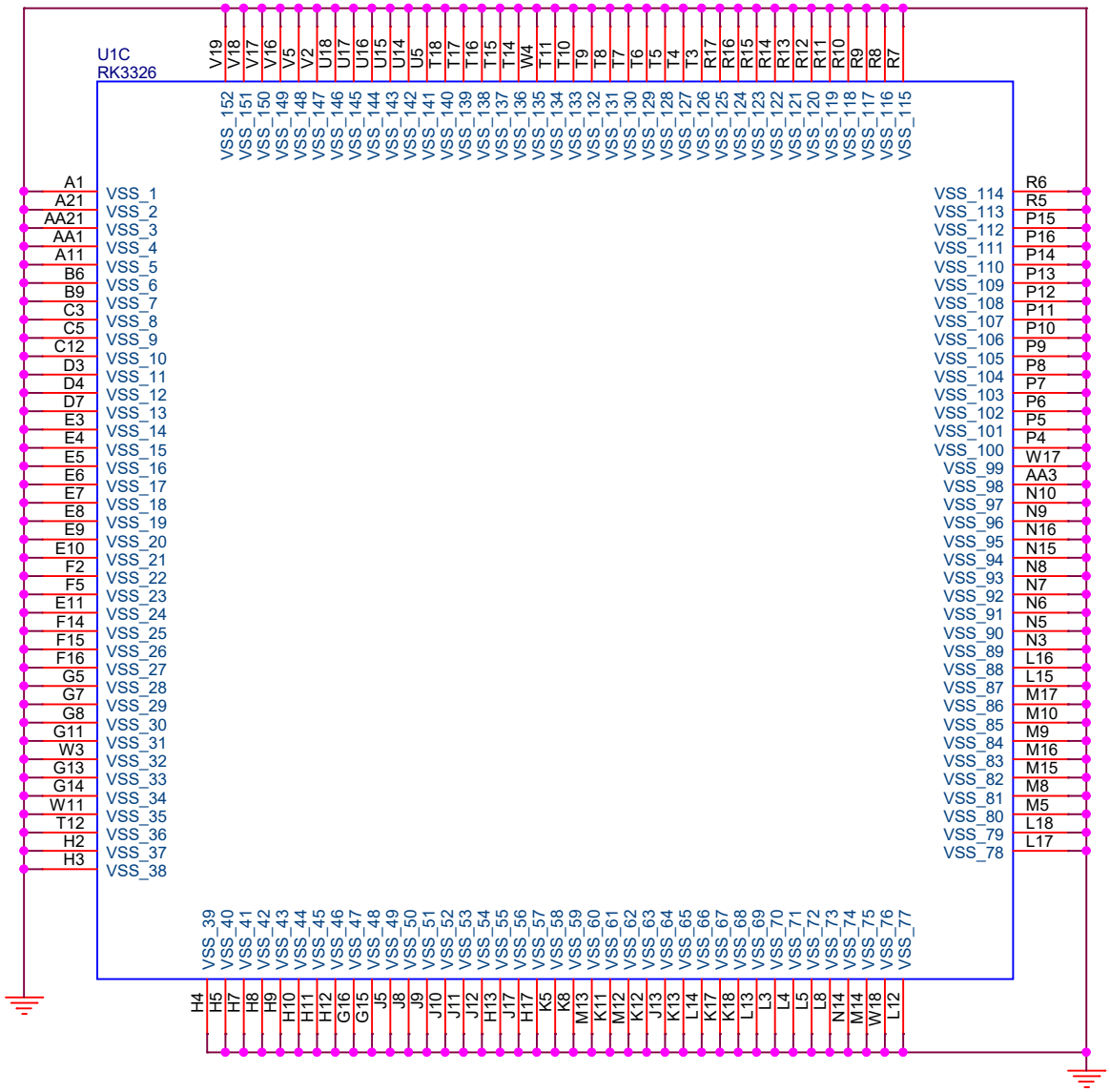
| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 06.Power Diagram and Sequence | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 6 of 21 |

# RK3326 Part-N



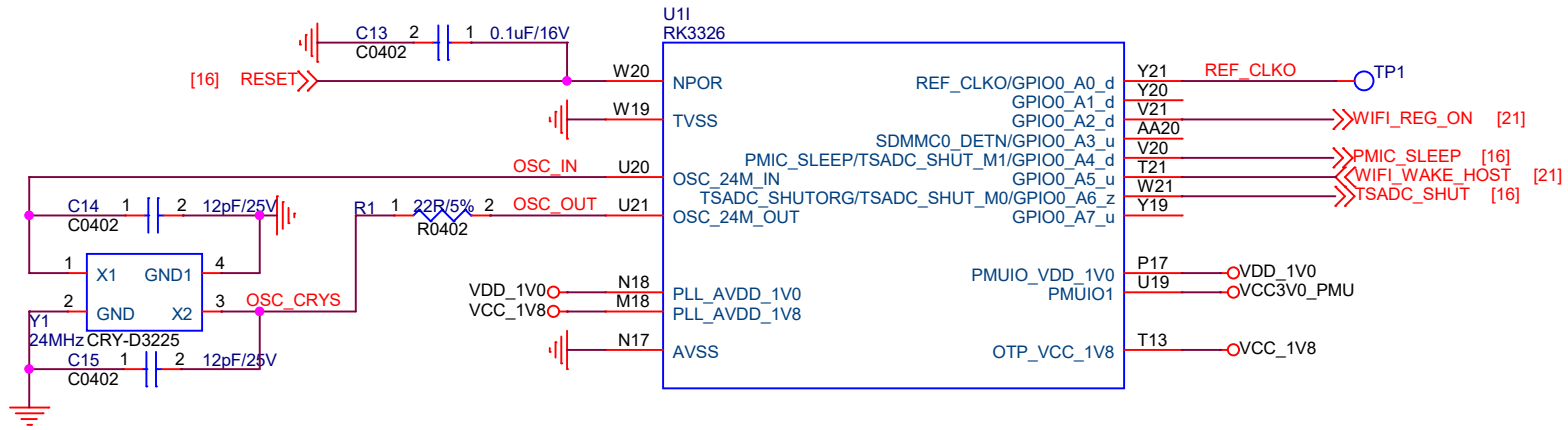

Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

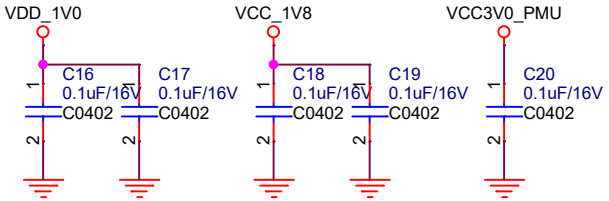
# RK3326 Part-C




| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 07.RK3326 Power | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 7 of 21 |

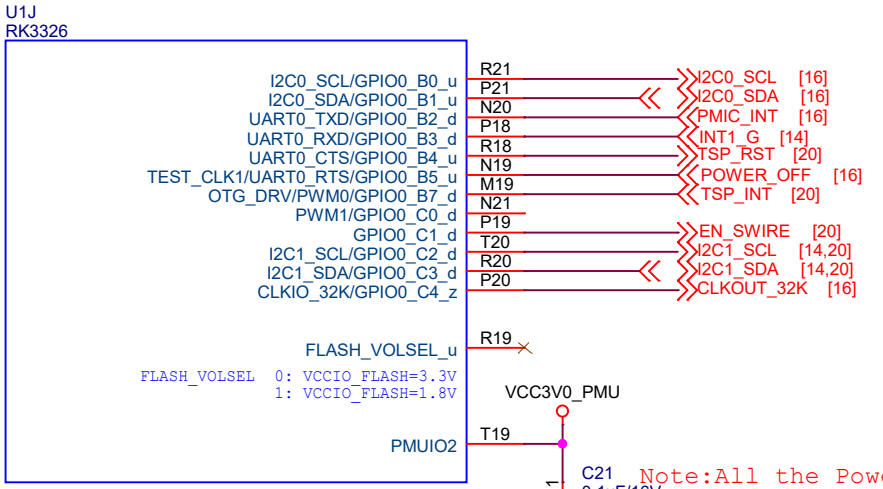
# RK3326 Part-I



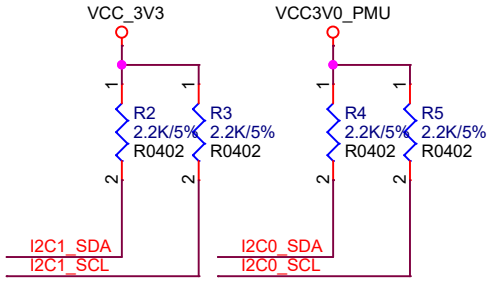




Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

# RK3326 Part-J




Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

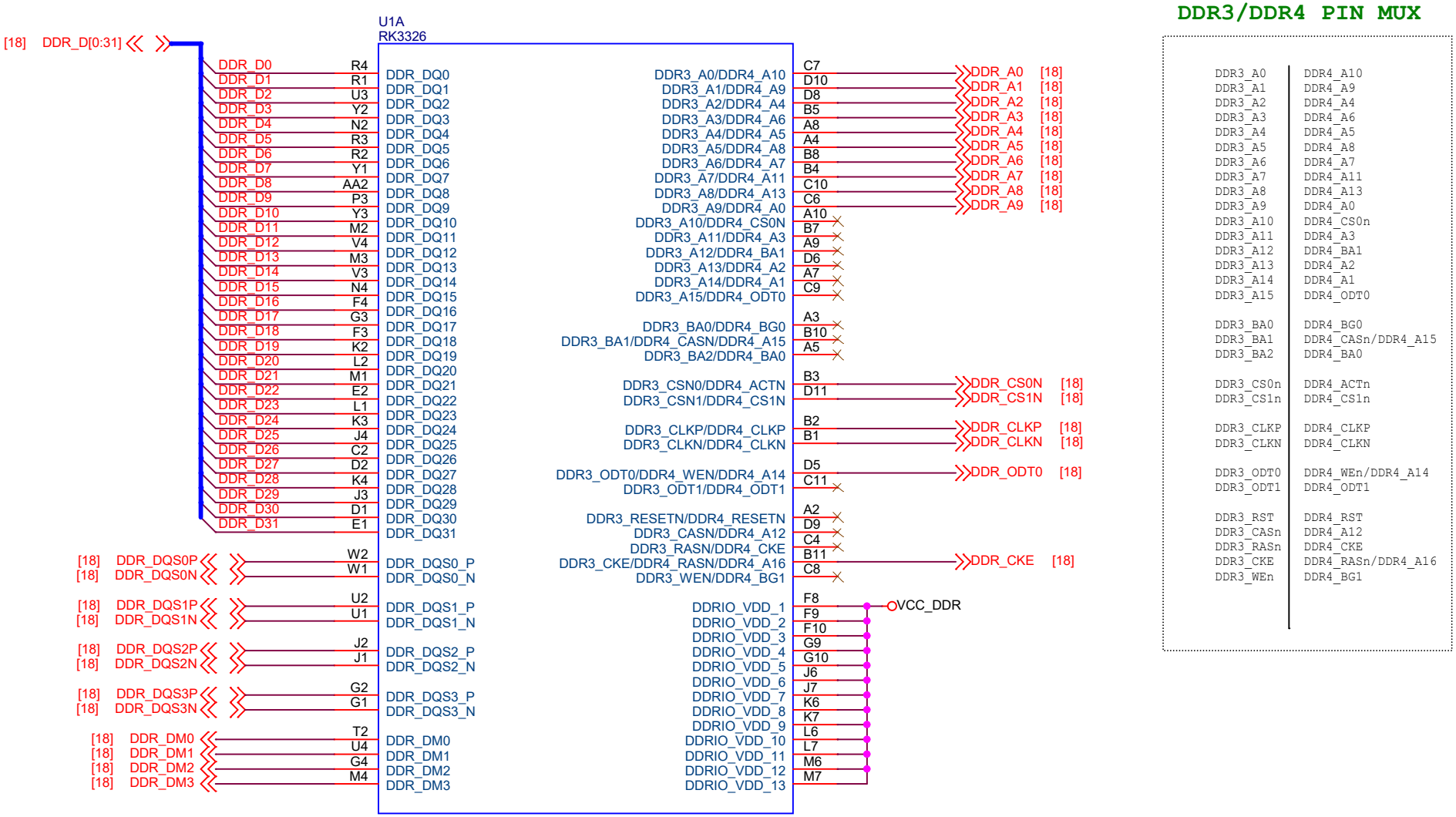



Note:

| | |
|---|---|
| Floating or Pull-up FLASH_VOLSEL=1 | Pull-down FLASH_VOLSEL=0 |
| VCCIO_FLASH=1.8V | VCCIO_FLASH=3.3V |

| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 08.RK3326 OSC/PMUIO1/PMUIO2 | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 8 of 21 |

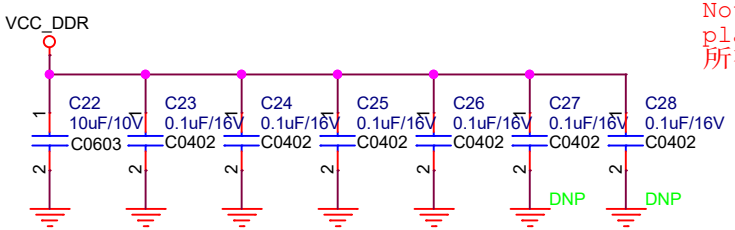
# RK3326 Part-A




## DDR3/DDR4 PIN MUX

| | |
|---|---|
| DDR3_A0 | DDR4_A10 |
| DDR3_A1 | DDR4_A9 |
| DDR3_A2 | DDR4_A4 |
| DDR3_A3 | DDR4_A6 |
| DDR3_A4 | DDR4_A5 |
| DDR3_A5 | DDR4_A8 |
| DDR3_A6 | DDR4_A7 |
| DDR3_A7 | DDR4_A11 |
| DDR3_A8 | DDR4_A13 |
| DDR3_A9 | DDR4_A0 |
| DDR3_A10 | DDR4_CS0n |
| DDR3_A11 | DDR4_A3 |
| DDR3_A12 | DDR4_BA1 |
| DDR3_A13 | DDR4_A2 |
| DDR3_A14 | DDR4_A1 |
| DDR3_A15 | DDR4_ODT0 |
| DDR3_BA0 | DDR4_BG0 |
| DDR3_BA1 | DDR4_CASn/DDR4_A15 |
| DDR3_BA2 | DDR4_BA0 |
| DDR3_CS0n | DDR4_ACTn |
| DDR3_CS1n | DDR4_CS1n |
| DDR3_CLKP | DDR4_CLKP |
| DDR3_CLKN | DDR4_CLKN |
| DDR3_ODT0 | DDR4_WEn/DDR4_A14 |
| DDR3_ODT1 | DDR4_ODT1 |
| DDR3_RST | DDR4_RST |
| DDR3_CASn | DDR4_A12 |
| DDR3_RASn | DDR4_CKE |
| DDR3_CKE | DDR4_RASn/DDR4_A16 |
| DDR3_WEn | DDR4_BG1 |

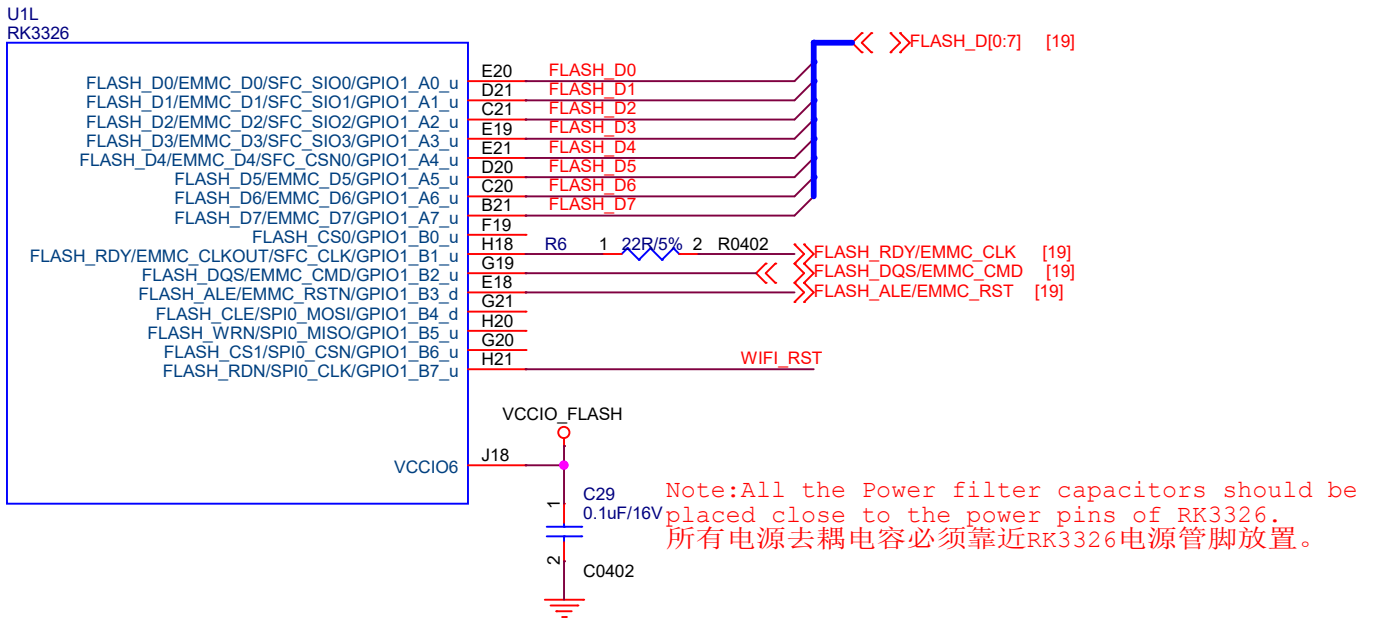
# Power Filter



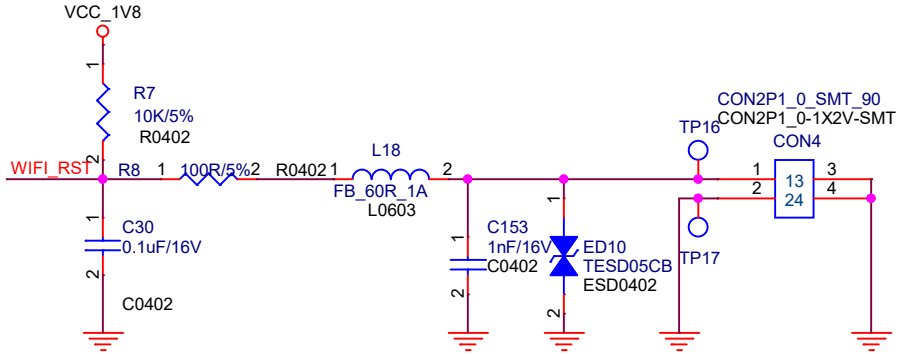

Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 09.RK3326 DDR Controller | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 9 of 21 |

# RK3326 Part-L



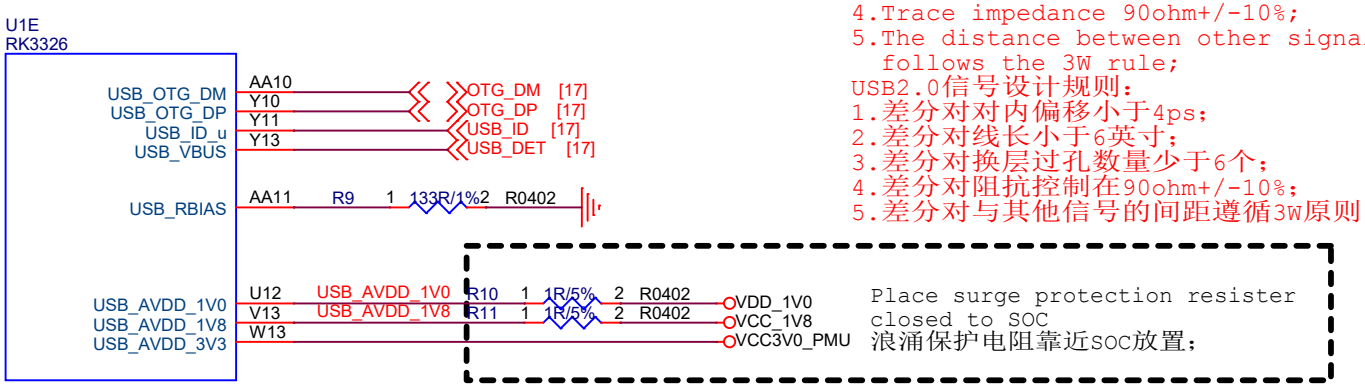

Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。



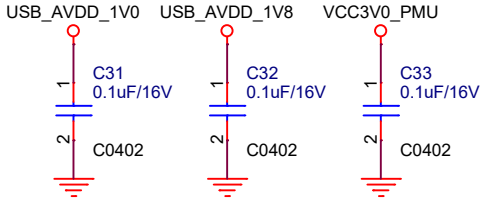

WiFi reset key

| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 10.RK3326 FLASH Controller | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 10 of 21 |

# RK3326 Part-E




USB2.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;
USB2.0信号设计规则：
1.差分对对内偏移小于4ps；
2.差分对线长小于6英寸；
3.差分对换层过孔数量少于6个；
4.差分对阻抗控制在90ohm+/-10%；
5.差分对与其他信号的间距遵循3W原则；




Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 11.RK3326 USB Controller | | |
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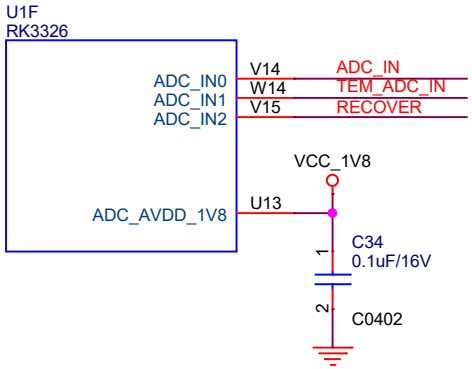
| Designed by: | Yangyin | Sheet: | 11 of 21 |

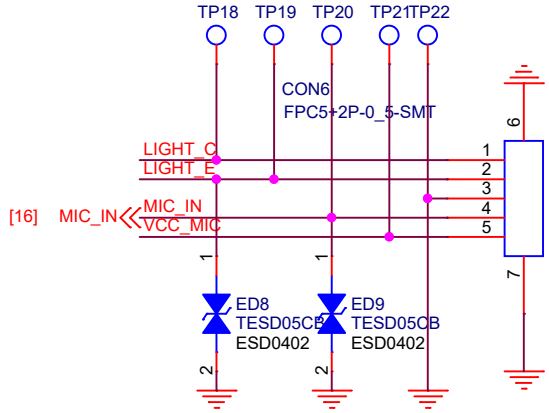
# RK3326 Part-F

Note:
Reserve ADC_IN2 for firmware update.If ADC2_KEY_IN=0V at power-on reset,then system will enter into Recovery/Loader mode.
预留ADC_IN2用于固件升级，上电复位情况下如果ADC2_KEY_IN为低电平，系统会进入Recovery/Loader模式。

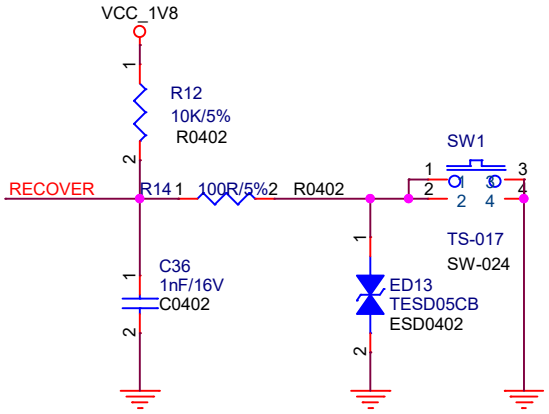



SARADC design rules:
1.The distance between other signals follows the 3W rule;
SARADC信号设计规则：
1.差分对与其他信号的间距遵循3W原则；

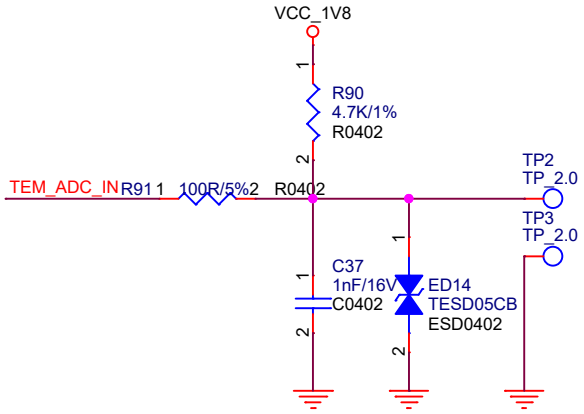
Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。



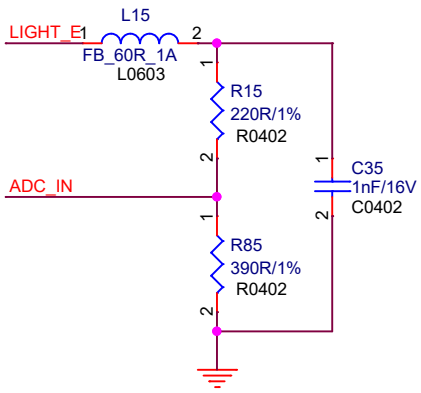

Mic&Light Sensor Interface



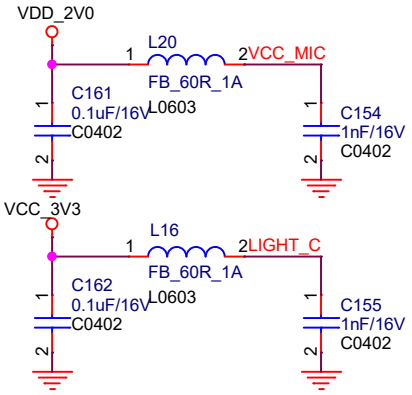

Recovery按键




Thermistor

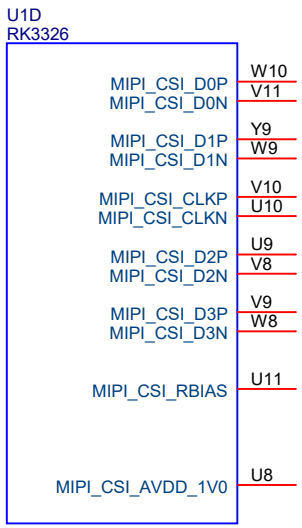



Light Sensor




| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 12.RK3326 SARADC | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 12 of 21 |

# RK3326 Part-D

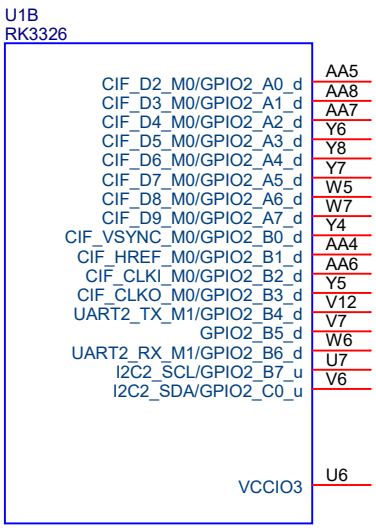



Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

MIPI信号设计规则:
1.差分对对内偏移小于4ps;
2.Clk与Data的差分对组间偏移小于7ps;
3.差分对线长小于7.2英寸;
4.差分对换层过孔数量少于4个;
5.差分对阻抗控制在100ohm+/-10%;
6.差分对与其他信号的间距遵循3W原则;

# RK3326 Part-B




Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 13.RK3326 DVP Interface | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
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# RK3326 Part-M

U1M
RK3326

| | | |
|---|---|---|
| LVDS/MIPI_TX_D0N/LCDC_D11_M1 | B16 | MIPI_TXD0N [20] |
| LVDS/MIPI_TX_D0P/LCDC_D8_M1 | B17 | MIPI_TXD0P [20] |
| LVDS/MIPI_TX_D1N/LCDC_D1_M1 | B15 | MIPI_TXD1N [20] |
| LVDS/MIPI_TX_D1P/LCDC_D10_M1 | A16 | MIPI_TXD1P [20] |
| LVDS/MIPI_TX_CLKN/LCDC_D4_M1 | B14 | MIPI_TXCLKN [20] |
| LVDS/MIPI_TX_CLKP/LCDC_D3_M1 | A14 | MIPI_TXCLKP [20] |
| LVDS/MIPI_TX_D2N/LCDC_VSYNC_M1 | C13 | MIPI_TXD2N [20] |
| LVDS/MIPI_TX_D2P/LCDC_D5_M1 | B13 | MIPI_TXD2P [20] |
| LVDS/MIPI_TX_D3N/LCDC_HSYNC_M1 | B12 | MIPI_TXD3N [20] |
| LVDS/MIPI_TX_D3P/LCDC_DEN_M1 | A12 | MIPI_TXD3P [20] |
| LCDC_CLK/GPIO3_A0_d | D19 | R81 1 22R/5% 2 R0402 ERR_FG [20] |
| UART5_RXD/I2S2_2CH_MCLK/LCDC_HSYNC_M0/GPIO3_A1_d | E13 | R82 1 22R/5% 2 R0402 LCD_TE [20] |
| UART5_TXD/I2S2_2CH_SCLK/LCDC_VSYNC_M0/GPIO3_A2_d | F13 | R83 1 22R/5% 2 R0402 RESX [20] |
| UART5_CTS/I2S2_2CH_LRCK/CIF_D2_M1/LCDC_DEN_M0/GPIO3_A3_d | E14 | |
| LCDC_D0/GPIO3_A4_d | C15 | |
| UART5_RTS/I2S2_2CH_SDI/CIF_D3_M1/LCDC_D1_M0/GPIO3_A5_d | E15 | |
| LCDC_D2/GPIO3_A6_d | C14 | |
| I2S2_2CH_SDO/CIF_D4_M1/LCDC_D3_M0/GPIO3_A7_d | E16 | |
| I2S0_8CH_SDI3/CIF_D5_M1/LCDC_D4_M0/GPIO3_B0_d | E17 | |
| SPI1_CSN0/I2S0_8CH_SDI2/CIF_D6_M1/LCDC_D5_M0/GPIO3_B1_d | F17 | |
| SPI1_CSN1/LCDC_D6/GPIO3_B2_d | B18 | |
| I2S0_8CH_SDI1/LCDC_D7/GPIO3_B3_d | C17 | |
| SPI1_MOSI/I2S0_8CH_SCLKRX/CIF_D7_M1/LCDC_D8_M0/GPIO3_B4_d | F18 | |
| I2S0_8CH_LRCKRX/LCDC_D9/GPIO3_B5_d | C16 | |
| SPI1_MISO/I2S0_8CH_SDO3/CIF_D8_M1/LCDC_D10_M0/GPIO3_B6_d | G18 | |
| SPI1_CLK/I2S0_8CH_SDO2/CIF_D9_M1/LCDC_D11_M0/GPIO3_B7_d | G17 | |
| I2S0_8CH_SDO1/LCDC_D12/GPIO3_C0_d | A20 | |
| I2S0_8CH_MCLK/LCDC_D13/GPIO3_C1_d | B20 | |
| TDM_FSYNC/LCDC_D14/I2S0_8CH_LRCKTX/GPIO3_C2_d | C19 | |
| TDM_SCLK/I2S0_8CH_SCLKTX/LCDC_D15/GPIO3_C3_d | B19 | |
| TDM_SDO/I2S0_8CH_SDO0/LCDC_D16/GPIO3_C4_d | C18 | |
| TDM_SDI/I2S0_8CH_SDI0/LCDC_D17/GPIO3_C5_d | A18 | |
| PDM_CLK0_M0/LCDC_D18/GPIO3_C6_d | D13 | |
| PDM_CLK1/LCDC_D19/GPIO3_C7_d | D14 | |
| PDM_SDI1/CIF_CLKOUT_M1/LCDC_D20/GPIO3_D0_d | D15 | |
| ISP_PRELIGHT_TRIG/PDM_SDI2/CIF_VSYNC_M1/LCDC_D21/GPIO3_D1_d | D16 | |
| ISP_FLASH_TRIGOUT/PDM_SDI3/CIF_HREF_M1/LCDC_D22/GPIO3_D2_d | D17 | |
| ISP_FLASH_TRIGIN/PDM_SDI0_M0/CIF_CLKIN_M1/LCDC_D23/GPIO3_D3_d | D18 | |

LVDS_RBIAS — G12 — R20 1NC/2K/1% 2 R0402

Place surge protection resister closed to SOC
浪涌保护电阻靠近SOC放置；

| | | | |
|---|---|---|---|
| LVDS/MIPI_AVDD_1V0 | F11 | MIPI_DSI_VCCA_1V0 | R21 1 1R/5% 2 R0402 VDD_1V0 |
| LVDS/MIPI_AVDD_1V8 | F12 | MIPI_DSI_VCCA_1V8 | R22 1 1R/5% 2 R0402 VCC_1V8 |
| LVDS/MIPI_AVDD_3V3 | E12 | | VCC_3V3 |
| VCCIO4 | D12 | | R23 R0402 0R/5% VCC1V8_DVP |

LVDS/MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

MIPI信号设计规则:
1.差分对对内偏移小于4ps;
2.Clk与Data的差分对组间偏移小于7ps;
3.差分对线长小于7.2英寸;
4.差分对换层过孔数量少于4个;
5.差分对阻抗控制在100ohm+/-10%;
6.差分对与其他信号的间距遵循3W原则;

MIPI_DSI_VCCA_1V0 — C39 0.1uF/16V C0402
MIPI_DSI_VCCA_1V8 — C40 0.1uF/16V C0402
VCC_3V3 — C41 0.1uF/16V C0402

Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

[8,20] I2C1_SCL — R16 1 22R/5% 2 R0402
[8,20] I2C1_SDA — R17 1 22R/5% 2 R0402

U2
LSM6DSL
LGA14P0_5-3_0X2_5

VCC_3V3 — R18 R0402 0R/5%
[8] INT1_G

| | | | |
|---|---|---|---|
| 1 | SDO/SA0 | NC | 11 |
| 2 | SDx | NC1 | 10 |
| 3 | SCx | INT2 | 9 |
| 4 | INT1 | VDD | 8 |
| 5 | VDDIO | | |
| 6 | GND1 | | |
| 7 | GND | | |
| 12 | SDA | | |
| 13 | SCL | | |
| 14 | CS | | |

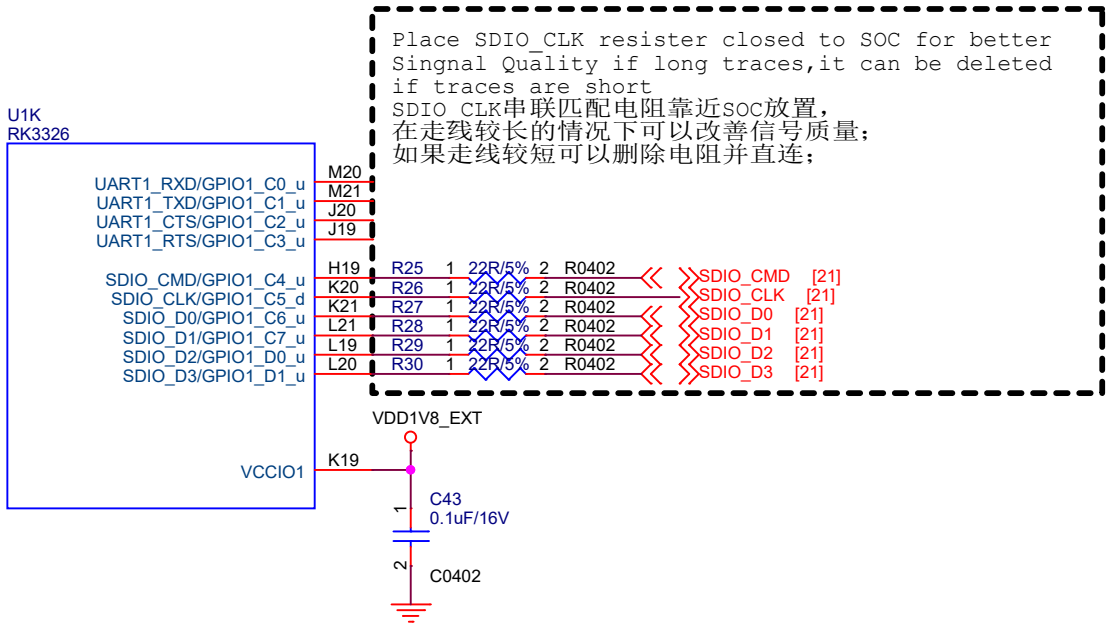
VDD — VCC_3V3

R19 1 22R/5% 2 R0402
C38 0.1uF/16V C0402

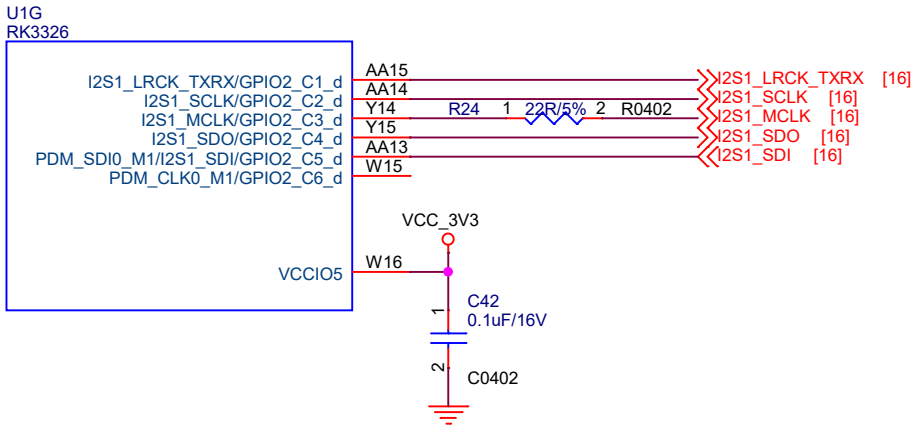
Gyroscope+G-sensor

| | |
|---|---|
| Project: | RK3326_TABLET_REF |
| File: | 14.RK3326 Display Interface |
| Date: | Monday, March 16, 2020 |
| Rev: | <V1.0> |
| Designed by: | Yangyin |
| Sheet: | 14 of 21 |

# RK3326 Part-K

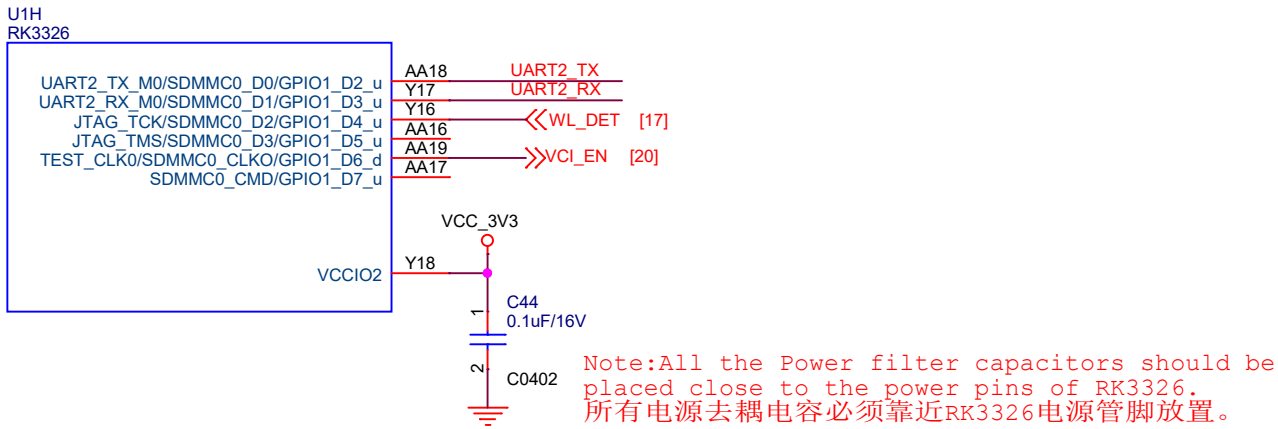



# RK3326 Part-G

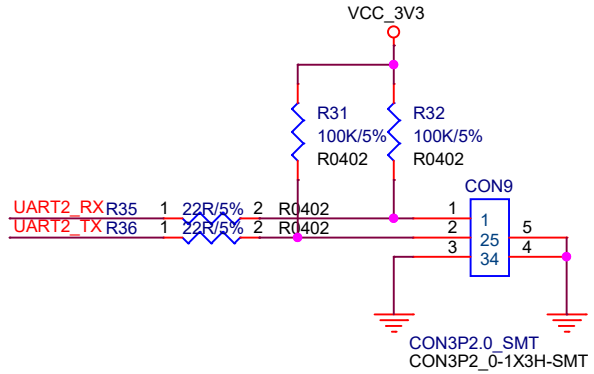



Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

# RK3326 Part-H

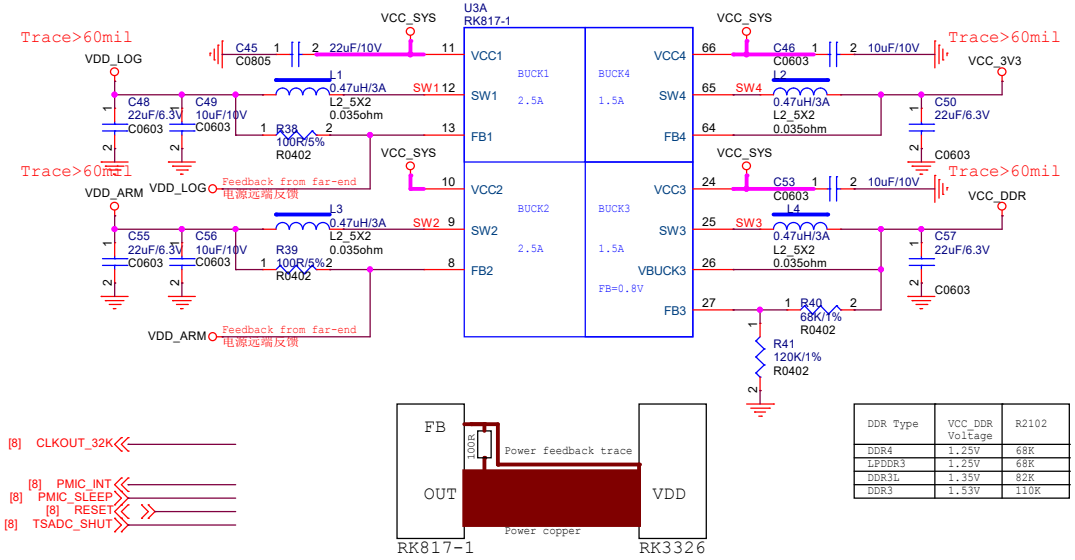



Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。



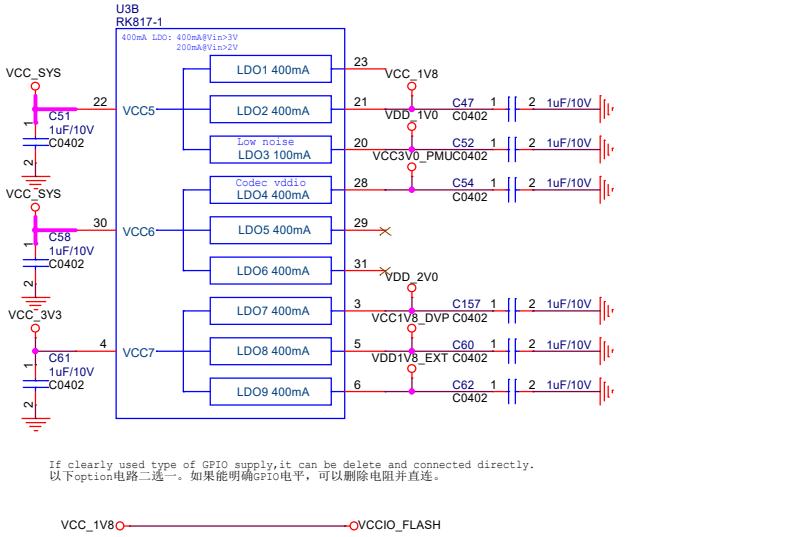

| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 15.RK3326 UART/SDIO/I2S/SDMMC | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 15 of 21 |

# PMIC RK817-1 DCDC

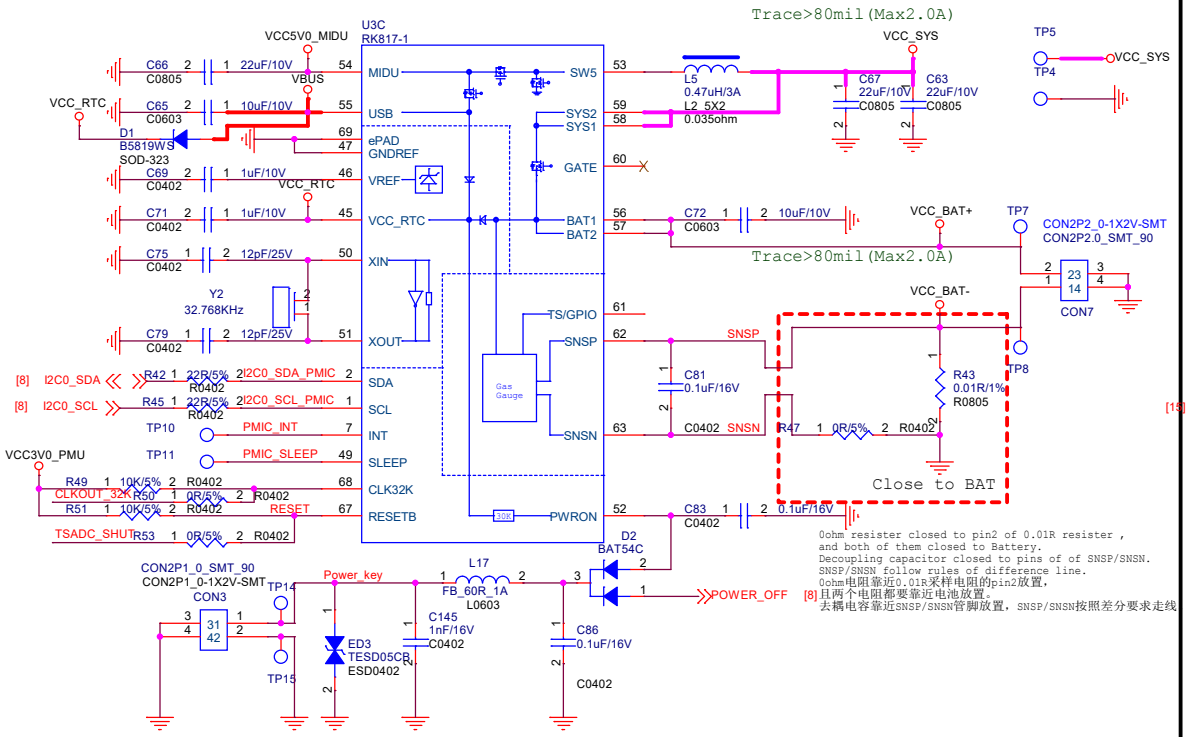



| DDR Type | VCC_DDR Voltage | R2102 |
|---|---|---|
| DDR4 | 1.25V | 68K |
| LPDDR3 | 1.25V | 68K |
| DDR3L | 1.35V | 82K |
| DDR3 | 1.53V | 110K |

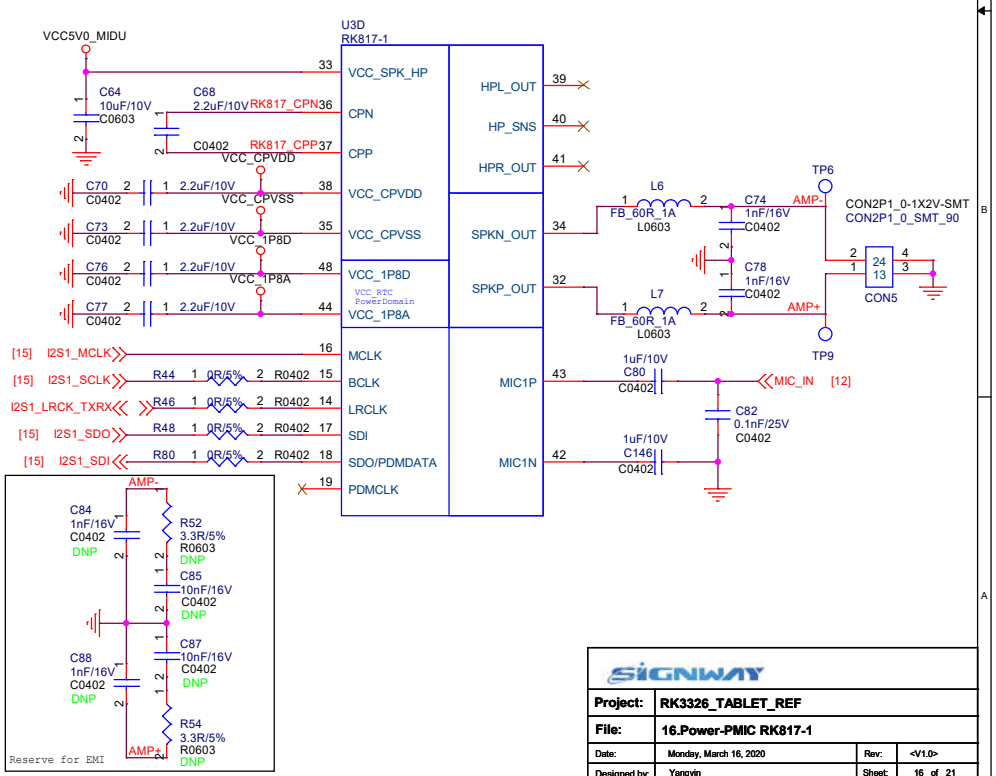
# PMIC RK817-1 LDO




# PMIC RK817-1 Managerment

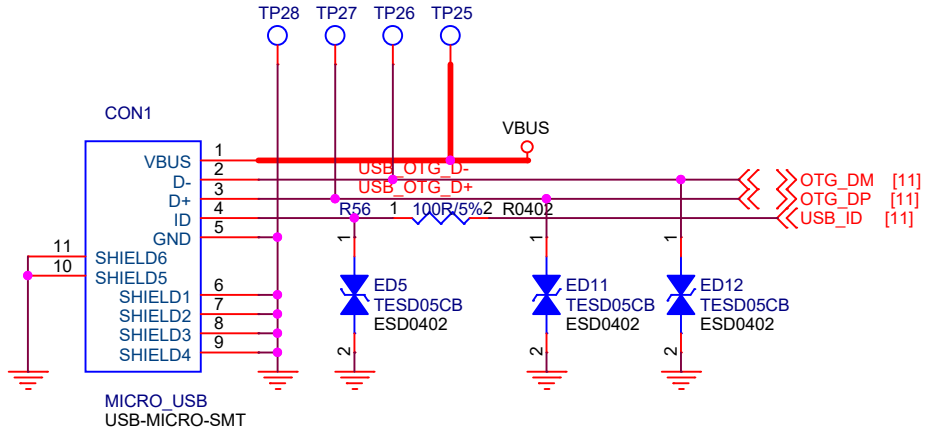


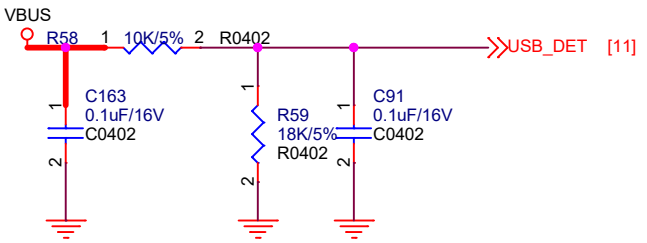

# PMIC RK817-1 CODEC

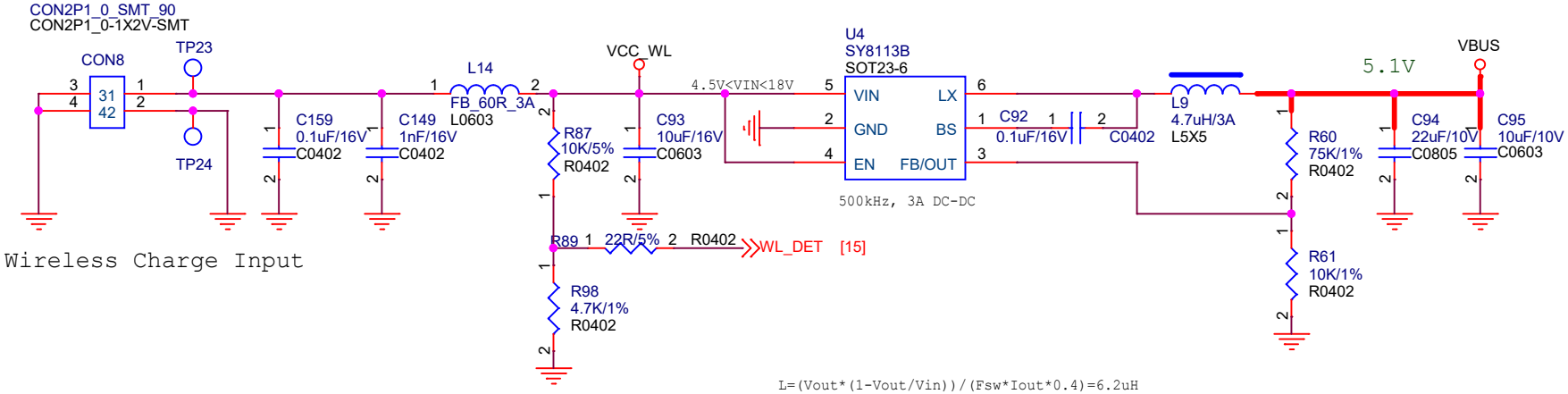



| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 16.Power-PMIC RK817-1 | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 16 of 21 |

# USB Port



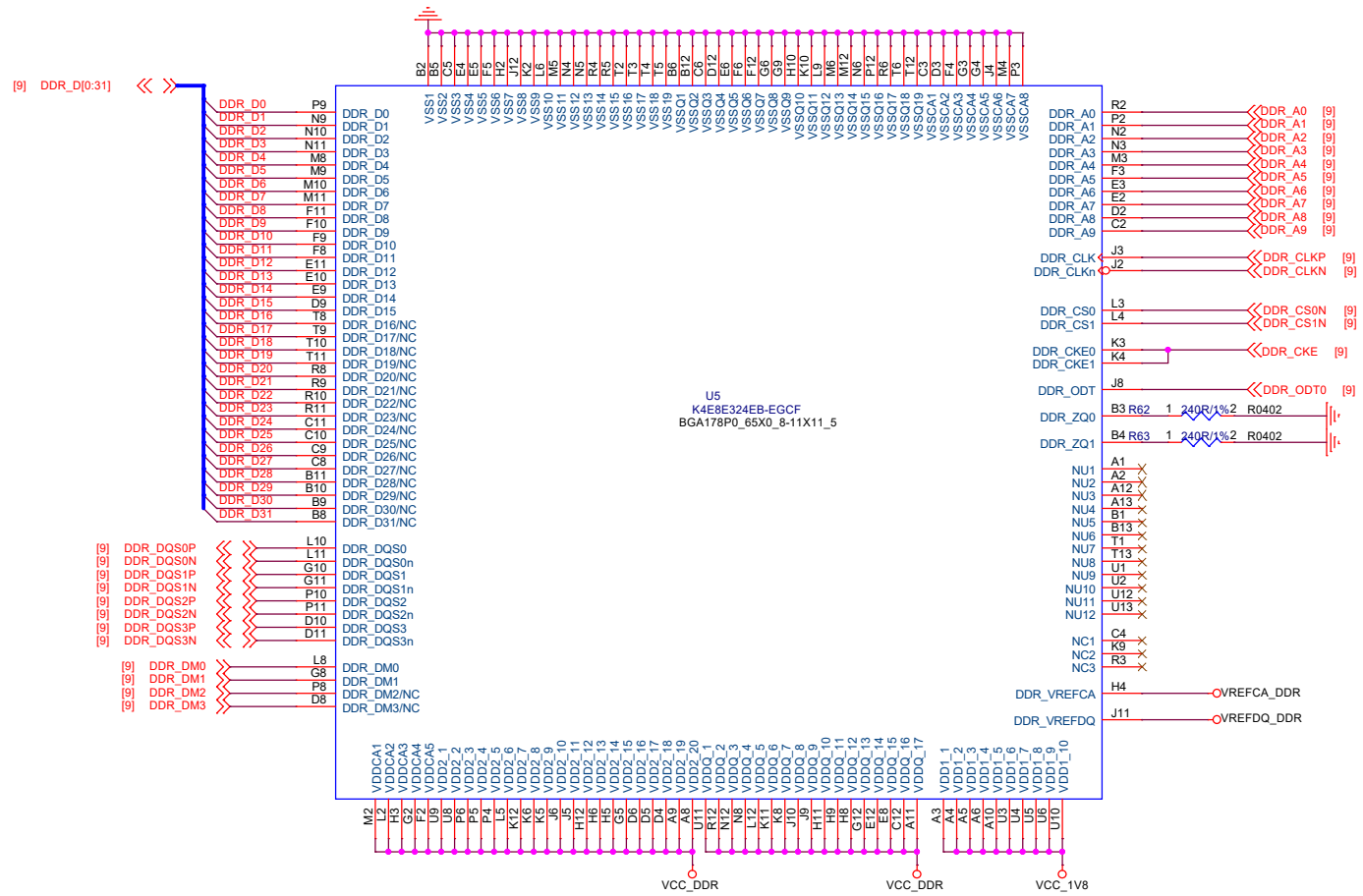



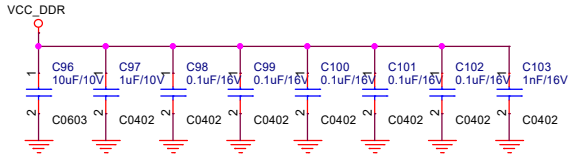



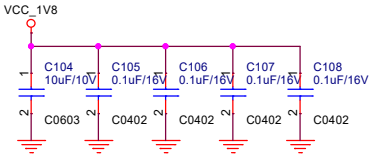

| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 17.USB Port&Power in | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 17 of 21 |

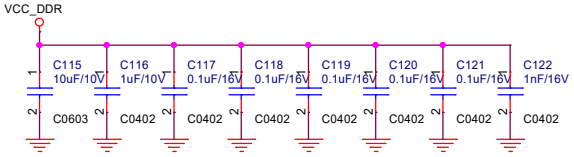
# LPDDR3 1x32bit

Note:The simulation frequency of the template is 800MHz.
**Remind: Refer to the latest AVL for parts selection.**

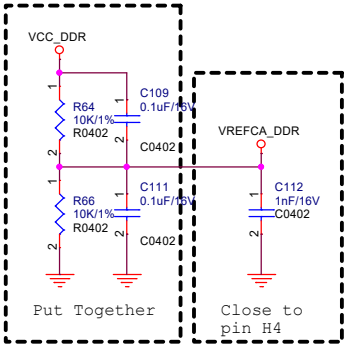


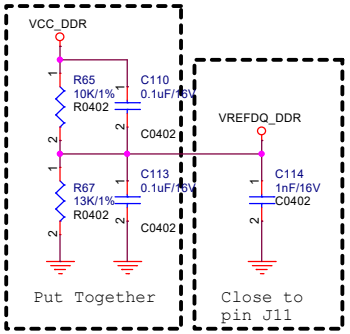




Note:All the Power filter capacitors should be placed close to the power pins of LPDDR3.
所有电源去耦电容必须靠近LPDDR3颗粒电源管脚放置。



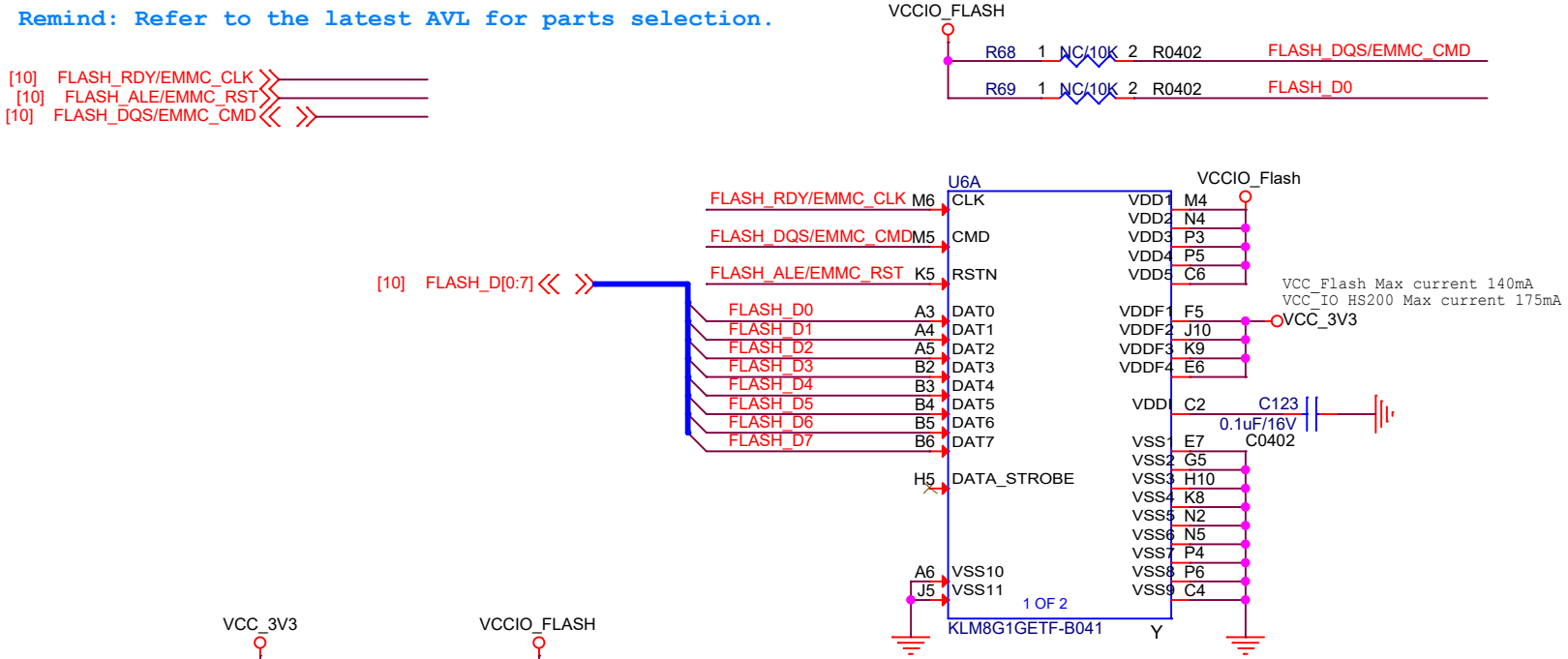

**Note:**
**Vih=VCC**
**Vil=VCC*Ron/(Ron+Rodt)**
**VREFDQ_DDR=(Vih+Vil)/2**

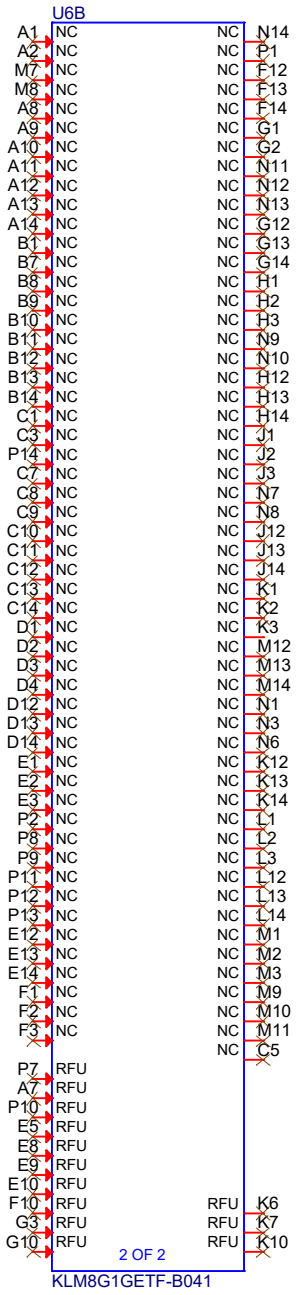
**eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm**
**so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V**

| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 18.RAM-LPDDR3(178P) 1x32bit | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 18 of 21 |

# eMMC Flash

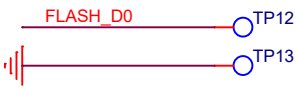
**Remind: Refer to the latest AVL for parts selection.**



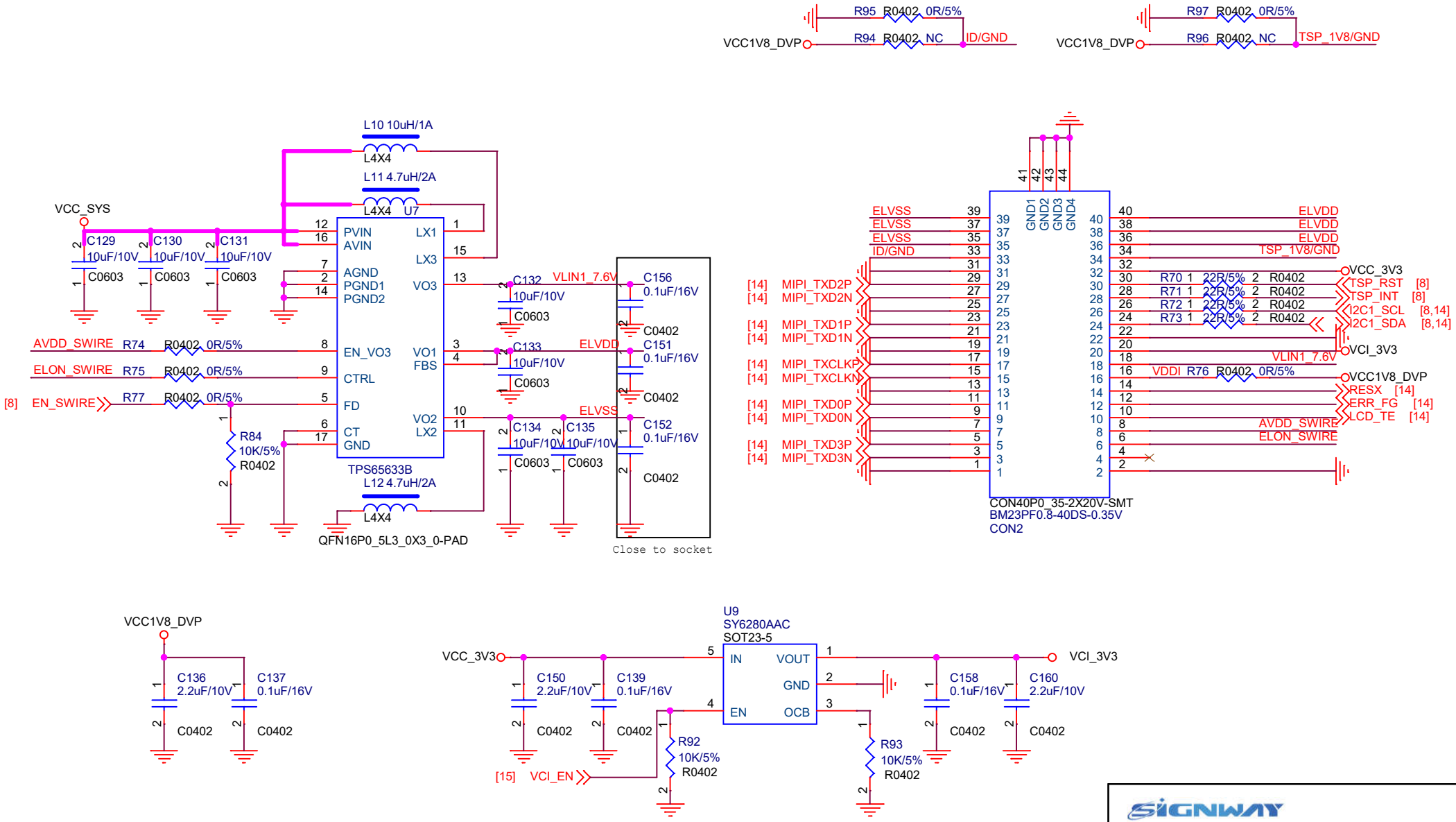

Note:All the Power filter capacitors should be placed close to the power pins of eMMC Flash
所有电源去耦电容必须靠近eMMC Flash电源管脚放置。

Note:
Reserve TestPoint for firmware update.
If FLASH_D0=0V at power-on reset,
then system will enter into Maskrom mode.
预留用于固件升级的测试点，上电复位情况下如果FLASH_D0为低电平，系统会进入Maskrom模式。




| | | | |
|---|---|---|---|
| Project: | RK3326_TABLET_REF | | |
| File: | 19.Flash-eMMC Flash | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 19 of 21 |

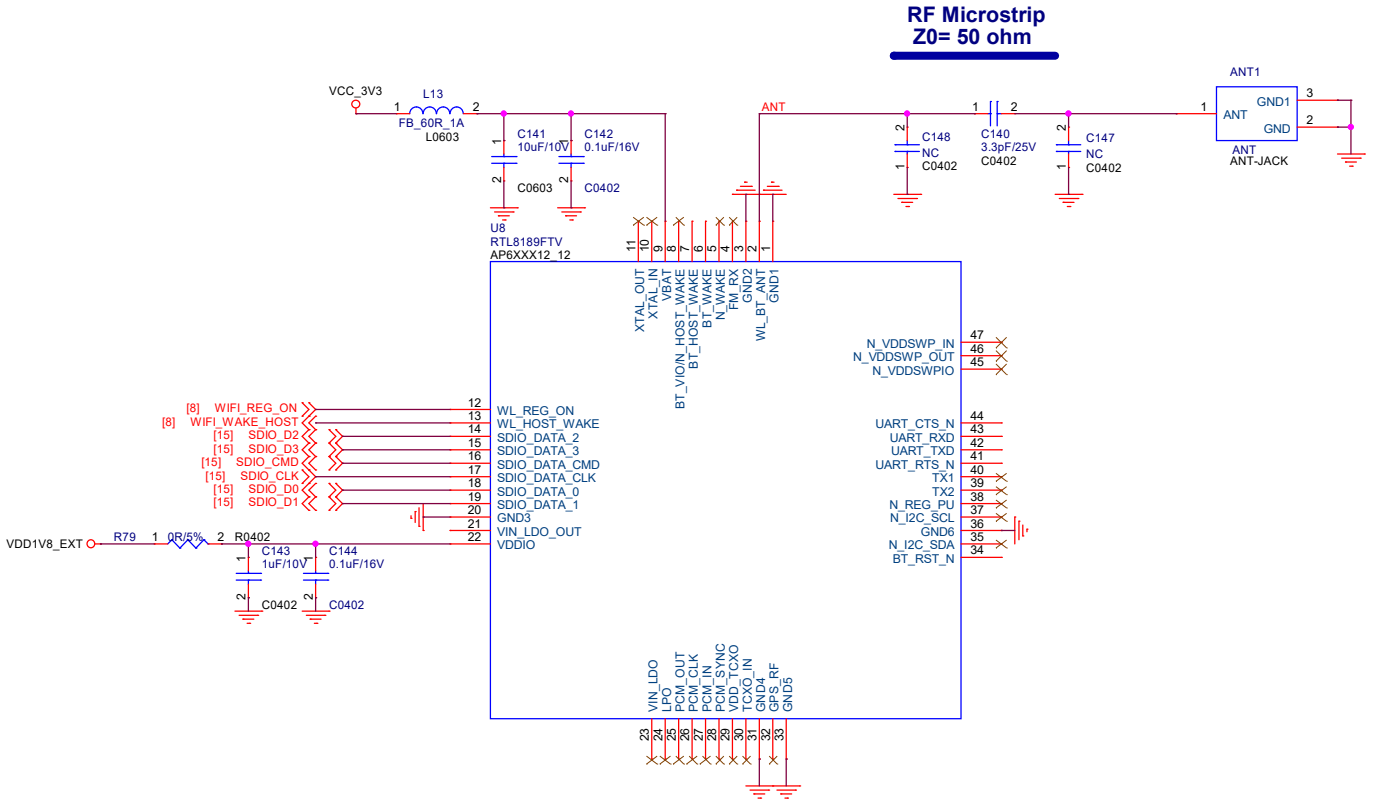
# MIPI Panel




| | | | |
|---|---|---|---|
| SIGNWAY | | | |
| Project: | RK3326_TABLET_REF | | |
| File: | 20.LCM-MIPI Panel | | |
| Date: | Monday, March 16, 2020 | Rev: | <V1.0> |
| Designed by: | Yangyin | Sheet: | 20 of 21 |

# WIFI/BT Module

Note:VBAT voltage range is 3.0V-4.8V,
and peak-current is at least 400mA.




Note:
Yes: option circuit be mounted
No: option circuit not be mounted

| OPTION | WIFI | | | | BT | Crystals | VCCIO_SDIO | OPTION1 | OPTION2 | OPTION3 | OPTION4 | OPTION5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | a | b/g/n | ac | 5GHz | | | | | | | | |
| AW-CM256SM | Yes | Yes | Yes | Yes | Yes | 37.4MHz | 1.71-3.6V | Yes | Yes | Yes@SDIO2.0<br>No@SDIO3.0 | Yes | No |
| AP6212 | No | Yes | No | No | Yes | 26MHz | 1.71-3.6V | Yes | Yes | No | Yes | No |
| AP6255 | Yes | Yes | Yes | Yes | Yes | 37.4MHz | 1.71-3.6V | Yes | Yes | Yes@SDIO2.0<br>No@SDIO3.0 | Yes | No |
| RTL8723BS | No | Yes | No | No | Yes | Module Integrated | 1.62-3.6V | No | No | No | Yes | No |
| RTL8723DS | No | Yes | No | No | Yes | Module Integrated | 1.62-3.6V | No | No | No | No | Yes |
| RTL8189ETV Module | No | Yes | No | No | No | Module Integrated | 1.8-3.3V | No | No | No | No | No |

| | |
|---|---|
| Project: | RK3326_TABLET_REF |
| File: | 21.SDIO WIFI/BT-1T1R |
| Date: | Monday, March 16, 2020 |
| Rev: | <V1.0> |
| Designed by: | Yangyin |
| Sheet: | 21 of 21 |